AmPAL22V10

24-Pin IMOX™ Programmable Array Logic (PAL)

Distinctive Characteristics

- Second-generation PAL device architecture
- Increased logic power — up to 22 inputs and 10 outputs
- Increased product terms — average 12 per output
- Variable product term distribution improves ease of use
- Each output user programmable for registered or combinatorial operation
- Individually user programmable output polarity
- Extra terms provide logical synchronous PRESET and asynchronous RESET capability
- Comes in standard and high-speed versions — 18 ns typical propagation delay
- PRELOAD for improved testability
- Packaged in 24-pin Slim DIP and 28-pin chip carrier packages
- Platinum-Silicide fuses ensure high programming yield, fast programming and high reliability
- AC and DC testing done at the factory utilizing special designed-in test features

General Description

The AmPAL22V10 is a second-generation Programmable Array Logic (PAL) device. It utilizes the familiar sum-of-products (AND-OR) logic structure, allowing users to program custom logic functions. The AmPAL22V10 is an extension of the PAL device concept. The AmPAL22V10 permits the development of custom LSI functions of 500 to 800 equivalent gate complexity.

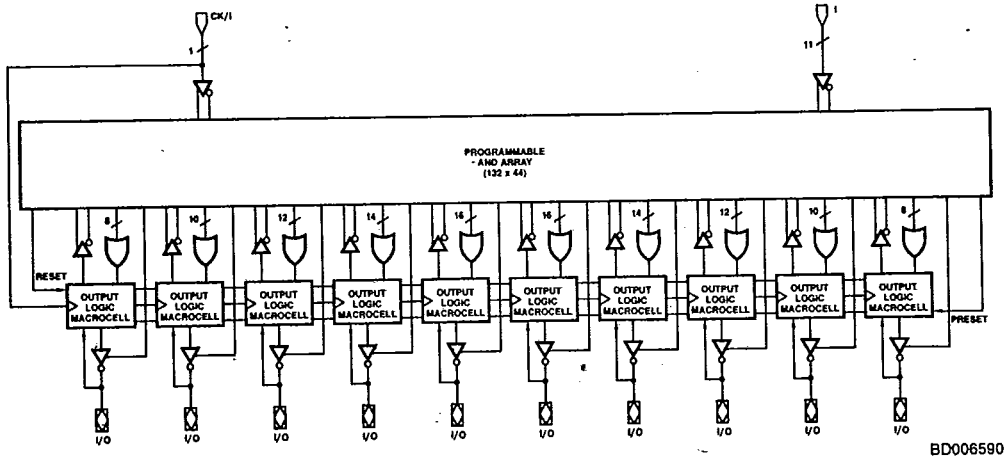
The AmPAL22V10 contains up to 22 inputs and 10 outputs. It incorporates the capability of defining and programming the architecture of each output on an individual basis. Each output is user programmable for either registered or combinatorial operation. This allows the designer to optimize the device design, by having only as many registers as needed. In addition each output has user-programmable output polarity, further simplifying design and contributing to the precise application requirements.

Increased logic power has been built into the AmPAL22V10 by increasing the number of product terms from 8-per-output to an average of 12-per-output. Further innovation can be seen in the introduction of variable product term distribution. This technique allocates from 8 to 16 logical product terms to each output (please refer to block diagram for distribution details). This variable allocation of terms allows far more complex functions to be implemented than in previous devices .

System operation has been enhanced by the addition of a synchronous-PRESET and an asynchronous-RESET product term. These terms are common to all output registers.

The AmPAL22V10 also incorporates power-up RESET and the capability to PRELOAD the output registers to any desired state during testing. PRELOAD is essential to permit full logical verification during test.

Block Diagram



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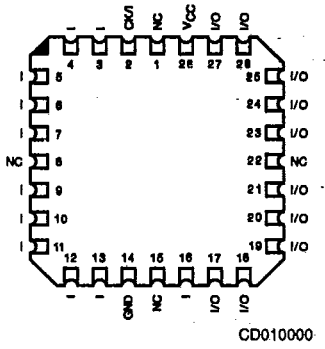
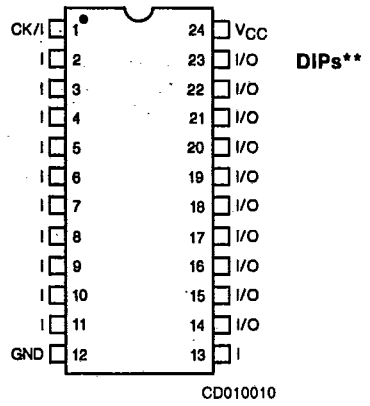
Connection Diagram

Top View





*Also available in PLCC. Pinouts identical to LCC.
**Also available in Flatpack. Pinouts identical to DIPs.

Ordering Information

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

A. Device Number
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing

AMPAL22V10 A D C

E. OPTIONAL PROCESSING
Blank = Standard processing
B = Burn-in

D. TEMPERATURE RANGE
C = Commercial (0 to +75°C)
E = Extended Commercial (–55 to +125°C)

C. PACKAGE TYPE
P = 24-Pin Plastic DIP (PD3024)
D = 24-Pin Ceramic DIP (CD3024)
J = 28-Pin Plastic Leaded Chip Carrier (PL 028)
L = 28-Pin Ceramic Leadless Chip Carrier (CL 028)

B. SPEED OPTION
Blank = 35 ns
A = 25 ns

A. DEVICE NUMBER/DESCRIPTION
AmPAL22V10
24-Pin IMOX Programmable Array Logic

Valid Combinations	
AMPAL22V10	PC, DC, DCB, DE, JC, LC, LE
AMPAL22V10A	

Valid Combinations

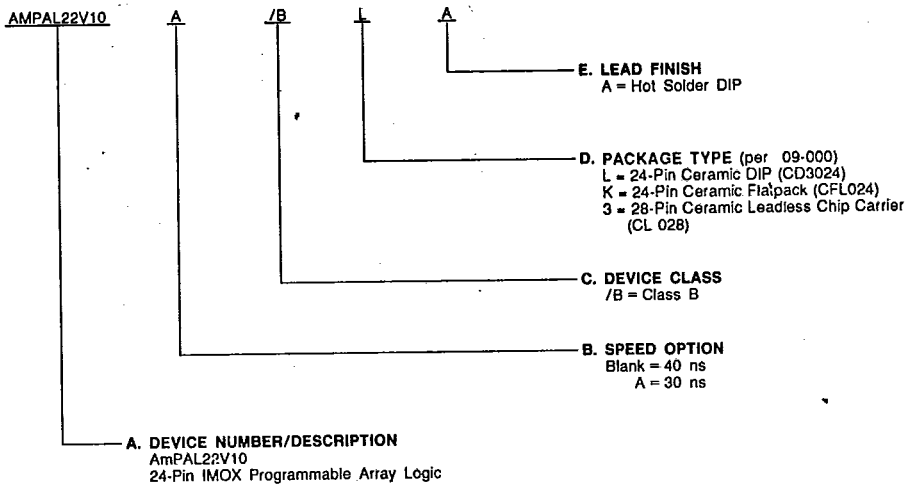
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Ordering Information

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

A. Device Number
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AMPAL22V10 AMPAL22V10A	/BLA/B3A/BKA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, and 11.

DESC Certified PAL Devices

Generic	AMD Part Number	DESC Numbers
22V10	AmPAL22V10A/BLA	5962-8605301LX
	AmPAL22V10A/B3A	5962-86053013X
	AmPAL22V10A/BKA	5962-8605301KX

Functional Description

The AmPAL22V10 is a second-generation Programmable Array Logic device. It contains a programmable fuse array organized in the familiar sum-of-products (AND-OR) structure.

The block diagram below shows the basic architecture of the AmPAL22V10. There up to 22 inputs and 10 outputs available. The inputs are connected to a programmable-AND array which contains 120 logical product terms. Initially the AND gates are connected, via fuses, to both the TRUE and complement of every input. By selective programming of fuses the AND gates may be "connected" to only the TRUE input (by blowing the complement fuse), to only the complement input (by blowing the TRUE fuse), or to neither type of input (by blowing both fuses) establishing a logical "don't care." When both the TRUE and complement fuses are left intact, a logical FALSE results on the output of the AND gate. An AND gate with all fuses blown will assume the logical-TRUE state. The outputs of the AND gates are connected to fixed-OR gates. There is an average of 12 product terms per OR gate (output), and as the block diagram shows, variable product term distribution has been implemented. This technique allocates different quantities of logical product terms to different outputs, allowing more complex logical functions to be performed than were previously possible. Up to 16 logical terms can be evaluated in one output in a single clock cycle (no feedback necessary).

Output Logic Macrocells (OLMs)

A dramatic innovation in logic design is the implementation on the AmPAL22V10 of variable output architecture. This allows the user to program on an output-by-output basis the function of the outputs. As shown in the Output Logic Macrocell (OLM) diagram below, each output cell contains two additional fuses (S_0 and S_1). S_1 controls whether the output will be registered or combinatorial. S_0 controls the output polarity (active HIGH or active LOW). Depending on the states of these 2 fuses, an individual output will operate in one of four modes (see logic diagrams on next page). Registered/Active LOW; Registered/Active HIGH; Combinatorial/Active LOW; Combinatorial/Active HIGH. (Note that the feedback path also changes with output mode.) This innovation gives the designer more flexibility and enables him to optimize the device for precise application requirements. It also allows for better device utilization — you only program as many registers as are needed.

PRESET/RESET

To improve in-system functionality, the AmPAL22V10 has additional PRESET and RESET product terms. These terms are connected to all registered outputs. When the synchronous-PRESET product term is asserted (HIGH), the output registers will be loaded with a HIGH on the next LOW-to-HIGH clock transition. When the asynchronous-RESET product term is asserted (HIGH), the output registers will be immediately loaded with a LOW (independent of the clock). These functions are particularly useful for applications such as system power-on and reset.

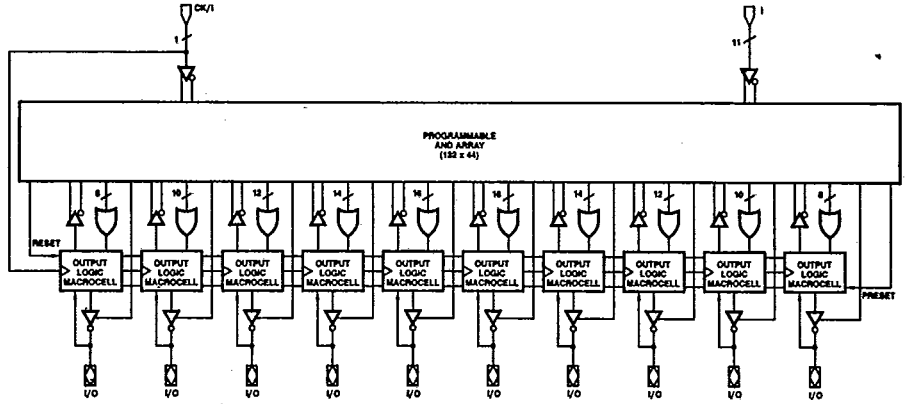
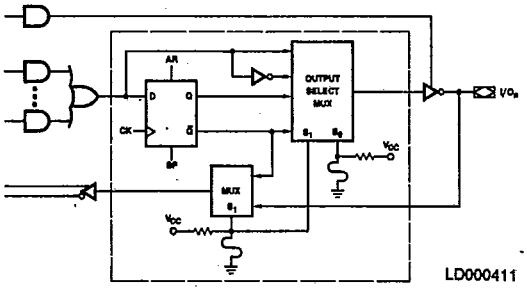


Figure 1. Block Diagram



S_1	S_0	Output Configuration
0	0	Registered/Active LOW
0	1	Registered/Active HIGH
1	0	Combinatorial/Active LOW
1	1	Combinatorial/Active HIGH

0 = Unblown Fuse
1 = Blown Fuse

Figure 2. Output Logic Macrocell Diagram

PRELOAD

To simplify testing, the AmPAL22V10 is designed with PRELOAD circuitry that provides an easy method of testing registered devices for logical functionality. PRELOAD allows any arbitrary state value to be loaded into the output registers.

A typical functional test sequence would be to verify all possible state transitions for the device being tested. To verify these transitions requires the ability to set the state registers into an arbitrary "present state" value and to set the device inputs to any arbitrary "present input" value. Once this is done, the state machine is then clocked into a new state, or "next state." The next state is then checked to validate the transition from the present state. In this way any state transition can be checked.

Fabrication

The AmPAL22V10 is manufactured using Advanced Micro Devices' IMOX oxide isolation process. This advanced process permits an increase in density and a decrease in internal capacitance resulting in the fastest possible programmable logic devices.

The AmPAL22V10 is fabricated with AMD's fast programming, highly reliable Platinum-Silicide Fuse technology. Utilizing an easily implemented programming algorithm, these products can be rapidly programmed to any customized pattern. Extra test words are preprogrammed during manufacturing to ensure extremely high field programming yields (> 98.5%), and provide extra test paths to achieve excellent parametric correlation.

Platinum Silicide was selected as the fuse-link material to achieve a well-controlled melt rate resulting in large nonconductive gaps that ensure very stable, long-term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers high reliability for fusible link programmable logic.

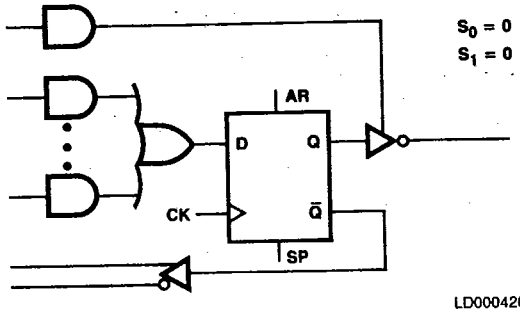


Figure 3-1. Registered/Active LOW

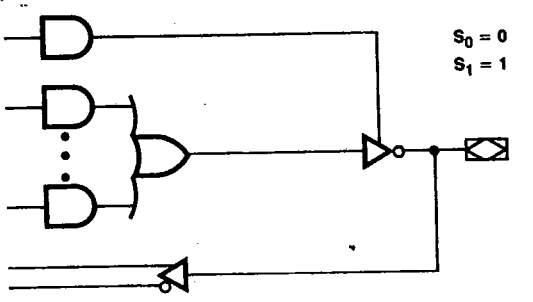


Figure 3-3. Combinatorial/Active LOW

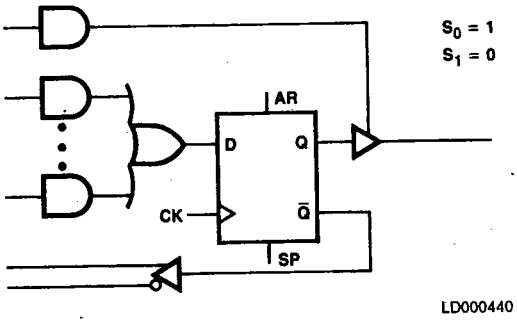


Figure 3-2. Registered/Active HIGH

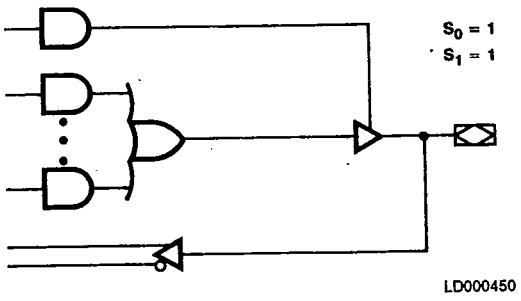
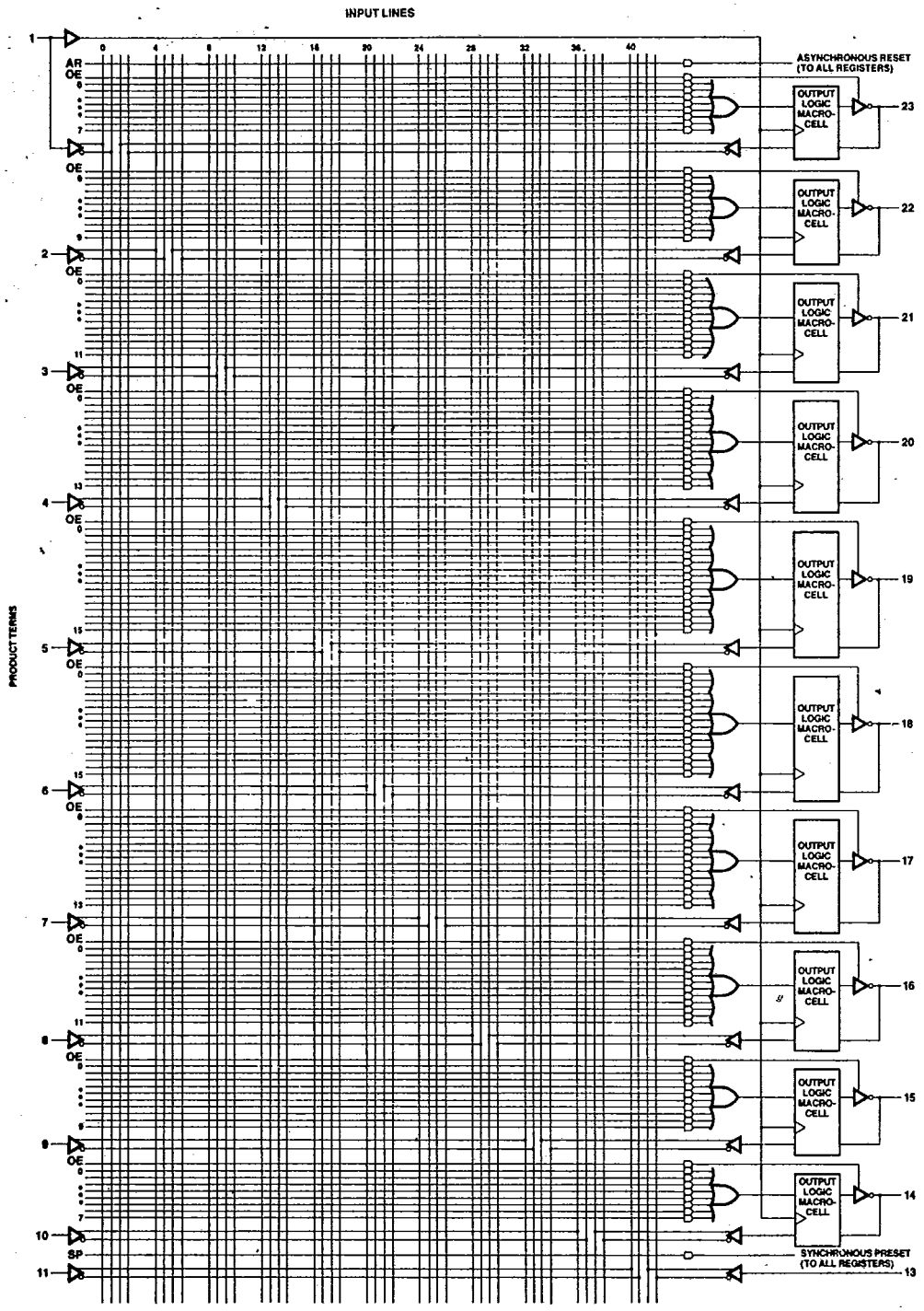


Figure 3-4. Combinatorial/Active HIGH



*Pinout for DIPs only.

Figure 4. AmPAL22V10* Logic Diagram

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Absolute Maximum Ratings

Storage Temperature ..... −65 to +150°C
Supply Voltage to Ground Potential
(Pin 24 to Pin 12) Continuous ..... −0.5 to +7 V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5 V to +V_{CC} Max.
DC Voltage Applied to Outputs
During Programming ..... 16 V
Output Current Into Outputs During Programming
(Max. Duration of 1 sec) ..... 200 mA
DC Input Voltage ..... −0.5 to +5.5 V
DC Input Current ..... −30 to +5 mA
Ambient Temperature with Power Applied ..... +125°C

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Operating Ranges

Commercial (C) Devices
Temperature (T_A) Operating Free Air ..... 0°C to +75°C
Supply Voltage (V_{CC}) ..... +4.75 to +5.25 V

Extended Commercial (E) Devices
Temperature (T_A) ..... −55°C Min.
Temperature (T_C) ..... +125°C Max.
Supply Voltage (V_{CC}) ..... +4.50 to +5.50 V

Military (M) Devices*
Temperature (T_A) ..... −55°C Min.
Temperature (T_C) Operating Case ..... +125°C Max.
Supply Voltage (V_{CC}) ..... +4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military Product 100% tested at T_C = +25°C, +125°C, and −55°C.

DC Characteristics

over operating range unless otherwise specified; included in Group A, Subgroup 1, 2, 3 tests unless otherwise noted

Parameter Symbol	Parameter Description	Test Conditions			Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.2 mA	C Devices	2.4	3.5		Volts
			I_{OH} = −2 mA	E/M Devices				
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA	C Devices			0.50	Volts
			I_{OL} = 12 mA	E/M Devices				
V_{IH} (Note 2)	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for all Inputs			2.0			Volts
V_{IL} (Note 2)	Input LOW Level	Guaranteed Input Logical LOW Voltage for all Inputs					0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.40 V				−20	−100	μA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V					25	μA
I_I	Input HIGH Current	V_{CC} = Max., V_{IN} = 5.5 V					1.0	mA
I_{SC}	Output Short-Circuit Current	V_{CC} = Max., V_{OUT} = 0.5 V (Note 3)			−30	−50	−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max.				150	180	mA
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA				−0.9	−1.2	Volts
I_{OZH}	Output Leakage Current (Note 4)	V_{CC} = Max., V_{IN} = V_{IL} or V_{IH}	V_O = 2.7 V				100	μA
I_{OZL}			V_O = 0.4 V				−100	
C_{IN} †	Input Capacitance	V_{IN} = 2.0 V @ f = 1 MHz (Note 5)		Pins 1, 13		11		pF
				Others		6		
C_{OUT} †	Output Capacitance	V_{OUT} = 2.0 V @ f = 1 MHz (Note 5)				9		pF

Notes: 1. Typical limits are at V_{CC} = 5.0 V and T_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.
4. I/O pin leakage is the worst case of I_{OZX} or I_{IX} (where X = H or L).
5. Pinout for DIPs only.

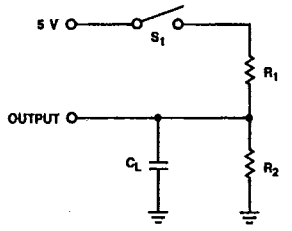
† Not included in Group A tests.

Switching Characteristics over operating range unless otherwise specified; included in Group A, Subgroup 7, 8, 9, 10, 11 tests unless otherwise noted

Parameter Symbol	Parameter Description	Test Conditions	Typ. (Note 1)	C Devices "A" Min.	C Devices "A" Max.	C Devices "Std" Min.	C Devices "Std" Max.	E/M Devices "A" Min.	E/M Devices "A" Max.	E/M Devices "Std" Min.	E/M Devices "Std" Max.	Units
t_{PD}	Input or Feedback to Non-Registered Output	C Devices $R_1 = 300$ $R_2 = 390$	18		25		35		30		40	ns
t_{EA}	Input to Output Enable		18		25		35		30		40	ns
t_{ER}	Input to Output Disable		18		25		35		30		40	ns
t_{CO}	Clock to Output		10		15		25		20		25	ns
t_S	Input or Feedback Setup Time		13	20		30		25		35		ns
t_H	Hold Time		-10	0		0		0		0		ns
t_P	Clock Period ($t_S + t_{CO}$)			35		55		45		60		ns
t_W	Clock Width			15		25		20		30		ns
f_{MAX}	Maximum Frequency	E/M Devices $R_1 = 390$ $R_2 = 750$			28.5		18		22		16.5	MHz
t_{AW}	Asynchronous Reset Width			25		35		30		40		ns
t_{AR}	Asynchronous Reset Recovery Time			25		35		30		40		ns
t_{AP}	Asynchronous Reset to Registered Output Reset				30		40		35		45	ns

Notes:
1. Typical limits are at $V_{CC} = 5.0$ V and $T_A = 25°C$.
2. t_{PD} is tested with switch S_1 closed and $C_L = 50$ pF.
3. For three-state outputs, output enable times are tested with $C_L = 50$ pF to the 1.5 V level; S_1 is open for high-impedance to HIGH tests and closed for high-impedance to LOW tests. Output disable times are tested with $C_L = 5$ pF. HIGH to high-impedance tests are made to an output voltage of $V_{OH} - 0.5$ V with S_1 open; LOW to high-impedance tests are made to the $V_{OL} + 0.5$ V level with S_1 closed.

Switching Test Circuit



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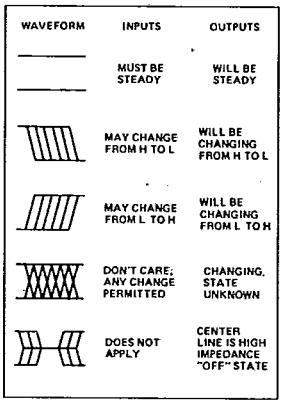
Key to Switching Waveforms



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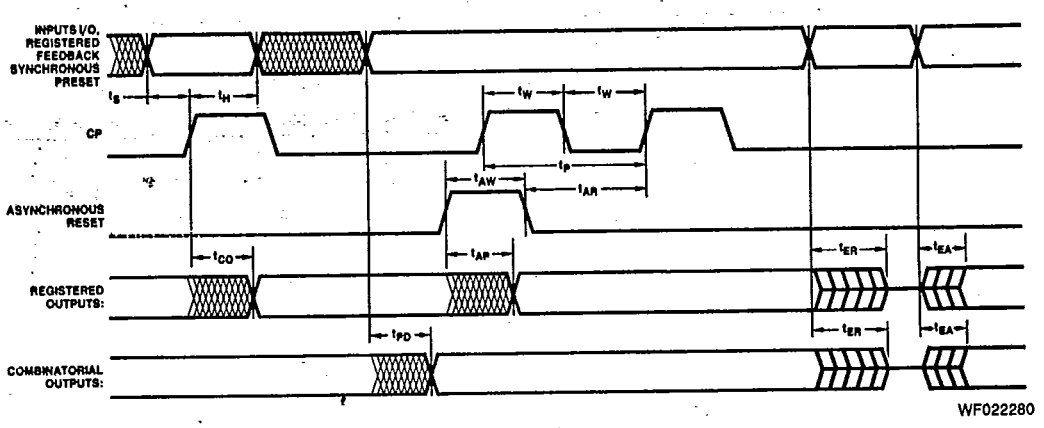
Switching Waveforms



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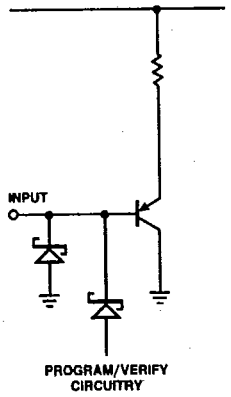
Input/Output Current Diagram



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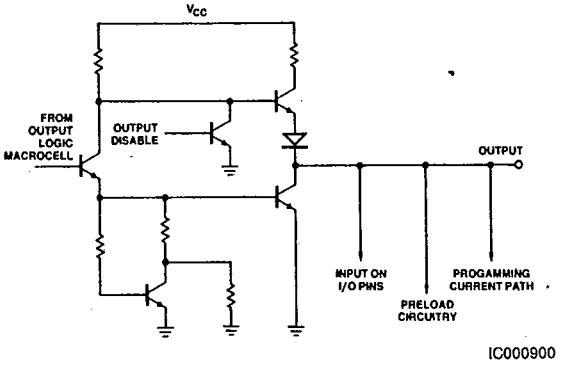
Input Circuitry



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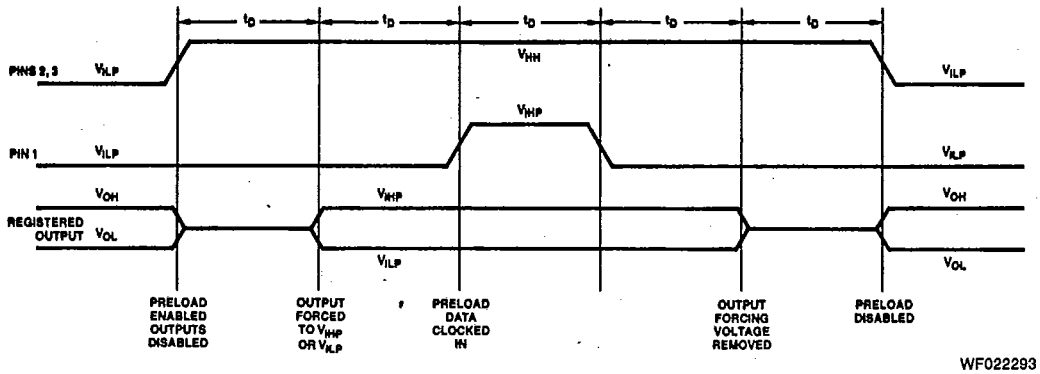
Output Circuitry

PRELOAD of Registered Outputs

The AmPAL22V10 registered outputs are provided with circuitry to allow loading each register synchronously with either a HIGH or LOW. This feature will simplify testing since any state can be loaded into the registers to control test sequencing.

The pin levels and timing necessary to perform the PRELOAD function are detailed below. Parameters are listed in the Programming Parameters table (page 12).



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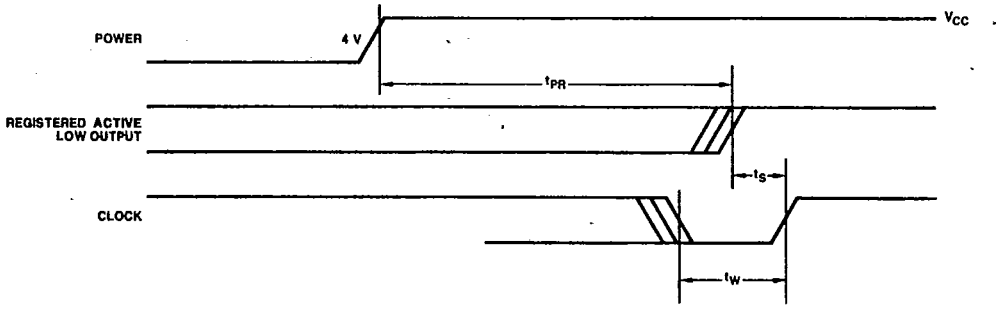
Par.	Min.	Max.
V_{HH}	10	12
V_{ILP}	0	0.5
V_{IHP}	2.4	5.5

Level forced on registered output pin during PRELOAD cycle	Register Q output state after cycle
V_{IHP}	HIGH
V_{ILP}	LOW

Power-up RESET

The registered devices in the AMD PAL Family have been designed with the capability to reset during system power-up. Following power-up, all registers will be reset to LOW. The output state will depend on the polarity of the output buffer. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the asynchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.



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Parameter Symbol	Parameter Description	Min.	Typ.	Max.	Units
t_{PR}	Power-Up Reset Time		600	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics			
t_W	Clock Width				

Security Fuse Programming

A single fuse is provided on each AmPAL22V10 part to prevent unauthorized copying of PAL fuse patterns. Once blown, the circuitry enabling fuse verification and registered output PRELOAD is permanently disabled.

Programming of the security fuse is the same as an array fuse. Verification of a blown security fuse is accomplished by verifying the whole fuse array as if every fuse is blown.

Programmers/Development Systems

(refer to Programmer Reference Guide, page 3-81)