

FEATURES

Complete Analog I/O Port for Voiceband DSP

Applications

Linear-Coded 16-Bit Sigma-Delta ADC

Linear-Coded 16-Bit Sigma-Delta DAC

On-Chip Anti-Aliasing and Anti-Imaging Filters

On-Chip Voltage Reference

8 kHz Sampling Frequency

Twos Complement Coding

65 dB SNR + THD

Programmable Gain on DAC and ADC

Serial Interface To DSP Processors

24-Pin DIP/28-Lead SOIC

Single 5 V Power Supply

GENERAL DESCRIPTION

The AD28msp02 Voiceband Signal Port is a complete analog front end for high performance voiceband DSP applications. Compared to traditional μ -law and A-law codecs, the AD28msp02's linear-coded ADC and DAC maintain wide dynamic range while maintaining superior SNR and THD. A sampling rate of 8.0 kHz coupled with 65 dB SNR + THD performance make the AD28msp02 attractive in many telecom and speech processing applications, for example digital cellular radio and high quality telephones. The AD28msp02 simplifies overall system design by requiring only a single +5 V power supply.

The inclusion of on-chip anti-aliasing and anti-imaging filters, 16-bit sigma-delta ADC and DAC, and programmable gain amplifiers ensures a highly integrated and compact solution to voiceband analog processing requirements. Sigma-delta conversion technology eliminates the need for complex off-chip anti-aliasing filters and sample-and-hold circuitry.

The AD28msp02's serial I/O port provides an easy interface to host DSP microprocessors such as the ADSP-2101, ADSP-2105 and ADSP-2111. The AD28msp02 is available in a 24-pin, 0.3" plastic DIP and a 28-lead SOIC package.

FUNCTIONAL DESCRIPTION

Figure 1 shows a block diagram of the AD28msp02.

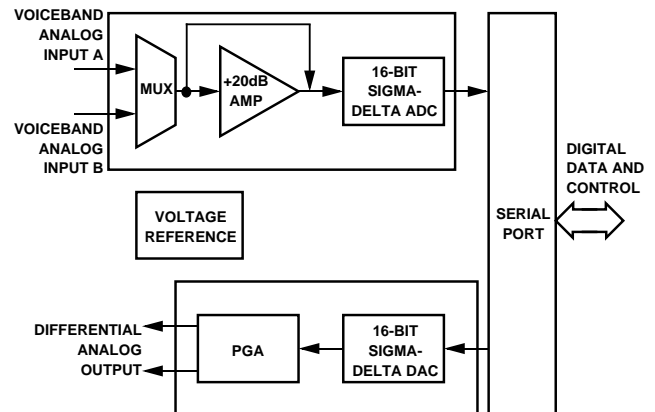
A/D CONVERSION

The A/D conversion circuitry of the AD28msp02 consists of two analog input amplifiers, an optional 20 dB preamplifier, and a sigma-delta analog-to-digital converter (ADC). The analog input signal to the AD28msp02 must be ac-coupled.

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FUNCTIONAL BLOCK DIAGRAM



Analog Input Amplifiers

The two analog input amplifiers (NORM, AUX) are internally biased by an on-chip voltage reference in order to allow operation of the AD28msp02 with a single +5 V power supply.

An analog multiplexer selects either the NORM or AUX amplifier as the input to the ADC's sigma-delta modulator. The optional 20 dB preamplifier may be used to increase the signal level; the preamplifier can be inserted before the modulator or can be bypassed. Input signal level to the sigma-delta modulator should not exceed V_{INMAX} , which is specified under "Analog Interface Electrical Characteristics." Refer to "Analog Input" in the "Design Considerations" section of this data sheet for more information.

The input multiplexer and 20 dB preamplifier are configured by Bits 0 and 1 (IPS, IMS) of the AD28msp02's control register. If the multiplexer setting is changed while an input signal is being processed, the ADC's output must be allowed time to settle to ensure that the output data is valid.

ADC

The ADC consists of a 2nd-order analog sigma-delta modulator, an anti-aliasing decimation filter, and a digital high-pass filter. The sigma-delta modulator noise-shapes the signal and produces 1-bit samples at a 1.0 MHz rate. This bit stream, which represents the analog input signal, is fed to the anti-aliasing decimation filter.

Decimation Filter

The anti-aliasing decimation filter contains two stages. The first stage is a sinc^4 digital filter that increases resolution to 16 bits and reduces the sample rate to 40 kHz. The second stage is an IIR low-pass filter.

AD28msp02

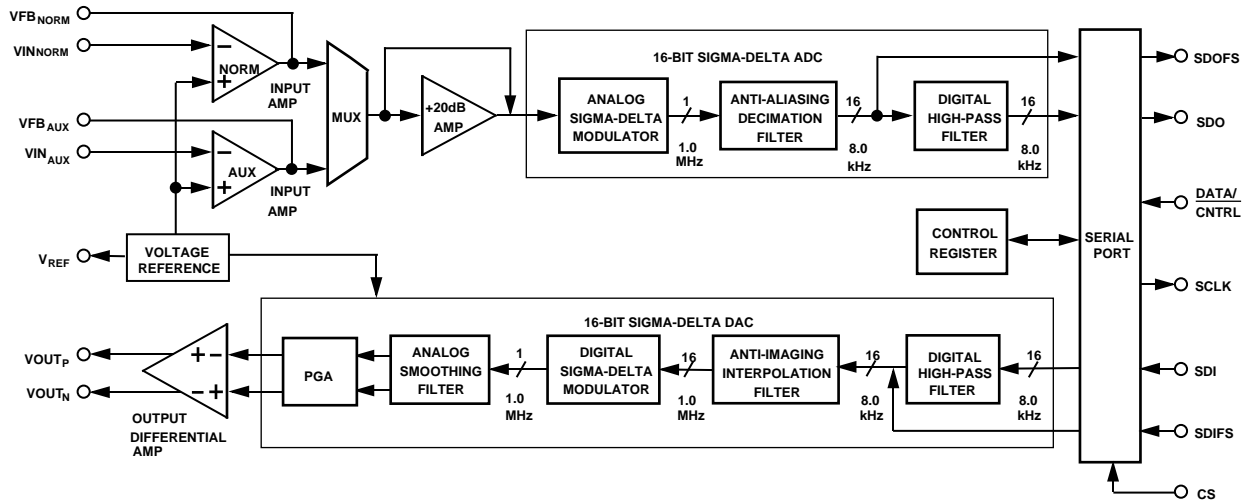


Figure 1. AD28msp02 Block Diagram

The IIR low-pass filter is a 10th-order elliptic filter with a passband edge at 3.7 kHz and a stopband attenuation of 65 dB at 4 kHz. This filter has the following specifications:

| | |
|-------------------|----------------------------------|
| Filter type: | 10th-order low-pass elliptic IIR |
| Sample frequency: | 40.0 kHz |
| Passband cutoff:* | 3.70 kHz |
| Passband ripple: | ±0.2 dB |
| Stopband cutoff: | 4.0 kHz |
| Stopband ripple: | -65.00 dB |

*The passband cutoff frequency is defined to be the last point in the passband that meets the passband ripple specification.

(Note that these specifications apply only to this filter, and not to the entire ADC. The specifications can be used to perform further analysis of the exact characteristics of the filter, for example using a digital filter design software package.)

Figure 2 shows the frequency response of the IIR low-pass filter.

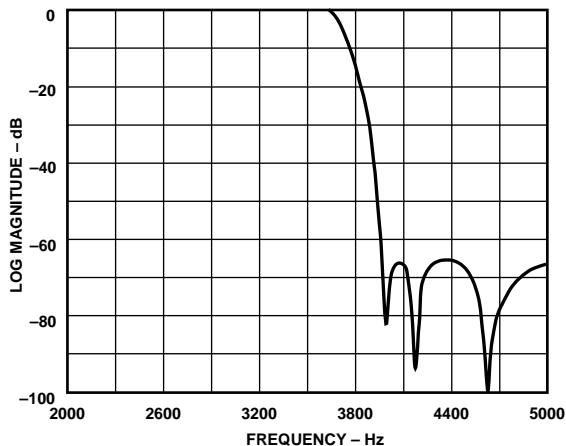


Figure 2. IIR Low-Pass Filter Frequency Response

High-Pass Filter

The digital high-pass filter removes frequency components at the low end of the spectrum; it attenuates signal energy below the passband of the converter. The high-pass filter can be bypassed by setting the ADBY bit (Bit 3) of the AD28msp02's control register.

The high-pass filter is a 4th-order elliptic filter with a passband cutoff at 150 Hz. Stopband attenuation is 25 dB. This filter has the following specifications:

| | |
|-------------------|----------------------------------|
| Filter type: | 4th-order high-pass elliptic IIR |
| Sample frequency: | 8.0 kHz |
| Passband cutoff: | 150.0 Hz |
| Passband ripple: | ±0.2 dB |
| Stopband cutoff: | 100.0 Hz |
| Stopband ripple: | -25.00 dB |

(Note that these specifications apply only to this filter, and not to the entire ADC. The specifications can be used to perform further analysis of the exact characteristics of the filter, for example using a digital filter design software package.)

Figure 3 shows the frequency response of the high-pass filter.

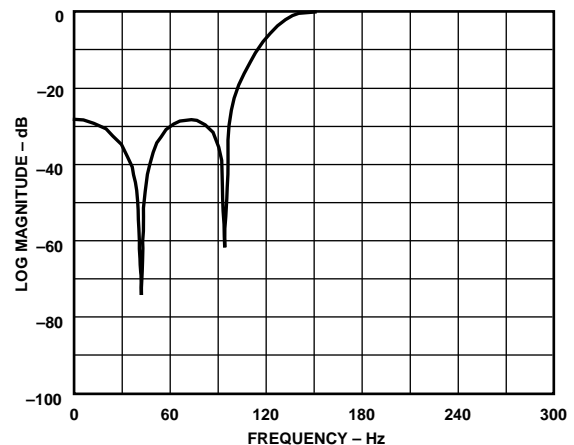


Figure 3. High-Pass Filter Frequency Response

Passband ripple is ±0.2 dB for the combined effects of the ADC's digital filters (i.e., high-pass filter and IIR low-pass of the decimation filter) in the 300 Hz–3400 Hz passband.

The output of the ADC is transferred to the AD28msp02's serial port (SPORT) at an 8 kHz rate, for transmission to the host DSP processor. Maximum group delay in the ADC will not exceed 1 ms in the region from 300 Hz to 3 kHz.

PIN DESCRIPTIONS

| Pin Name | I/O/Z | Function |
|---------------------|-------|--|
| VIN _{NORM} | I | Analog input to inverting terminal of NORM input amplifier. |
| VFB _{NORM} | O | Output terminal of NORM amplifier. |
| VIN _{AUX} | I | Analog input to inverting terminal of AUX input amplifier. |
| VFB _{AUX} | O | Output terminal of AUX amplifier. |
| VOU _{Tp} | O | Analog output from noninverting terminal of differential output amplifier. |
| VOU _{Tn} | O | Analog output from inverting terminal of differential output amplifier. |
| V _{REF} | O | On-chip bandgap voltage reference (2.5 V ± 10%). |
| MCLK | I | Master clock input; frequency must equal 13.0 MHz to guarantee listed specifications. |
| SCLK | O/Z | Serial clock used to clock data or control bits to and from the serial port (SPORT). The frequency of SCLK is equal to the frequency of the master clock (MCLK) divided by 5. SCLK is 3-stated when CS is low. |
| SDI | I | Serial data input of SPORT. Both data and control information are input on this pin. Input at SDI is ignored when CS is low. |
| SDO | O/Z | Serial data output of SPORT. Both data and control information are output on this pin. SDO is 3-stated when CS is low. |
| SDIFS | I | Framing signal for SDI serial transfers. Input at SDIFS is ignored when CS is low. |
| SDOFS | O/Z | Framing signal for SDO serial transfers. SDOFS is 3-stated when CS is low. |
| DATA/ <u>CNTRL</u> | I | Configures AD28msp02 for either data or control information transfers (via SPORT). |
| CS | I | Active-high chip select. Can be used to 3-state the SPORT interface; when CS is low, the SCLK, SDO, and SDOFS outputs are 3-stated and the SDI and SDIFS inputs are ignored. If CS is deasserted during a serial data transfer, the 16-bit word being transmitted is lost. |
| <u>RESET</u> | I | Active low reset signal; resets Control Register and clears digital filters. <u>RESET</u> does not 3-state the SPORT outputs (SCLK, SDO, SDOFS). |
| V _{CC} | | Analog supply voltage; nominal +5 V. |
| GND _A | | Analog ground. |
| V _{DD} | | Digital supply voltage; nominal +5 V. |
| GND _D | | Digital ground. |

D/A CONVERSION

The D/A conversion circuitry of the AD28msp02 consists of a sigma-delta digital-to-analog converter (DAC), an analog smoothing filter, a programmable gain amplifier, and a differential output amplifier.

DAC

The AD28msp02's sigma-delta DAC implements digital filters and a sigma-delta modulator with the same characteristics as the filters and modulator of the ADC. The DAC consists of a digital high-pass filter, an anti-imaging interpolation filter, and a digital sigma-delta modulator.

The DAC receives 16-bit samples from the host DSP processor via AD28msp02's serial port at an 8 kHz rate. If the host processor fails to write a new value to the serial port, the existing (previous) data is read again. The data stream is filtered first by the DAC's high-pass filter and then by the anti-imaging interpolation filter. These filters have the same characteristics as the ADC's anti-aliasing decimation filter and digital high-pass filter.

The output of the interpolation filter is fed to the DAC's digital sigma-delta modulator, which converts the 16-bit data to 1-bit samples at a 1.0 MHz rate. The modulator noise-shapes the signal such that errors inherent to the process are minimized in the passband of the converter. The bit stream output of the sigma-delta modulator is fed to the AD28msp02's analog smoothing filter where it is converted to an analog voltage.

High-Pass Filter

The digital high-pass filter of the AD28msp02's DAC has the same characteristics as the high-pass filter of the ADC. The high-pass filter removes frequency components at the low end of the spectrum; it attenuates signal energy below the passband of the converter. The DAC's high-pass filter can be bypassed by setting the DABY bit (Bit 2) of the AD28msp02's control register.

The high-pass filter is a 4th-order elliptic filter with a passband cutoff at 150 Hz. Stopband attenuation is 25 dB. This filter has the following specifications:

| | |
|-------------------|----------------------------------|
| Filter type: | 4th-order high-pass elliptic IIR |
| Sample frequency: | 8.0 kHz |
| Passband cutoff: | 150.0 Hz |
| Passband ripple: | ±0.2 dB |
| Stopband cutoff: | 100.0 Hz |
| Stopband ripple: | -25.00 dB |

(Note that these specifications apply only to this filter, and not to the entire DAC. The specifications can be used to perform further analysis of the exact characteristics of the filter, for example using a digital filter design software package.)

Figure 3 shows the frequency response of the high-pass filter.

Interpolation Filter

The anti-imaging interpolation filter contains two stages. The first stage is an IIR low-pass filter that interpolates the data rate from 8 kHz to 40 kHz and removes images produced by the interpolation process. The output of this stage is then interpolated to 1.0 MHz and fed to the second stage, a sinc⁴ digital filter that attenuates images produced by the 40 kHz to 1.0 MHz interpolation process.

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The IIR low-pass filter is a 10th-order elliptic filter with a passband edge at 3.70 kHz and a stopband attenuation of 65 dB at 4 kHz. This filter has the following specifications:

| | |
|-------------------|----------------------------------|
| Filter type: | 10th-order low-pass elliptic IIR |
| Sample frequency: | 40.0 kHz |
| Passband cutoff:* | 3.70 kHz |
| Passband ripple: | ±0.2 dB |
| Stopband cutoff: | 4.0 kHz |
| Stopband ripple: | -65.00 dB |

*The passband cutoff frequency is defined to be the last point in the passband that meets the passband ripple specification.

(Note that these specifications apply only to this filter, and not to the entire DAC. The specifications can be used to perform further analysis of the exact characteristics of the filter, for example using a digital filter design software package.)

Figure 2 shows the frequency response of the IIR low-pass filter.

Passband ripple is ±0.2 dB for the combined effects of the DAC's digital filters (i.e., high-pass filter and IIR low pass of the interpolation filter) in the 300 Hz–3400 Hz passband.

Analog Smoothing Filter and Programmable Gain Amplifier

The programmable gain amplifier (PGA) can be used to adjust the output signal level by -15 dB to +6 dB. This gain is selected by bits 7–9 (OG0, OG1, OG2) of the AD28msp02's control register.

The AD28msp02's analog smoothing filter consists of a 2nd-order Sallen-Key continuous-time filter and a 3rd-order switched capacitor filter. The Sallen-Key filter has a 3 dB point at approximately 80 kHz.

Differential Output Amplifier

The AD28msp02's analog output (VOUT_P, VOUT_N) is produced by a differential output amplifier. The differential amplifier can drive loads of 2 kΩ or greater and has a maximum differential output voltage swing of ±3.156 V peak-to-peak (3.17 dBm0). The output signal is dc-biased to the AD28msp02's on-chip voltage reference (V_{REF}) and can be ac-coupled directly to a load or dc-coupled to an external amplifier. Refer to "Analog Output" in the "Design Considerations" section of this data sheet for more information.

The VOUT_P–VOUT_N outputs must be used as differential outputs; do not use either as a single-ended output.

SERIAL PORT

The AD28msp02 communicates with a host processor via the bidirectional synchronous serial port (SPORT). The SPORT is used to transmit and receive digital data and control information.

All serial transfers are 16 bits long, MSB first. Data bits are transferred at the serial clock rate (SCLK). SCLK equals the master clock frequency divided by 5. SCLK = 2.6 MHz for the master clock frequency MCLK = 13.0 MHz.

Host Processor Interface

The AD28msp02-to-host processor interface is shown in Figure 4.

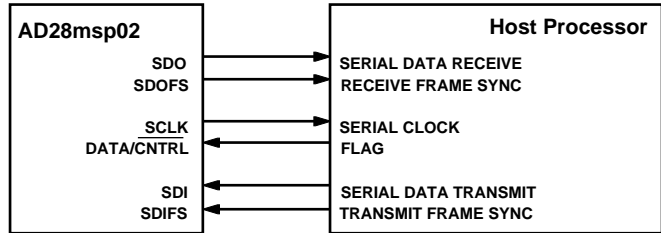


Figure 4. AD28msp02-to-Host Processor Interface

Table I describes the SPORT signals and how they are used to communicate with the host processor. The AD28msp02's chip select (CS) must be held high to enable SPORT operation. CS can be used to 3-state the SPORT pins and disable communication with the host processor.

To use the ADSP-2101 or ADSP-2111 as host DSP processor for the AD28msp02, the following connections can be used (as shown in Figure 5):

| AD28msp02 Pin | | ADSP-2101/2111 Pin |
|---------------|---|--------------------|
| SCLK | – | SCLK0 |
| SDO | – | DR0 |
| SDOFS | – | RFS0 |
| SDI | – | DT0 |
| SDIFS | – | TFS0 |
| DATA/CNTRL | – | FO (Flag Output) |

Table I. SPORT Signals

| Signal Name | Description | Generated By | Signal State When RESET Low (CS High) | Signal State During Powerdown (CS High) |
|-------------|-------------------------------|----------------|---------------------------------------|---|
| SCLK | Serial clock | AD28msp02 | Low | Active |
| SDO | Serial data output | AD28msp02 | Low | Active* |
| SDOFS | Serial data output frame sync | AD28msp02 | Low | Low |
| SDI | Serial data input | Host Processor | — | — |
| SDIFS | Serial data input frame sync | Host Processor | — | — |

(CS must be held high to enable SPORT operation.)

*Outputs last data value that was valid prior to entering powerdown.

Note that the ADSP-2101's SPORT0 communicates with the AD28msp02's SPORT while the ADSP-2101's Flag Output (FO) is used to signal the AD28msp02's DATA/CNTRL input. SPORT1 on the ADSP-2101 must be configured for flags and interrupts in this system.

Figure 6 shows an ADSP-2101 assembly language program that initializes the AD28msp02 and implements digital loopback through the DSP processor.

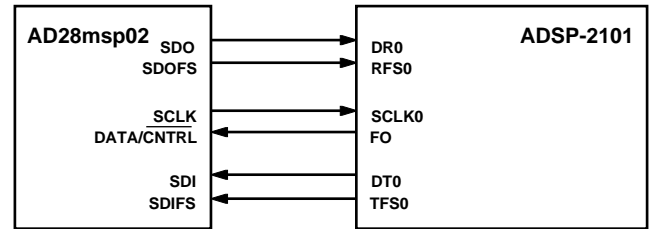


Figure 5. AD28msp02-to-ADSP-2101 Interface

```

{ This ADSP-2101 program initializes the AD28msp02 }
{ and executes a loopback, or talk-through, routine. }
.MODULE/ABS = 0/BOOT = 0 test1;

resetv:  JUMP begin;                {restart}
         RTI; RTI; RTI;

irq2v:   RTI; RTI; RTI; RTI;        {IRQ2}
st0x:    RTI; RTI; RTI; RTI;        {SPORT0 Tx}
sr0x:    ax0 = rx0;                 {SPORT0 Rx}
         tx0 = ax0;
         RTI; RTI;

irq1v:   RTI; RTI; RTI; RTI;        {irq1}
irq0v:   RTI; RTI; RTI; RTI;        {irq0}
timerv:  RTI; RTI; RTI; RTI;

begin:   RESET FLAG_OUT;
         AX0 = 0x2A0F;               {Configure ADSP-2101 SPORT0 for }
         DM (0x3FF6) = AX0;         { ext. SCLK, ext. RFS, int. TFS }

         AX0 = 0x101F;               { Enable ADSP-2101 SPORT0, }
         DM (0x3FFF) = AX0;         { configure SPORT1 for Flag Out }

         IMASK= 0x10;
         AX0 = 0x30;                 { Write control word to take}
         TX0 = AX0;                 { AD28msp02 out of powerdown }

         IDLE;
         NOP;
         IMASK= 0x08;
         SET FLAG_OUT;

wait:    JUMP wait;                 { Wait for receive interrupt }
         NOP;

.ENDMOD;

```

Figure 6. ADSP-2101 Digital Loopback Routine

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Serial Data Output

The AD28msp02's SPORT will begin transmitting data to the host processor at an 8 kHz rate when the PWDD and PWDA bits (Bits 4, 5) of the control register are set to 1. In the program shown in Figure 6, the instructions

AX0 = 0x30; { Write control word to take }

TX0 = AX0; { AD28msp02 out of powerdown }

accomplish this by writing 0x30 to the AD28msp02's control register. There is a short start-up time (after the end of this control register write) before the AD28msp02 raises SDOFS and begins transmitting data; see Figure 11.

At the 13 MHz MCLK frequency, data is transmitted at an 8 kHz rate with a single 16-bit word transmitted every 125 μ s. While data is being output, the AD28msp02 asserts SDOFS at an 8 kHz rate. Each 16-bit word transfer begins one serial clock cycle after SDOFS is asserted.

Serial Data Input

The host processor must initiate data transfers to the AD28msp02 by asserting the serial data input frame sync (SDIFS) high. The 16-bit word transfer begins one serial clock cycle after SDIFS is asserted. The DATA/CNTRL line must be driven high when SDIFS is driven high.

The host processor must assert SDIFS shortly after the rising edge of SCLK and must maintain SDIFS high for one cycle. Data is then driven from the host processor (to the SDI input) shortly after the rising edge of the next SCLK and is clocked into the AD28msp02 on the falling edge of SCLK in that cycle.

Each bit of a 16-bit data word is thus clocked into the AD28msp02 on the falling edge of SCLK (MSB first).

If SDIFS is asserted high again before the end of the present data word transfer, it is not recognized until the falling edge of SCLK in the last (LSB) cycle.

(Note: Exact SPORT timing requirements are defined in the "Specifications" section of this data sheet.)

CONTROL REGISTER

The AD28msp02's control register configures the device for various modes of operation including ADC and DAC gain settings, ADC input mux selection, filter bypass, and powerdown. The AD28msp02's host processor can read and write to the control register through the AD28msp02's serial port (SPORT) by driving the DATA/CNTRL pin low.

The control register is cleared (set to 0x0000) when the AD28msp02 is reset.

Control Register Writes

To write the control register, the host processor must assert DATA/CNTRL low when it asserts SDIFS. If the MSB of the bit stream is also low, the SPORT recognizes the incoming serial data as a new control word and copies it to the AD28msp02's control register. The format for the control word write is shown in Table II; reserved Bits 10-15 must be set to zero.

Table II. Control Word Write Format

| | | | | | | | | | | | | | | | |
|----|----|----|----|----|----|-----|-----|-----|---|------|------|------|------|-----|-----|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | OG2 | OG1 | OG0 | 0 | PWDD | PWDA | ADBY | DABY | IMS | IPS |

| | | |
|-------|---------|--|
| 0 | IPS | Analog input preamplifier select: 1 = insert (+20 dB), 0 = bypass (0 dB) |
| 1 | IMS | Analog input multiplexer select: 1 = AUX input, 0 = NORM input |
| 2 | DABY | DAC high-pass filter bypass select: 0 = insert, 1 = bypass |
| 3 | ADBY | ADC high-pass filter bypass select: 0 = insert, 1 = bypass |
| 4 | PWDA | Powerdown analog: 0 = powerdown, 1 = operating |
| 5 | PWDD | Powerdown digital: 0 = powerdown, 1 = operating |
| 7-9 | OG2-OG0 | Analog output gain setting (for D/A output PGA) |
| 10-15 | | Reserved |

| Gain | OG2 | OG1 | OG0 |
|--------|-----|-----|-----|
| +6 dB | 0 | 0 | 0 |
| +3 dB | 0 | 0 | 1 |
| 0 dB | 0 | 1 | 0 |
| -3 dB | 0 | 1 | 1 |
| -6 dB | 1 | 0 | 0 |
| -9 dB | 1 | 0 | 1 |
| -12 dB | 1 | 1 | 0 |
| -15 dB | 1 | 1 | 1 |

Gain settings are accurate within ± 0.6 dB.

(Control Register is set to 0x0000 at RESET. Reserved Bits 10-15 must be set to 0 for all Control Register writes.)

Table III. Control Word Read Format

Read Request

| | | | | | | | | | | | | | | | |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Read Ready

| | | | | | | | | | | | | | | | |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Control Register Reads

To read the control register, the host processor must transfer two control words. For each transfer, the $\overline{\text{DATA/CNTRL}}$ pin must be low when SDIFS is asserted. If the MSB of the bit stream is high, the SPORT recognizes the incoming serial data as a request for control information. The protocol for reading the control register is as follows:

1. The host processor sends a “Read Request” control word to the AD28msp02. Since the MSB of this control word is high, the SPORT recognized the incoming serial data as a read request and does not overwrite the control register.
2. When the AD28msp02 receives the read request, it finishes any data transfers in progress and waits for a “Read Ready” control word.
3. The host processor then transfers a “Read Ready” control word to the AD28msp02. Upon receiving this control word, the AD28msp02 transfers the control register contents to the host processor via the SPORT.
4. When the SPORT completes the control register transfer, it immediately resumes transmitting data at an 8 kHz rate.

This scheme allows any data transfers in progress to be completed and resolves any ambiguities between data and control words. The format for the read control words is shown in Table III.

DESIGN CONSIDERATIONS**Analog Input**

The analog input signal to the AD28msp02 must be ac-coupled. Figure 7 shows the recommended input circuit for the AD28msp02’s analog input pin (either VIN_{NORM} or VIN_{AUX}). The circuit of Figure 7 implements a first-order low-pass filter with a 3 dB point at 20 kHz; this is the only filter that must be implemented external to the AD28msp02 to prevent aliasing of the sampled signal. Since the AD28msp02’s ADC uses a highly oversampled approach that transfers the bulk of the anti-aliasing filtering into the digital domain, the off-chip anti-aliasing filter need only be of low order.

In the circuit shown in Figure 7, scaling of the analog input is achieved by the resistors R_{IN} and R_{FB} . The input signal gain, $-R_{\text{FB}}/R_{\text{IN}}$, can be adjusted from -12 dB to $+26$ dB by varying the values of these resistors. The AD28msp02’s on-chip 20 dB preamplifier can be enabled when there is not enough gain in the input circuit; the preamplifier is configured by Bit 0 (IPS) of the control register. Total gain must be configured to ensure that a full-scale input signal (at C_{IN} in Figure 7) produces a signal level at the input to the sigma-delta modulator of the ADC that does not exceed V_{INMAX} , which is specified under “Analog Interface Electrical Characteristics.” If the total gain is increased above unity, signal-to-noise (SNR + THD) performance will not meet the listed specifications.

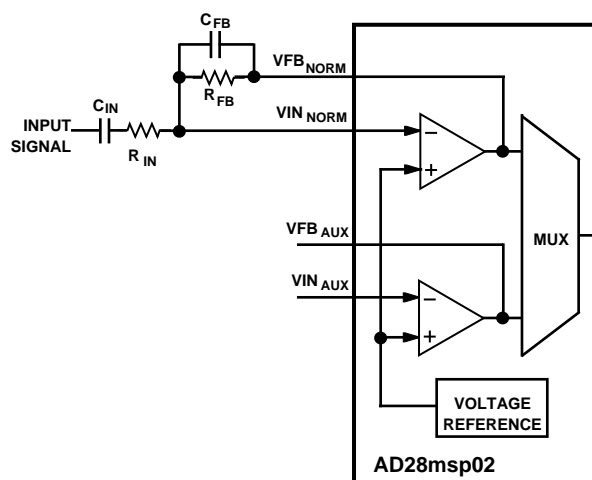


Figure 7. Recommended Analog Input Circuit

The dc biasing of the analog input signal is accomplished with an on-chip voltage reference which nominally equals 2.5 V. The input signal must be ac-coupled with an external coupling capacitor (C_{IN}). C_{IN} and R_{IN} should be chosen to ensure a coupling corner frequency of 30 Hz. C_{IN} should be 0.1 μF or larger.

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To select values for the components shown in Figure 7, use the following equations:

$$Gain = \frac{R_{FB}}{R_{IN}}$$

$$C_{IN} = \frac{1}{60 \pi R_{IN}}$$

$$C_{FB} = \frac{1}{(2 \pi)(20 \times 10^3) R_{FB}}$$

$10 \text{ k}\Omega \leq R_{FB}, R_{IN} \leq 50 \text{ k}\Omega$

$150 \text{ pF} \leq C_{FB} \leq 600 \text{ pF}$

Figure 8 shows an example of a typical input circuit configured for 0 dB gain. The circuit's diodes are used to prevent the input signal from exceeding maximum limits.

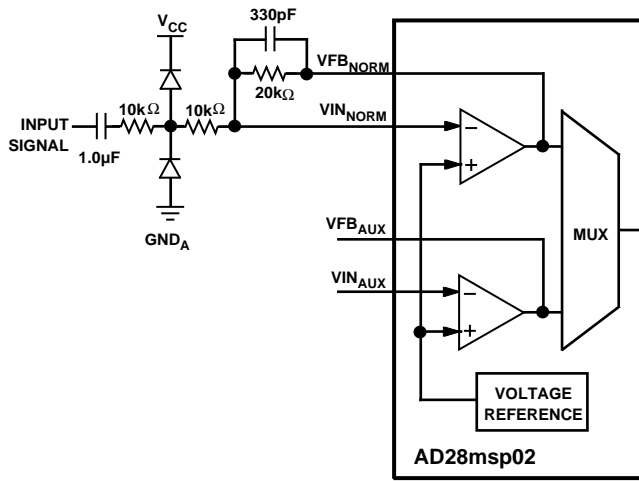


Figure 8. Example Analog Input Circuit for 0 dB Gain

Analog Output

The AD28msp02's differential analog output (V_{OUT_P} , V_{OUT_N}) is produced by an on-chip differential amplifier. The differential amplifier can drive a minimum load of $2 \text{ k}\Omega$ ($R_L \geq 2 \text{ k}\Omega$) and has a maximum differential output voltage swing of $\pm 3.156 \text{ V}$ peak-to-peak (3.17 dBm0). The differential output can be ac-coupled directly to a load or dc-coupled to an external amplifier.

Figure 9 shows a simple circuit providing a differential output with ac coupling. The capacitor of this circuit (C_{OUT}) is optional; if used, its value can be chosen as follows:

$$C_{OUT} = \frac{1}{(60 \pi) R_L}$$

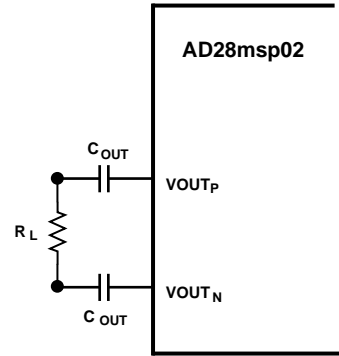


Figure 9. Example Circuit for Differential Output

The V_{OUT_P} – V_{OUT_N} outputs must be used as differential outputs; do not use either as a single-ended output. Figure 10 shows an example circuit which can be used to convert the differential output to a single-ended output. The circuit uses a differential-to-single-ended amplifier, the Analog Devices SSM2141.

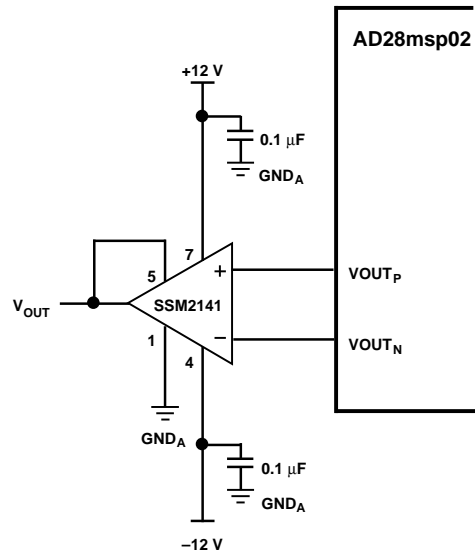


Figure 10. Example Circuit for Single-Ended Output

Serial Output Startup Time

The AD28msp02 begins transmitting data to the host processor after it is taken out of powerdown. To take the AD28msp02 out of powerdown, the host processor writes a control word to the AD28msp02.

The start-up time (from the start of this control word write) before the AD28msp02 begins transmitting data is shown in Figure 11.

PC Board Layout Considerations

Separate analog and digital ground planes should be provided for the AD28msp02 in order to ensure the characteristics of the device's ADC and DAC. The two ground planes should be connected at a single point—this is often referred to as a “Star” or “Mecca” grounding configuration. The point of connection may be at the system power supply, at the PC board power connection, or at any other appropriate location. Because ground loops increase susceptibility to EMF, multiple connections between the analog and digital ground planes should be avoided.

The ground planes should be designed such that all noise-sensitive areas are isolated from one another and critical signal

traces (such as digital clocks and analog signals) are as short as possible.

Each +5 V digital supply pin, V_{DD} , of the AD28msp02 (SOIC Pins 20, 21) should be bypassed to ground with a 0.1 μF capacitor. These capacitors should be low inductance, monolithic, ceramic, and surface-mount. The capacitor leads and PC board traces should be as short as possible to minimize inductive effects. In addition, a 10 μF capacitor should be connected between V_{DD} and ground, near the PC board power connection.

MCLK Frequency

The sigma-delta converters and digital filters of the AD28msp02 are specifically designed to operate at a master clock (MCLK) frequency of 13.0 MHz. MCLK must equal 13.0 MHz to guarantee the filter characteristics and sample rate of the ADC and DAC. The AD28msp02 is not tested or characterized at any other clock frequency.

A low cost crystal with a different frequency, for example 12.288 MHz, can be used for the master clock input; in this case, however, the AD28msp02 is not guaranteed to meet the specifications listed in this data sheet.

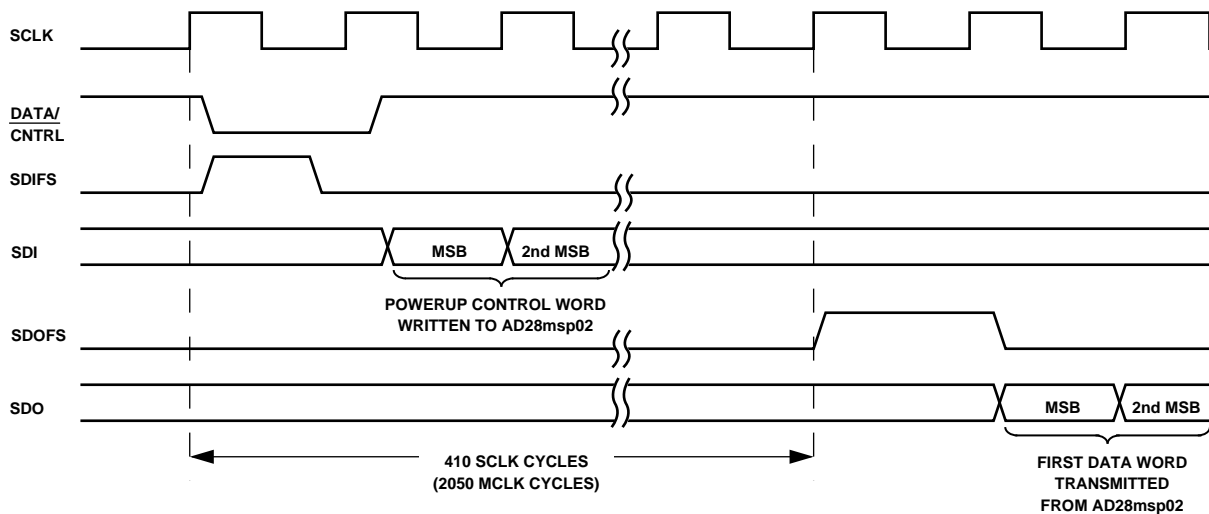


Figure 11. Serial Output Startup Time

AD28msp02

DEFINITION OF SPECIFICATIONS

Absolute Gain

Absolute gain is a measure of converter gain for a known signal. Absolute gain is measured with a 1.0 kHz sine wave at 0 dBm0. The absolute gain specification is used as a reference for gain tracking error specification.

Gain Tracking Error

Gain tracking error measures changes in converter output for different signal levels relative to an absolute signal level. The absolute signal level is 1 kHz at 0 dBm0 (equal to absolute gain). Gain tracking error at 0 dBm0 is 0 dB by definition.

SNR + THD

Signal-to-noise ratio plus total harmonic distortion is defined to be the ratio of the rms value of the measured input signal to the rms sum of all other spectral components in the frequency range 300 Hz–3400 Hz, including harmonics but excluding dc.

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, f_a and f_b , any active device with nonlinearities will create distortion products at sum and difference frequencies of $m f_a \pm n f_b$ where $m, n = 0, 1, 2, 3$, etc. Intermodulation terms are those for which neither m or n are equal to zero. For final testing, the second order terms include $(f_a + f_b)$ and $(f_a - f_b)$, while the third order terms include $(2f_a + f_b)$, $(2f_a - f_b)$, $(f_a + 2f_b)$, and $(f_a - 2f_b)$.

Idle Channel Noise

Idle channel noise is defined as the total signal energy measured at the output of the device when the input is grounded (measured in the frequency range 300 Hz–3400 Hz).

Crosstalk

Crosstalk is defined as the ratio of the amplitude of a full-scale signal appearing on one channel to the amplitude of the same signal which couples onto the adjacent channel. Crosstalk is expressed in dB.

Power Supply Rejection

Power supply rejection measures the susceptibility of a device to noise on the power supply. Power supply rejection is measured by modulating the power supply with a sine wave and measuring the noise at the output (relative to 0 dB).

Group Delay

Group delay is defined as the derivative of radian phase with respect to radian frequency, $\partial\phi(\omega)/\partial\omega$. Group delay is a measure of average delay of a system as a function of frequency. A linear system with a constant group delay has a linear phase response. The deviation of group delay away from a constant indicates the degree of nonlinear phase response of the system.

SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

| Parameter | | K Grade | | B Grade | | Unit |
|------------------|-------------------------------|---------|------|---------|------|------|
| | | Min | Max | Min | Max | |
| V_{DD}, V_{CC} | Supply Voltage | 4.50 | 5.50 | 4.50 | 5.50 | V |
| T_{AMB} | Ambient Operating Temperature | 0 | +70 | -40 | +85 | °C |

Refer to Environmental Conditions for information on case temperature and thermal specifications.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage -0.3 V to +7 V
 Input Voltage -0.3 V to $V_{DD} + 0.3$ V
 Output Voltage Swing -0.3 V to $V_{DD} + 0.3$ V
 Operating Temperature Range (Ambient) ... -40°C to +85°C
 Storage Temperature Range -55°C to +150°C
 Lead Temperature (5 sec) SOIC +280°C

*Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD SENSITIVITY

The AD28msp02 features proprietary input protection circuitry to dissipate high-energy discharges (Human Body Model). Per method 3015 of MIL-STD-883C, the AD28msp02 has been classified as a Class 1 device.

Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges readily accumulate on the human body and test equipment and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed.



AD28msp02

DIGITAL INTERFACE ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Min | Typ | Max | Unit | Test Condition |
|------------------|---|-----|-----|-----|------|--|
| V _{IH} | Input High Voltage | 2.4 | | | V | V _{DD} = max |
| V _{IL} | Input Low Voltage | | | 0.8 | V | V _{DD} = min |
| V _{OH} | Output High Voltage | 2.4 | | | V | V _{DD} = min, I _{OH} = -0.5 mA |
| V _{OL} | Output Low Voltage | | | 0.4 | V | V _{DD} = min, I _{OL} = 2 mA |
| I _{IH} | High Level Input Current | | | 10 | μA | V _{DD} = max, V _{IN} = max |
| I _{IL} | Low Level Input Current | | | 10 | μA | V _{DD} = max, V _{IN} = 0 V |
| I _{OZL} | Low Level Output 3-State Leakage Current | | | 10 | μA | V _{DD} = max, V _{IN} = max |
| I _{OZH} | High Level Output 3-State Leakage Current | | | 10 | μA | V _{DD} = max, V _{IN} = 0 V |
| C _I | Digital Input Capacitance | | | 10 | pF | |

ANALOG INTERFACE ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Min | Typ | Max | Unit |
|---------------------|---|------|-----|-------|-------|
| ADC: | | | | | |
| I _L | Input Leakage Current at V _{IN,NORM} , V _{IN,AUX} | | 10 | | nA |
| R _I | Input Resistance ¹ at V _{IN,NORM} , V _{IN,AUX} | | 100 | | MΩ |
| C _{IL} | Input Load Capacitance ¹ at V _{IN,NORM} , V _{IN,AUX} | | 10 | | pF |
| V _{IN,MAX} | Maximum Input Range ² | | | 3.156 | V p-p |
| DAC: | | | | | |
| R _O | Output Resistance ^{1,3} | | 1 | | Ω |
| V _{O,OFF} | Output DC Offset ⁴ | | | 400 | mV |
| C _{OL} | Output Load Capacitance ³ | | | 100 | pF |
| V _{V,REF} | Voltage Reference (V _{REF}) | 2.25 | | 2.75 | V |
| V _O | Maximum Voltage Output Swing (p-p) Across R _L | | | | |
| | Single-Ended | | | 3.156 | V |
| | Differential | | | 6.312 | V |
| R _L | Load Resistance ³ | 2 | | | kΩ |

Test Conditions for all analog interface tests: Unity input gain, A/D 20 dB preamplifier bypassed, D/A PGA set for 0 dB gain, no load on analog output (V_{OUT,P}-V_{OUT,N}).

¹Guaranteed but not tested.

²At input to sigma-delta modulator of ADC.

³At V_{OUT,P}-V_{OUT,N}.

⁴Between V_{OUT,P} and V_{OUT,N}.

POWER DISSIPATION

| Symbol | Parameter | Min | Max | Unit |
|-----------------|---|-----|-----|------|
| V _{CC} | Analog Operating Voltage | 4.5 | 5.5 | V |
| V _{DD} | Digital Operating Voltage | 4.5 | 5.5 | V |
| I _{DD} | Operating Current Active ¹ | | 40 | mA |
| P _I | Power Dissipation Active ¹ | | 200 | mW |
| I _{DD} | Operating Current Inactive ² | | 0.5 | mA |
| P _O | Power Dissipation Inactive ² | | 2.5 | mW |

Test conditions: V_{DD} = V_{CC} = 5.0 V, MCLK frequency 13.0 MHz, no load on digital pins, analog inputs ac-coupled to ground, no load on analog output (V_{OUT,P}-V_{OUT,N}).

¹Active: AD28msp02 operational (PWDD and PWDA set to 1 in control register).

²Inactive: AD28msp02 in powerdown state (PWDD and PWDA set to 0 in control register) and MCLK tied to V_{DD}.

TIMING PARAMETERS

Clock Signals

| Parameter | | Min | Max | Unit |
|----------------------------------|-----------------|-------------------|-------------------|------|
| <i>Timing Requirement:</i> | | | | |
| t_{MCK} | MCLK Period | 76.9 | 76.9 | ns |
| t_{MKL} | MCLK Width Low | $0.5t_{MCK} - 10$ | $0.5t_{MCK} + 10$ | ns |
| t_{MKH} | MCLK Width High | $0.5t_{MCK} - 10$ | $0.5t_{MCK} + 10$ | ns |
| <i>Switching Characteristic:</i> | | | | |
| t_{SCK} | SCLK Period | $5t_{MCK}$ | | ns |
| t_{SKL} | SCLK Width Low | $3t_{MCK} - 10$ | $3t_{MCK} + 10$ | ns |
| t_{SKH} | SCLK Width High | $2t_{MCK} - 10$ | $2t_{MCK} + 10$ | ns |

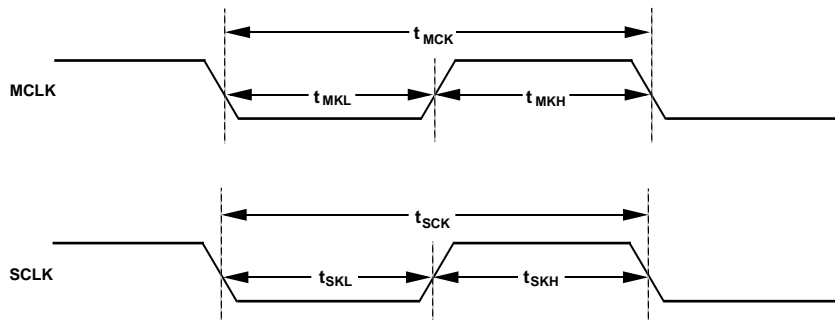


Figure 12. Clock Signals

Serial Port 3-State

| Parameter | | Min | Max | Unit |
|----------------------------------|------------------------------------|-----|-----|------|
| <i>Switching Characteristic:</i> | | | | |
| t_{SPD} | CS Low to SDO, SDOFS, SCLK Disable | | 25 | ns |
| t_{SPE} | CS High to SDO, SDOFS, SCLK Enable | 0 | | ns |
| t_{SPV} | CS High to SDO, SDOFS, SCLK Valid | | 10 | ns |

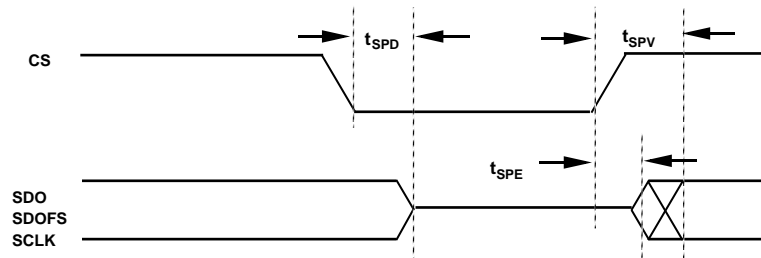


Figure 13. Serial Port 3-State

AD28msp02

Serial Ports

| Parameter | | Min | Max | Unit |
|----------------------------------|----------------------------------|-----|-----|------|
| <i>Timing Requirements:</i> | | | | |
| t_{SCS} | SDI/SDIFS Setup before SCLK Low | 10 | | ns |
| t_{SCH} | SDI/SDIFS Hold after SCLK Low | 10 | | ns |
| t_{DCS} | DATA/CNTRL Setup before SCLK Low | 10 | | ns |
| t_{DCH} | DATA/CNTRL Hold after SCLK Low | 10 | | ns |
| <i>Switching Characteristic:</i> | | | | |
| t_{RD} | SDOFS Delay from SCLK High | | 15 | ns |
| t_{RH} | SDOFS Hold after SCLK High | 0 | | ns |
| t_{SCDH} | SDO Hold after SCLK High | 0 | | ns |
| t_{SCDD} | SDO Delay from SCLK High | | 30 | ns |

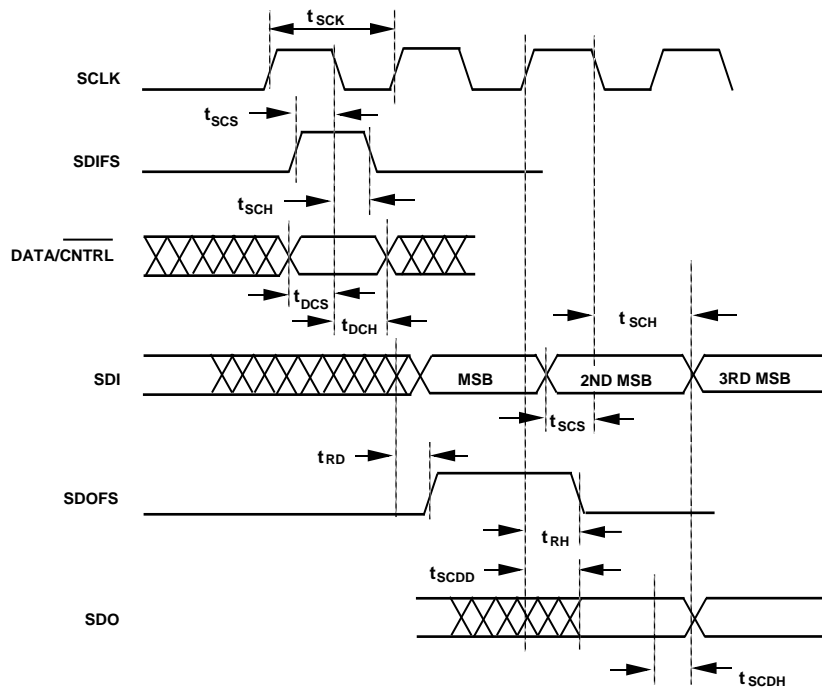


Figure 14. Serial Ports

DIGITAL TEST CONDITIONS

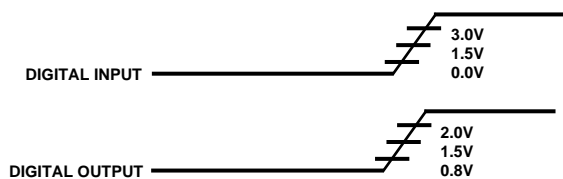


Figure 15. Voltage Reference Levels for AC Measurements

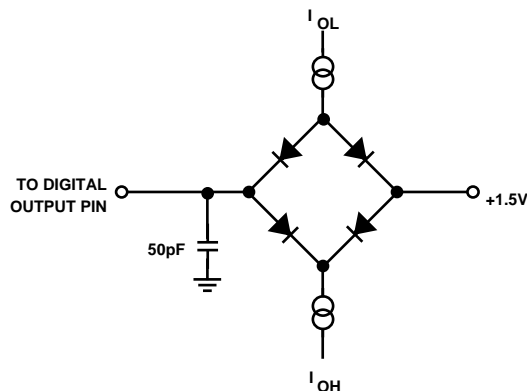


Figure 16. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

GAIN

| Parameter | Min | Typ | Max | Unit | Test Conditions |
|-------------------------|------|-----|-----|------|-------------------------|
| ADC Absolute Gain | -0.2 | 0 | 0.2 | dBm0 | 1.0 kHz, 0 dBm0 |
| ADC Gain Tracking Error | -0.1 | 0 | 0.1 | dBm0 | 1.0 kHz, +3 to -50 dBm0 |
| DAC Absolute Gain | -0.2 | 0 | 0.2 | dBm0 | 1.0 kHz, 0 dBm0 |
| DAC Gain Tracking Error | -0.1 | 0 | 0.1 | dBm0 | 1.0 kHz, +3 to -50 dBm0 |

FREQUENCY RESPONSE

| Input Freq (Hz) | Min Output (dB) | Max Output (dB) |
|-----------------|-----------------|-----------------|
| 0 | -∞ | -25 |
| 100 | -∞ | -25 |
| 150 | -0.3 | +0.3 |
| 200 | -0.3 | +0.3 |
| 300 | -0.2 | +0.2 |
| 1000 | -0.2 | +0.2 |
| 2000 | -0.2 | +0.2 |
| 3000 | -0.2 | +0.2 |
| 3400 | -0.2 | +0.2 |
| 3700 | -0.3 | +0.3 |
| 4000 | -∞ | -60 |
| >4000 | -∞ | -60 |

Frequency responses of ADC and DAC measured with input at audio reference level (the input level that produces an output level of -10 dBm0), with 20 dB preamplifier bypassed and input gain of 0 dB. The in-band ripple shall not exceed 0.2 dB.

AD28msp02

NOISE AND DISTORTION

| Parameter | Min | Max | Unit | Test Conditions |
|--------------------------------|-----|-----|------|---|
| ADC Intermodulation Distortion | | -70 | dB | ADC input signal level: 1.0 kHz, 0 dBm0 DAC input at idle ADC input signal level: analog ground DAC output signal level: 1.0 kHz, 0 dBm0 Input signal level at V_{CC} and V_{DD} pins: 1.0 kHz, 100 mV p-p sine wave Input signal level at V_{CC} and V_{DD} pins: 1.0 kHz, 100 mV p-p sine wave |
| DAC Intermodulation Distortion | | -70 | dB | |
| ADC Idle Channel Noise | | 72 | dBm0 | |
| DAC Idle Channel Noise | | 72 | dBm0 | |
| ADC Crosstalk | | -65 | dB | |
| DAC Crosstalk | | -65 | dB | |
| ADC Power Supply Rejection | | -55 | dB | |
| DAC Power Supply Rejection | | 55 | dB | |
| ADC Group Delay ¹ | | 1 | ms | |
| DAC Group Delay ¹ | | 1 | ms | |

¹Guaranteed but not tested.

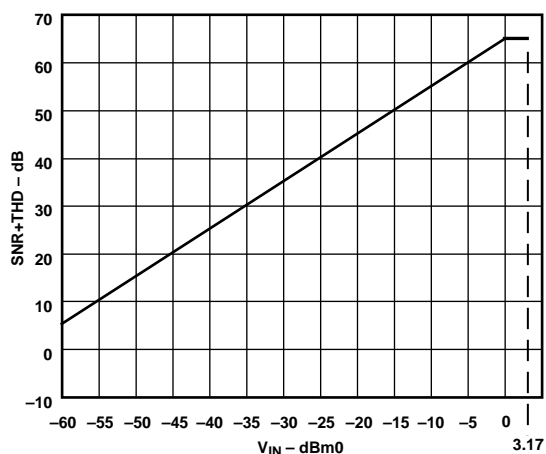


Figure 17. SNR + THD vs. V_{IN}

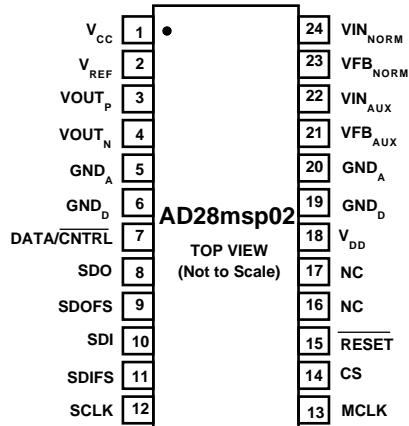
ORDERING GUIDE

| Part Number | Temperature Range | Package | Package Option* |
|-------------|-------------------|--------------------|-----------------|
| AD28msp02KN | 0°C to +70°C | 24-Pin Plastic DIP | N-24 |
| AD28msp02KR | 0°C to +70°C | 28-Lead SOIC | R-28 |
| AD28msp02BN | -40°C to +85°C | 24-Pin Plastic DIP | N-24 |
| AD28msp02BR | -40°C to +85°C | 28-Lead SOIC | R-28 |

*N = Plastic DIP, R = Small Outline (SOIC).

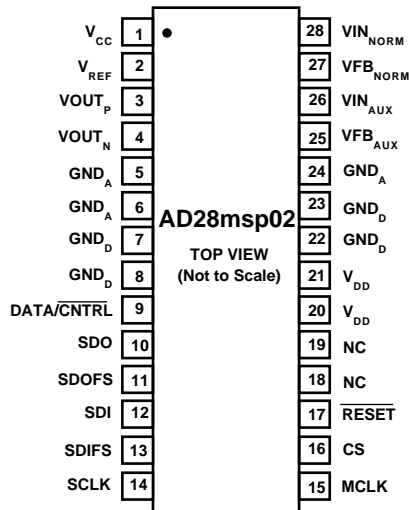
PIN CONFIGURATIONS

24-Pin Plastic DIP



NC = NO CONNECTION

28-Lead SOIC



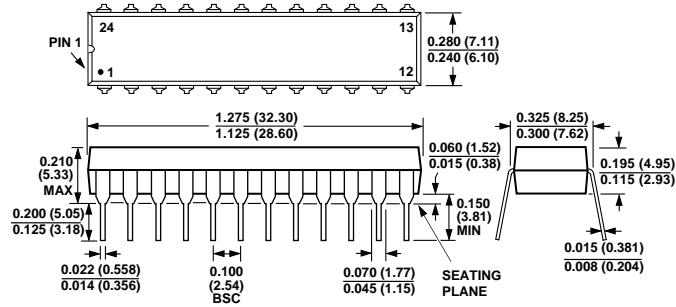
NC = NO CONNECTION

AD28msp02

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

24-Pin Plastic DIP (N-24)



28-Lead Wide-Body SOIC (R-28)

