68HC05BD7
68HC705BD7
68HC05BD2

SPECIFICATION

REV 2.0

(General Release)

Technical Operation Taiwan
Taipei, Taiwan

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SECTION 1 GENERAL DESCRIPTION

The MC68HC05BD7 HCMOS microcontroller is a member of the M68HC05 Family of low-cost single-chip microcontrollers. It is particularly suitable as multi-sync computer monitor controller. This 8-bit microcontroller unit (MCU) contains an on-chip oscillator, CPU, RAM, ROM, DDC12AB module, parallel I/O, Pulse Width Modulator, Multi-Function Timer, 6-bit ADC, and SYNC Processor.

1.1 Features

1.1.1 Hardware Features

- HC05 Core
- Low cost, HCMOS technology
- 40-pin DIP and 42-pin SDIP packages
- 256 Bytes of RAM for HC05BD2
- 384 Bytes of RAM for HC05BD7HC705BD7
- 5.75K-Bytes of User ROM for HC05BD2
- 11.75K-Bytes of User ROM for HC05BD7
- 11.5K-Bytes of User EPROM for HC705BD7
- 26 Bidirectional I/O lines: 14 dedicated and 12 multiplexed I/O lines. 4 of the 14 dedicated I/O lines and 6 of the 12 multiplexed I/O lines have max. +12V or +5V open-drain output buffers
- 16 x 8-bit PWM channels: Two 8-bit PWM channels have +12V open-drain outputs: 8 dedicated 8-bit PWM channels have +5V open-drain output options
- 6-bit ADC with 4 selectable input channels
- Multi-Function Timer (MFT) with Periodic Interrupt
- Sync Signal Processor module for processing horizontal, vertical, composite, and SOG SYNC signals; frequency counting; polarity detection; polarity controlled HSYNO and VSYNO or extracted VSYNC outputs, and CLAMP pulse output
- DDC12AB† module contains DDC1 hardware and multi-master I^2C†† hardware for DDC2AB protocol
- Software maskable Edge-Sensitive or Edge and Level-Sensitive External Interrupt

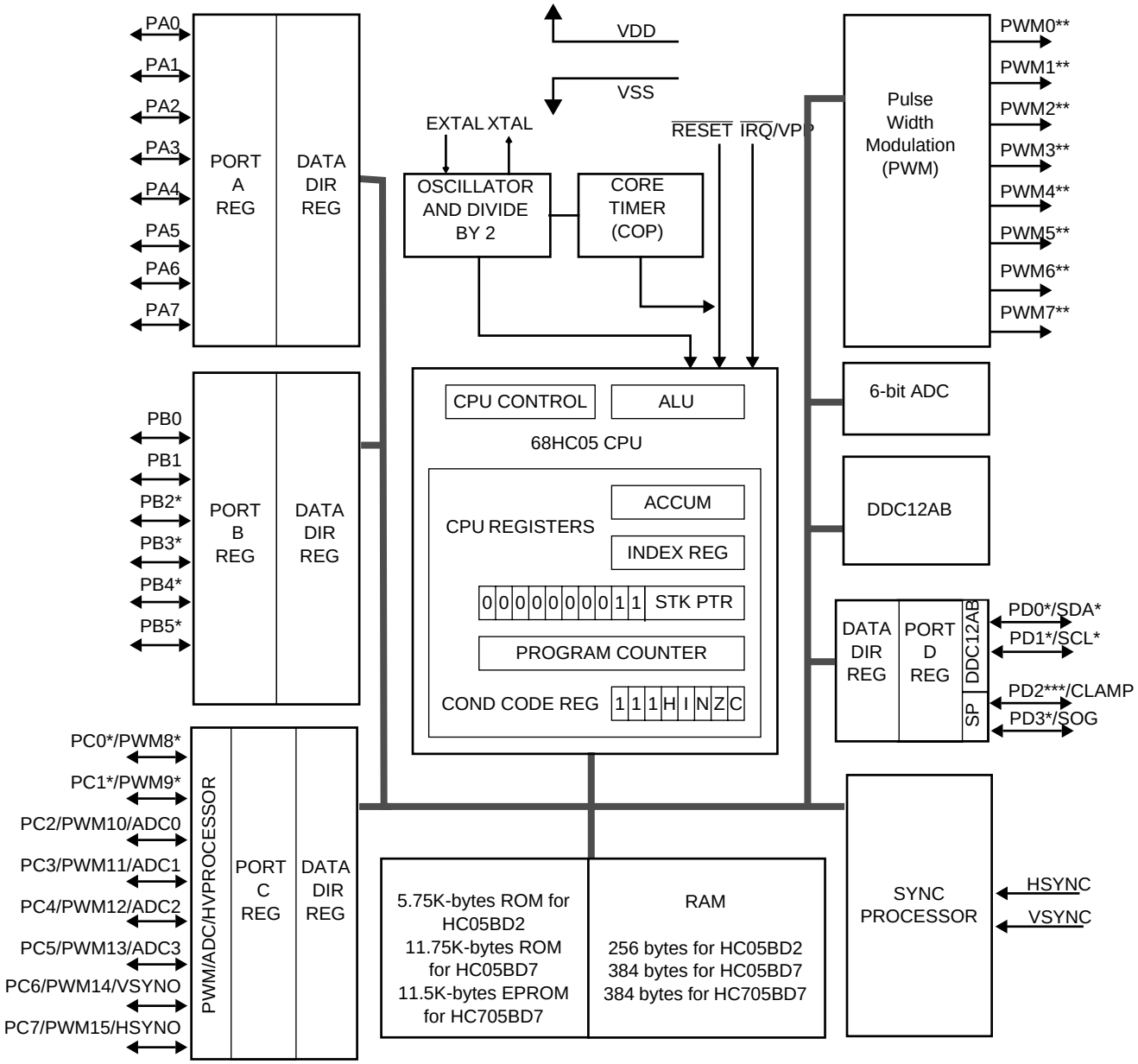
†DDC is a standard defined by VESA.

††I^2C-bus is a proprietary Philips interface bus.

- COP watchdog Reset
- Power-On Reset
- Power Saving WAIT Mode; STOP Mode not implemented

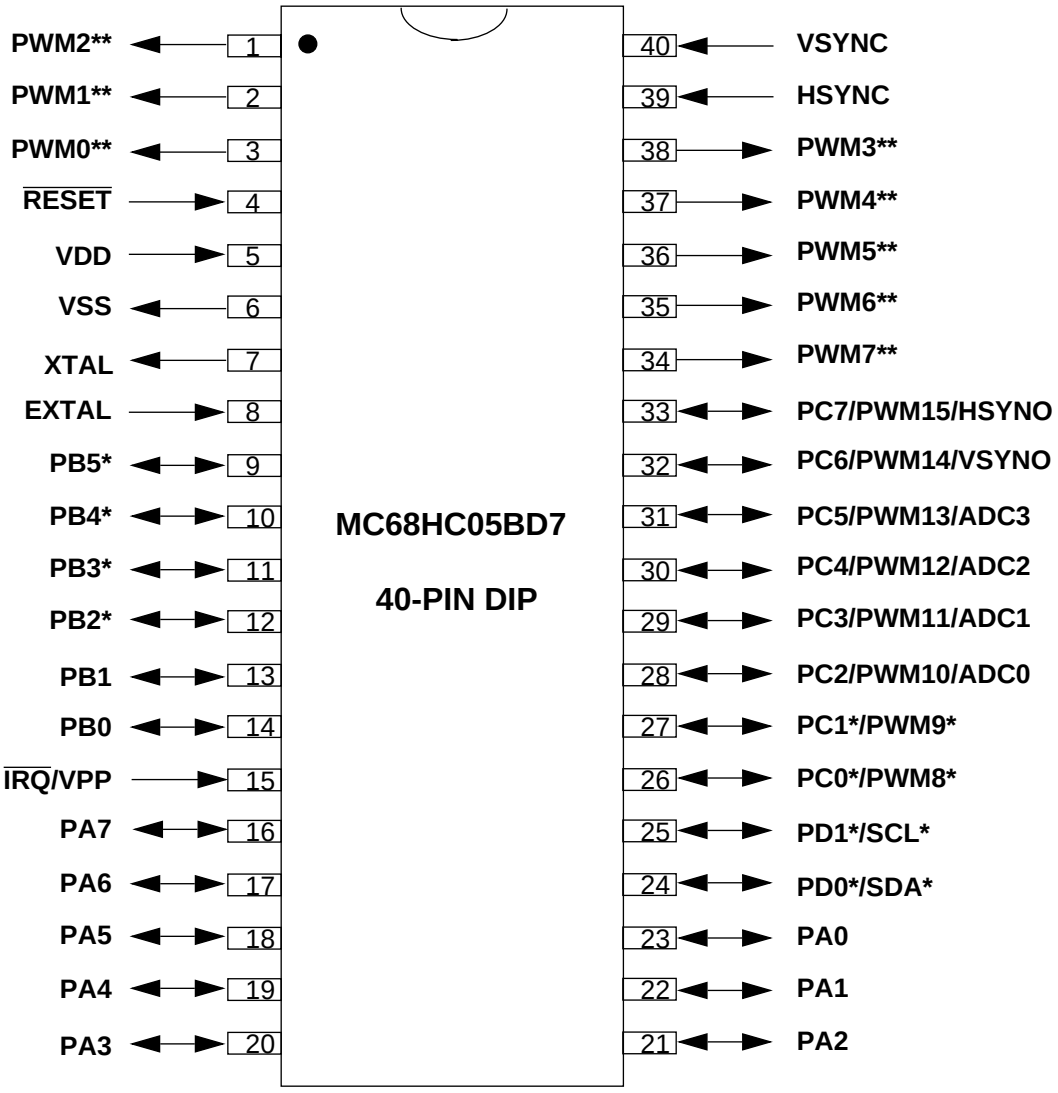
1.1.2 Software Features

- Similar to MC6800
- 8 X 8 unsigned multiply instruction
- Efficient use of program space
- Versatile interrupt handling
- Software programmable external interrupt options
- True bit manipulation
- Addressing modes with indexed addressing for tables
- Efficient instruction set
- Memory mapped I/O
- Upward software compatible with the MC146805 CMOS family



*****: +5V open-drain**
****: +5V open-drain option**
***: +12V open-drain**
IRQ/VPP: VPP valid for HC705 version only, not used for HC05 version

Figure 1-1: MC68HC05BD7 Block Diagram

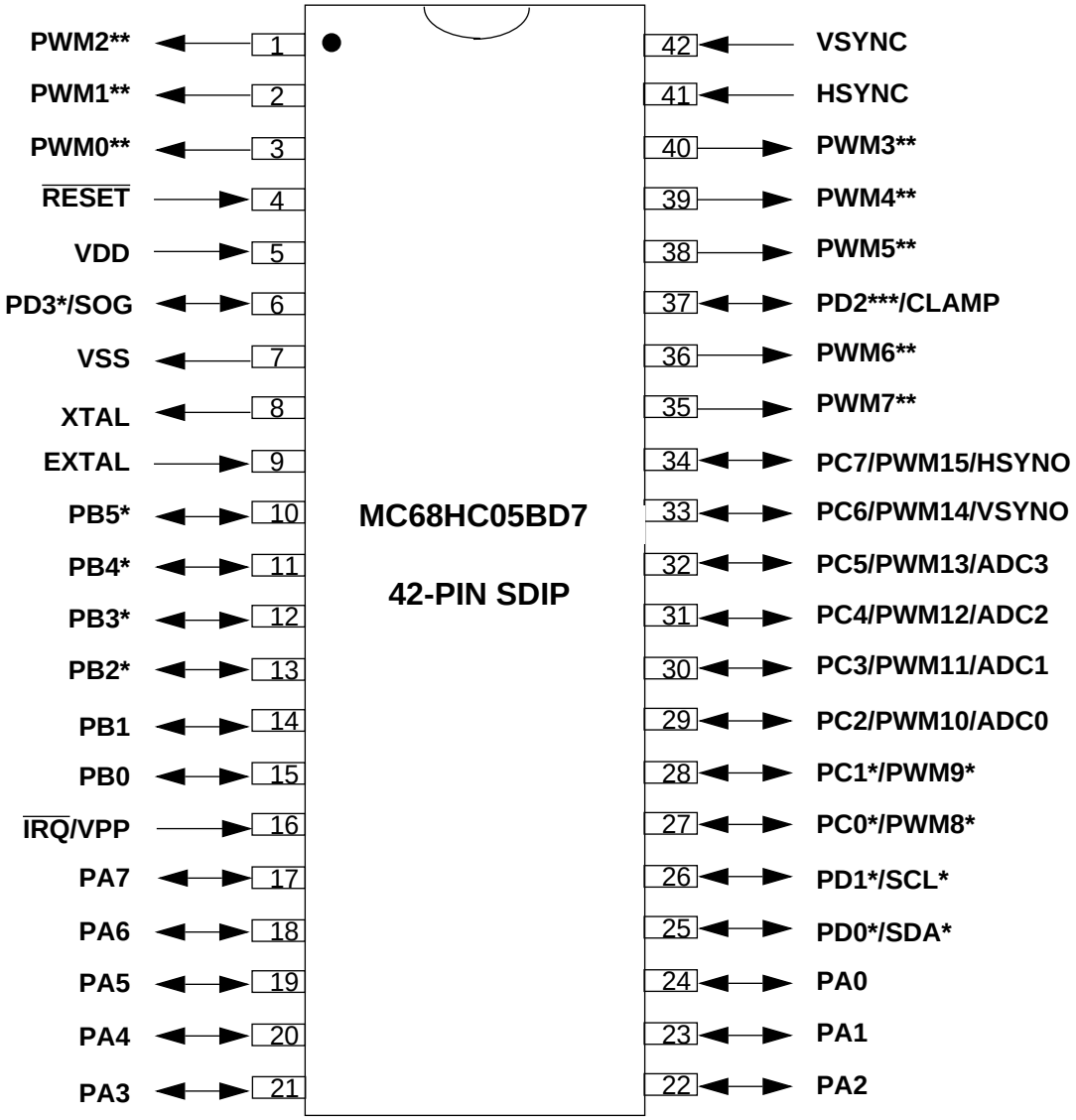


****: +5V open-drain option**

***: +12V open-drain**

IRQ/VPP: VPP valid for HC705 version only, not used for HC05 version

Figure 1-2: MC68HC05BD7/BD2 40-Pin DIP Pin Assignment



***: +5V open-drain option

**: +5V open-drain option

*: +12V open-drain

IRQ/VPP: VPP valid for HC705 version only, not used for HC05 version

Figure 1-3: MC68HC05BD7/BD2 42-Pin SDIP Pin Assignment

1.2 Signal Description

1.2.1 VDD and VSS

VDD is the positive supply pin and VSS is the ground pin.

1.2.2 $\overline{\text{IRQ}}$/VPP

This pin has two functions. While in user mode, this pin serves as $\overline{\text{IRQ}}$, a general purpose interrupt input which is software programmable for two choices of interrupt triggering sensitivity. These options are: 1) negative edge-sensitive triggering only, or 2) both negative edge-sensitive and level-sensitive triggering. In the latter case, either type of input to the $\overline{\text{IRQ}}$ pin will produce the interrupt. This interrupt can be inhibited by setting the INHIRQ bit in the MFT register. While in bootstrap mode, this pin is used as VPP pin for HC705 version. It is used to supply high voltage needed for programming the user EPROM.

1.2.3 EXTAL, XTAL

The EXTAL and XTAL pins are the connections for the on-chip oscillator. The EXTAL, and XTAL pins can accept the following sets of components:

1. A crystal as shown in **Figure 1-4(a)**
2. An external clock signal as shown in **Figure 1-4(b)**

The frequency, f_{OSC}, of the oscillator or external clock source is divided by two to produce the internal operating frequency, f_{OP}.

1.2.3.1 Crystal Oscillator

The circuit in shows **Figure 1-4(a)** a typical oscillator circuit for an AT-cut, parallel resonant crystal. The crystal manufacturer's recommendations should be followed, as the crystal parameters determine the external component values required to provide maximum stability and reliable start-up. The load capacitance values used in the oscillator circuit design should include all stray capacitances. The crystal and components should be mounted as close as possible to the pins for start-up stabilization and to minimize output distortion. An **internal start-up resistor** of approximately **2 MΩ** is provided between EXTAL and XTAL for the crystal type oscillator.

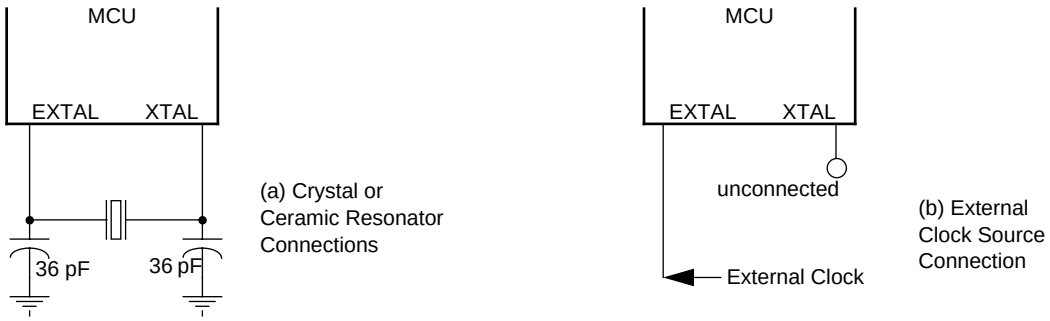


Figure 1-4: Oscillator Connections

1.2.4 $\overline{\text{RESET}}$

This active low input-only pin is used to reset the MCU to a known start-up state. The $\overline{\text{RESET}}$ pin contains an internal Schmitt trigger as part of its input to improve noise immunity. See **SECTION 5** for more details.

1.2.5 PA0-PA7

These eight I/O lines comprise Port A. The state of any pin is software programmable and all Port A lines are configured as inputs during Reset. See **SECTION 7** for a detailed description of I/O programming.

1.2.6 PB0-PB5

These six I/O lines comprise Port B. The state of any pin is software programmable and all Port B lines are configured as inputs during Reset. PB2 to PB5 are +12V open-drain pins. See **SECTION 7** for a detailed description of I/O programming.

1.2.7 PC0*/PWM8*-PC1*/PWM9*

These two +12V open-drain pins are either 8-bit PWM channels 8 to 9 outputs or general purpose I/O port C. The state of any pin is software programmable and all Port C lines are configured as inputs during Reset. See **SECTION 7** for a detailed description of I/O programming.

1.2.8 PC2/PWM10/ADC0- PC5/PWM13/ADC3

These four pins can be selected as general purpose I/O of port C, PWM or ADC input channel 0-2. See **SECTION 7** for how to configure the pins. Also see **SECTION 8** and **SECTION 12** for a detailed description of these modules.

1.2.9 PC6/PWM14/VSYNO, PC7/PWM15/HSYNO

These two pins can be selected as general purpose I/O of port C, PWM or sync signal outputs. See **SECTION 7** for how to configure the pins. Also see **SECTION 8** and **SECTION 10** for a detailed description of these modules.

1.2.10 PD0*/SDA*, PD1*/SCL*

These pins are either general purpose I/O pins of port D or the data line (SDA) and clock line (SCL) of DDC12AB. These two pins are open-drain pins. See **SECTION 7** for how to configure the pins. See **SECTION 9** for a detailed description.

1.2.11 PD2***/CLAMP, PD3*/SOG

The PD2*** is +5V open-drain general purpose I/O pin and the PD3* is +12V open-drain general purpose I/O pin. The PD2 pin could become the CLAMP pulse push-pull output to Pre-AMP IC and the PD3 pin could become the SOG digital input of the Sync Processor when the corresponding enable bit in SPIOCR register is set. These two pins will not be bonded out in 40-pin DIP package.

1.2.12 PWM0**-PWM7**

These pins are dedicated for 8-bit PWM channels 0 to 7, which have +5V open-drain software options. See **SECTION 8** for a detailed description.

1.2.13 HSYNC, VSYNC

These two input pins are for video sync signals input from the host computer. The signals will be used for video mode detection and output to **HSYNO** and **VSYNO**. The host computer can also send a composite sync signal to the **HSYNC** input. This composite signal will be separated internally. The polarity of the input signals can be either positive or negative. These two pins contain internal Schmitt triggers as part of their inputs to improve noise immunity. See **SECTION 10** for a detail description.

1.3 Options

MC68HC05BD7 provides an option for $\overline{\text{IRQ}}$ interrupt edge only sensitivity or edge and level sensitivity and one option register for individual PWM channels 0 to 7 to be programmed as open-drain type output. The IRQ option is selected by setting the appropriate bit in the MFTCSR register at address $0008 and the PWM open-drain option register is located at address $0012.

SECTION 2 MEMORY

The MC68HC05BD7 has a 16K byte memory map, consisting of user ROM/EPROM, RAM, Self-Check/Bootstrap ROM, and I/O as shown in **Figure 2-1**.

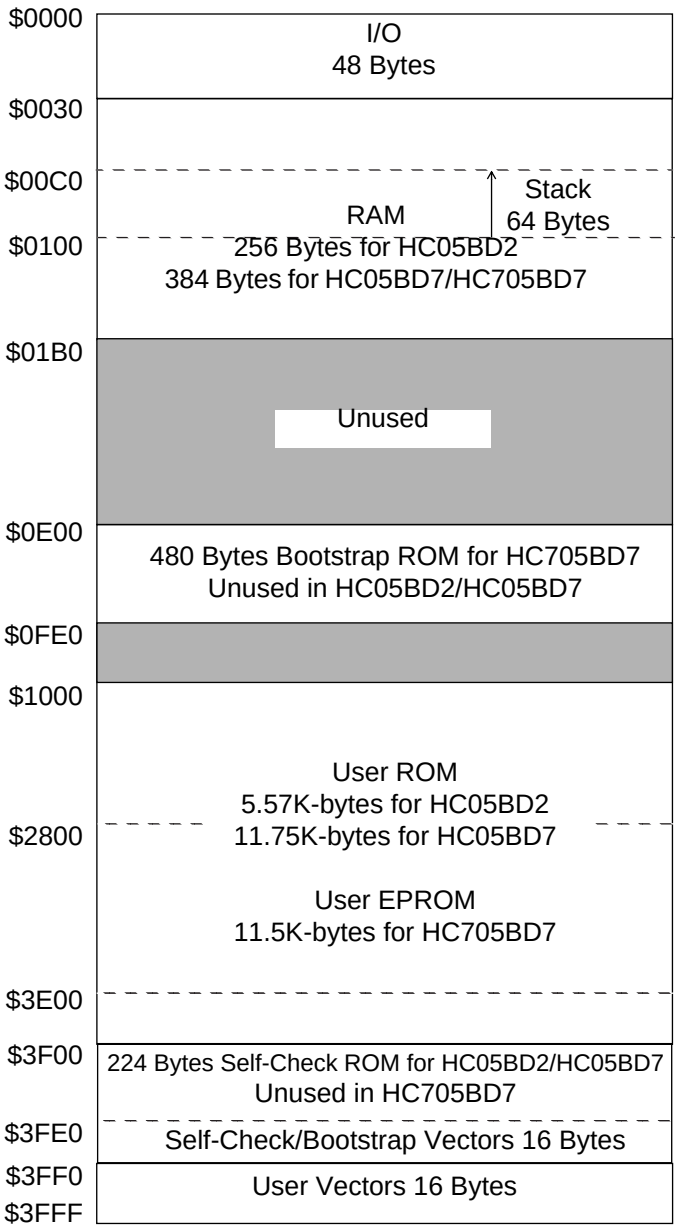


Figure 2-1: The 16K Memory Map of the MC68HC05BD7

ADDR	REGISTER	READ WRITE	7	6	5	4	3	2	1	0
$0000	PORT A DATA PORTA	R	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
		W								
$0001	PORT B DATA PORTB	R			PB5	PB4	PB3	PB2	PB1	PB0
		W								
$0002	PORT C DATA PORTC	R	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
		W								
$0003	PORT D DATA PORTD	R					PD3	PD2	PD1	PD0
		W								
$0004	PORT A DATA DIRECTION DDRA	R	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
		W								
$0005	PORT B DATA DIRECTION DDRB	R			DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
		W								
$0006	PORT C DATA DIRECTION DDRC	R	DDRC7	DDRC6	DDRC5	DDRC4	DDRC3	DDRC2	DDRC1	DDRC0
		W								
$0007	PORT D DATA DIRECTION DDRD	R					DDRD3	DDRD2	DDRD1	DDRD0
		W								
$0008	MFT CTRL/STATUS REG MFTCSR	R	TOF	RTIF	TOFIE	RTIE	IRQN	INHIRQ	RT1	RT0
		W								
$0009	MFT TIMER COUNTER REG MFTCR	R	MFTCR7	MFTCR6	MFTCR5	MFTCR4	MFTCR3	MFTCR2	MFTCR1	MFTCR0
		W								
$000A	CONFIGURATION REG 1 CR1	R	PWM15	PWM14	PWM13	PWM12	PWM11	PWM10	PWM9	PWM8
		W								
$000B	CONFIGURATION REG 2 CR2	R	HSYNO	VSYNO	ADC3	ADC2	ADC1	ADC0	SCL	SDA
		W								
$000C	SP CONTROL & STATUS SPCSR	R	VSIE	VEDGE	VSIF	COMP	VINVO	HINVO	VPOL	HPOL
		W								
$000D	VERT FREQUENCY HIGH REG VFHR	R	VOF	0	0	VF12	VF11	VF10	VF9	VF8
		W								
$000E	VERT FREQUENCY LOW REG VFLR	R	VF7	VF6	VF5	VF4	VF3	VF2	VF1	VF0
		W								
$000F	HOR FREQUENCY HIGH REG HFHR	R	HOVER	HFH6	HFH5	HFH4	HFH3	HFH2	HFH1	HFH0
		W								

UNIMPLEMENTED RESERVED

Figure 2-2: MC68HC05BD7 I/O Register $00-$0F

ADDR	REGISTER	READ / WRITE	7	6	5	4	3	2	1	0
$0010	HOR FREQUENCY LOW REG HFLR	R	0	0	0	HFL4	HFL3	HFL2	HFL1	HFL0
		W								
$0011	SP IO CONTROL REG SPIOCR	R	VSYNCS	HSYNCS	COINV		SOGIN	CLAMP	BPOR	SOUT
		W								
$0012	PWM OPEN-DRAIN OPTION REGISTER	R	7PWMO	6PWMO	5PWMO	4PWMO	3PWMO	2PWMO	1PWMO	0PWMO
		W								
$0013	UNIMPLEMENTED	R								
		W								
$0014	ADC CONTROL/STATUS REG	R	RESULT		AD5	AD4	AD3	AD2	AD1	AD0
		W								
$0015	ADC CHANNEL REGISTER	R							CHSL1	CHSL0
		W								
$0016	DDC MASTER CONTROL REG DMCR	R	ALIF	NAKIF	BB	MAST	MRW	BR2	BR1	BR0
		W								
$0017	DDC ADDRESS REGISTER DADR	R	DAD7	DAD6	DAD5	DAD4	DAD3	DAD2	DAD1	EXTAD
		W								
$0018	DDC CONTROL REGISTER DCR	R	DEN	DIEN			TXAK	SCLIEN	DDC1EN	
		W								
$0019	DDC STATUS REGISTER DSR	R	RXIF	TXIF	MATCH	RW	RXAK	SCLIF	TXBE	RXBF
		W								
$001A	DDC DATA TRANSMIT REG DDTR	R	DTD7	DTD6	DTD5	DTD4	DTD3	DTD2	DTD1	DTD0
		W								
$001B	DDC DATA RECEIVE REG DDRR	R	DRD7	DRD6	DRD5	DRD4	DRD3	DRD2	DRD1	DRD0
		W								
$001C	UNIMPLEMENTED	R								
		W								
$001D	RESERVED FOR EPROM CONTROL PCR	R							ELAT	PGM
		W								
$001E	UNIMPLEMENTED	R								
		W								
$001F	RESERVED	R								
		W								

UNIMPLEMENTED RESERVED

Figure 2-3: MC68HC05BD7 I/O Register $10-$1F

ADDR	REGISTER	READ WRITE	7	6	5	4	3	2	1	0
$0020	PULSE WIDTH MODULATOR 0PWM	R	0PWM4	0PWM3	0PWM2	0PWM1	0PWM0	0BRM2	0BRM1	0BRM0
		W								
$0021	PULSE WIDTH MODULATOR 1PWM	R	1PWM4	1PWM3	1PWM2	1PWM1	1PWM0	1BRM2	1BRM1	1BRM0
		W								
$0022	PULSE WIDTH MODULATOR 2PWM	R	2PWM4	2PWM3	2PWM2	2PWM1	2PWM0	2BRM2	2BRM1	2BRM0
		W								
$0023	PULSE WIDTH MODULATOR 3PWM	R	3PWM4	3PWM3	3PWM2	3PWM1	3PWM0	3BRM2	3BRM1	3BRM0
		W								
$0024	PULSE WIDTH MODULATOR 4PWM	R	4PWM4	4PWM3	4PWM2	4PWM1	4PWM0	4BRM2	4BRM1	4BRM0
		W								
$0025	PULSE WIDTH MODULATOR 5PWM	R	5PWM4	5PWM3	5PWM2	5PWM1	5PWM0	5BRM2	5BRM1	5BRM0
		W								
$0026	PULSE WIDTH MODULATOR 6PWM	R	6PWM4	6PWM3	6PWM2	6PWM1	6PWM0	6BRM2	6BRM1	6BRM0
		W								
$0027	PULSE WIDTH MODULATOR 7PWM	R	7PWM4	7PWM3	7PWM2	7PWM1	7PWM0	7BRM2	7BRM1	7BRM0
		W								
$0028	PULSE WIDTH MODULATOR 8PWM	R	8PWM4	8PWM3	8PWM2	8PWM1	8PWM0	8BRM2	8BRM1	8BRM0
		W								
$0029	PULSE WIDTH MODULATOR 9PWM	R	9PWM4	9PWM3	9PWM2	9PWM1	9PWM0	9BRM2	9BRM1	9BRM0
		W								
$002A	PULSE WIDTH MODULATOR 10PWM	R	10PWM4	10PWM3	10PWM2	10PWM1	10PWM0	10BRM2	10BRM1	10BRM0
		W								
$002B	PULSE WIDTH MODULATOR 11PWM	R	11PWM4	11PWM3	11PWM2	11PWM1	11PWM0	11BRM2	11BRM1	11BRM0
		W								
$002C	PULSE WIDTH MODULATOR 12PWM	R	12PWM4	12PWM3	12PWM2	12PWM1	12PWM0	12BRM2	12BRM1	12BRM0
		W								
$002D	PULSE WIDTH MODULATOR 13PWM	R	13PWM4	13PWM3	13PWM2	13PWM1	13PWM0	13BRM2	13BRM1	13BRM0
		W								
$002E	PULSE WIDTH MODULATOR 14PWM	R	14PWM4	14PWM3	14PWM2	14PWM1	14PWM0	14BRM2	14BRM1	14BRM0
		W								
$002F	PULSE WIDTH MODULATOR 15PWM	R	15PWM4	15PWM3	15PWM2	15PWM1	15PWM0	15BRM2	15BRM1	15BRM0
		W								

Figure 2-4: MC68HC05BD7 I/O Register $20-$2F

2.1 COP

The COP time-out is prevented by writing a ‘0’ to bit 0 of address $3FF0. See **SECTION 11** for detail.

2.2 ROM

For MC68HC05BD7, the user ROM consists of 11.75K bytes of ROM from $1000 through $3EFF and 16 bytes of user vectors from $3FF0 through $3FFF. For MC68HC05BD2, the user ROM consists of 5.75K bytes of ROM from $2800 through $3EFF and 16 bytes of user vectors from $3FF0 through $3FFF. The Self-Check ROM is located from $3F00 through $3FE0 and Self-Check vectors are located from $3FE0 through $3FEF.

2.3 EPROM

For MC68HC705BD7, the user EPROM consists of 11.5K bytes of EPROM from $1000 through $3DFF and 16 bytes of user vectors from $3FF0 through $3FFF. The Bootstrap ROM is located from $0E00 through $0FDF and Bootstrap vectors are located from $3FE0 through $3FEF, at the same location as Self-Check vectors.

2.4 RAM

The user RAM consists of 384 bytes from $0030 to $01AF for HC05BD7/HC705BD7. User RAM consists of 256 bytes from $30 to $12F for HC05BD2. The stack pointer can access 64 bytes of RAM from $00FF to $00C0. See **Section 3.1.3, Stack Pointer (SP)**.

NOTE: Using the stack area for data storage or temporary work locations requires care to prevent it from being overwritten due to stacking from an interrupt or subroutine call.

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SECTION 3 CPU CORE

The MC68HC05BD7 has a 16K memory map. Therefore it uses only the lower 14 bits of the address bus. In the following discussion the upper 2 bits of the address bus can be ignored. The stack has only 64 bytes. Therefore, the stack pointer has been reduced to only 6 bits and will only decrement down to $00C0 and then wrap-around to $00FF. All other instructions and registers behave as described in this chapter.

3.1 Registers

The MCU contains five registers which are hard-wired within the CPU and are not part of the memory map. These five registers are shown in **Figure 3-1** and are described in the following paragraphs.

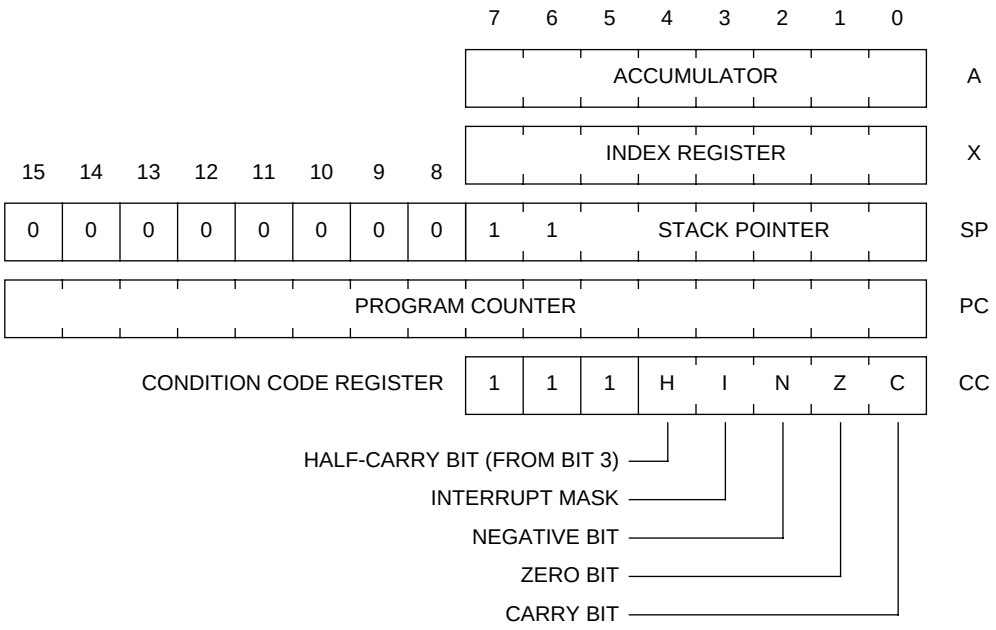

Figure 3-1: MC68HC05 Programming Model

3.1.1 Accumulator (A)

The accumulator is a general purpose 8-bit register as shown in **Figure 3-1**. The CPU uses the accumulator to hold operands and results of arithmetic calculations or non-arithmetic operations. The accumulator is not affected by a reset of the device.

3.1.2 Index Register (X)

The index register shown in **Figure 3-1** is an 8-bit register that can perform two functions:

- Indexed addressing
- Temporary storage

In indexed addressing with no offset, the index register contains the low byte of the operand address, and the high byte is assumed to be $00. In indexed addressing with an 8-bit offset, the CPU finds the operand address by adding the index register content to an 8-bit immediate value. In indexed addressing with a 16-bit offset, the CPU finds the operand address by adding the index register content to a 16-bit immediate value.

The index register can also serve as an auxiliary accumulator for temporary storage. The index register is not affected by a reset of the device.

3.1.3 Stack Pointer (SP)

The stack pointer shown in **Figure 3-1** is a 16-bit register. In MCU devices with memory space less than 64K bytes the unimplemented upper address lines are ignored. The stack pointer contains the address of the next free location on the stack. During a reset or the reset stack pointer (RSP) instruction, the stack pointer is set to $00FF. The stack pointer is then decremented as data is pushed onto the stack and incremented as data is pulled off the stack.

When accessing memory, the ten most significant bits are permanently set to 0000000011. The six least significant register bits are appended to these ten fixed bits to produce an address within the range of $00FF to $00C0. Subroutines and interrupts may use up to 64 ($40) locations. If 64 locations are exceeded, the stack pointer wraps around and overwrites the previously stored information. A subroutine call occupies two locations on the stack and an interrupt uses five locations.

3.1.4 Program Counter (PC)

The program counter shown in **Figure 3-1** is a 16-bit register. In MCU devices with memory space less than 64K bytes the unimplemented upper address lines are ignored. The program counter contains the address of the next instruction or operand to be fetched.

Normally, the address in the program counter increments to the next sequential memory location every time an instruction or operand is fetched. Jump, branch, and interrupt operations load the program counter with an address other than that of the next sequential location.

3.1.5 Condition Code Register (CCR)

The CCR shown in **Figure 3-1** is a 5-bit register in which four bits are used to indicate the results of the instruction just executed. The fifth bit is the interrupt mask. These bits can be individually tested by a program, and specific actions can be taken as a result of their states. The condition code register should be thought of as having three additional upper bits that are always ones. Only the interrupt mask is affected by a reset of the device. The following paragraphs explain the functions of the lower five bits of the condition code register.

3.1.5.1 Half Carry Bit (H-Bit)

When the half-carry bit is set, it means that a carry occurred between bits 3 and 4 of the accumulator during the last ADD or ADC (add with carry) operation. The half-carry bit is required for binary-coded decimal (BCD) arithmetic operations.

3.1.5.2 Interrupt Mask (I-Bit)

When the interrupt mask is set, the internal and external interrupts are disabled. Interrupts are enabled when the interrupt mask is cleared. When an interrupt occurs, the interrupt mask is automatically set after the CPU registers are saved on the stack, but before the interrupt vector is fetched. If an interrupt request occurs while the interrupt mask is set, the interrupt request is latched. Normally, the interrupt is processed as soon as the interrupt mask is cleared.

A return from interrupt (RTI) instruction pulls the CPU registers from the stack, restoring the interrupt mask to its state before the interrupt was encountered. After any reset, the interrupt mask is set and can only be cleared by the Clear I-Bit (CLI), or WAIT instructions.

3.1.5.3 Negative Bit (N-Bit)

The negative bit is set when the result of the last arithmetic operation, logical operation, or data manipulation was negative. (Bit 7 of the result was a logical one.)

The negative bit can also be used to check an often tested flag by assigning the flag to bit 7 of a register or memory location. Loading the accumulator with the contents of that register or location then sets or clears the negative bit according to the state of the flag.

3.1.5.4 Zero Bit (Z-Bit)

The zero bit is set when the result of the last arithmetic operation, logical operation, data manipulation, or data load operation was zero.

3.1.5.5 Carry/Borrow Bit (C-Bit)

The carry/borrow bit is set when a carry out of bit 7 of the accumulator occurred during the last arithmetic operation, logical operation, or data manipulation. The carry/borrow bit is also set or cleared during bit test and branch instructions and during shifts and rotates. This bit is neither set by an INC nor by a DEC instruction.

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SECTION 4 INTERRUPTS

4.1 CPU Interrupt Processing

Interrupts cause the processor to save register contents on the stack and to set the interrupt mask (I-bit) to prevent additional interrupts. Unlike RESET, hardware interrupts do not cause the current instruction execution to be halted, but are considered pending until the current instruction is complete.

If interrupts are not masked (I-bit in the CCR is cleared) and the corresponding interrupt enable bit is set the processor will proceed with interrupt processing. Otherwise, the next instruction is fetched and executed. If an interrupt occurs the processor completes the current instruction, then stacks the current CPU register states, sets the I-bit to inhibit further interrupts, and finally checks the pending hardware interrupts. If more than one interrupt is pending following the stacking operation, the interrupt with the highest vector location shown in **Table 4-1** will be serviced first. The SWI is executed the same as any other instruction, regardless of the I-bit state.

When an interrupt is to be processed the CPU fetches the address of the appropriate interrupt software service routine from the vector table at locations $3FF0 thru $3FFF as defined in **Table 4-1**.

Table 4-1: Vector Address for Interrupts and Reset

Register	Flag	Interrupts	CPU Int	Vector Adds.
N/A	N/A	Reset	RESET	$3FFE-$3FFF
N/A	N/A	Software	SWI	$3FFC-$3FFD
N/A	N/A	External Interrupt	IRQ	$3FFA-$3FFB
SPCSR	VSIF	VSINT	SP	$3FF8-$3FF9
DMCR DSR	TXIF RXIF ALIF NAKIF SCLIF	DDC12AB interrupt	DDC12AB	$3FF6-$3FF7
MFTCSR	TOF RTIF	Timer Overflow Real Time Interrupt	MFT	$3FF4-$3FF5
N/A	N/A	N/A	N/A	$3FF2-$3FF3
N/A	N/A	N/A	N/A	$3FF0-$3FF1

An RTI instruction is used to signify when the interrupt software service routine is completed. The RTI instruction causes the register contents to be recovered from the stack and normal processing to resume at the next instruction that was to be executed when the interrupt took place. **Figure 4-1** shows the sequence of events that occur during interrupt processing.

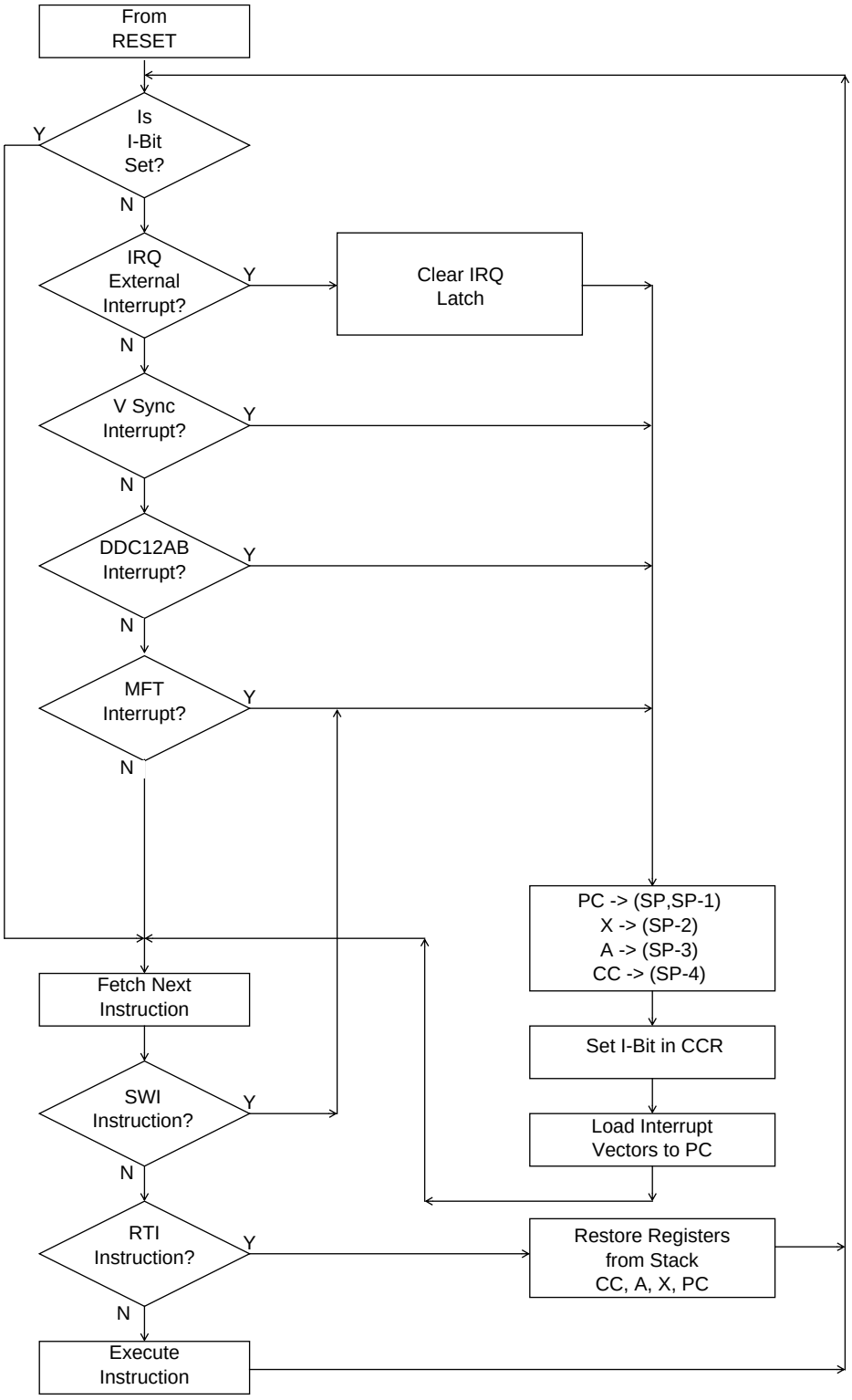

Figure 4-1: Interrupt Processing Flowchart

4.2 Reset Interrupt Sequence

The RESET function is not in the strictest sense an interrupt; however, it is acted upon in a similar manner. A low level input on the $\overline{\text{RESET}}$ pin or an internally generated reset signal causes the program to vector to its starting address which is specified by the contents of $3FFE and $3FFF. The I-bit in the condition code register is also set. The MCU is configured to a known state during this type of reset as described in **SECTION 5**.

4.3 Software Interrupt (SWI)

The SWI is an executable instruction and a non-maskable interrupt since it is executed regardless of the state of the I-bit in the CCR. If the I-bit is zero (interrupts enabled), the SWI instruction executes after interrupts which were pending before the SWI was fetched, or before interrupts generated after the SWI was fetched. The interrupt service routine address is specified by the contents of $3FFC and $3FFD.

4.4 Hardware Interrupts

All hardware interrupts except RESET are maskable by the I-bit in the CCR. If the I-bit is set, all hardware interrupts (internal and external) are disabled. Clearing the I-bit enables the hardware interrupts. There are four types of hardware interrupts which are explained in the following sections.

4.4.1 External Interrupt ($\overline{\text{IRQ}}$)

If the IRQ option is edge and level sensitive triggering (IRQN=0), a low level at the $\overline{\text{IRQ}}$ pin and a cleared interrupt mask bit of the condition code register will cause an EXTERNAL INTERRUPT to occur. If the MCU has finished with the interrupt service routine, but the $\overline{\text{IRQ}}$ pin is still low, the EXTERNAL INTERRUPT will start again. In fact, the MCU will keep on servicing the EXTERNAL INTERRUPT as long as the $\overline{\text{IRQ}}$ pin is low. If the $\overline{\text{IRQ}}$ pin goes low for a while and resumes to high (a negative pulse) before the interrupt mask bit is cleared, the MCU will not recognize there was an interrupt request, and no interrupt will occur after the interrupt mask bit is cleared.

If the IRQ option is negative edge sensitive triggering (IRQN=1), a negative edge occurs at the $\overline{\text{IRQ}}$ pin and a cleared interrupt mask bit of the condition code register will cause an EXTERNAL INTERRUPT to occur. If the MCU has finished with the interrupt service routine, but the $\overline{\text{IRQ}}$ pin has not returned back to high, no further interrupt will be generated. The interrupt logic recognizes negative edge transitions and pulses (special case of negative edges) only. If the negative edge occurs while the interrupt mask bit is set, the interrupt signal will be latched, and interrupt will occur as soon as the interrupt mask bit is cleared. The latch will be cleared by RESET or cleared automatically during fetch of the EXTERNAL INTERRUPT vectors. Therefore, one (and only one) external interrupt edge could be latched while the interrupt mask bit is set. If the INHIRQ bit in the MFT register is set, no IRQ interrupt can be generated.

The service routine address is specified by the contents of $3FFA and $3FFB. **Figure 4-2** shows the two methods for the interrupt line ($\overline{\text{IRQ}}$) to be recognized by the processor. The first method is single pulses on the interrupt line spaced far apart enough to be serviced. The minimum time between pulses is a function of the number of cycles required to execute

the interrupt service routine plus 21 cycles. Once a pulse occurs, the next pulse should not occur until the MCU software has exited the routine (an RTI occurs). The second configuration shows several interrupt line “wire-ANDed” to perform the interrupts at the processor. Thus, if after servicing one interrupt and the interrupt line remains low, then the next interrupt is recognized.

NOTE: IRQN is located at bit 3 of the Multi-function Timer Register at $0008, and is cleared by reset.

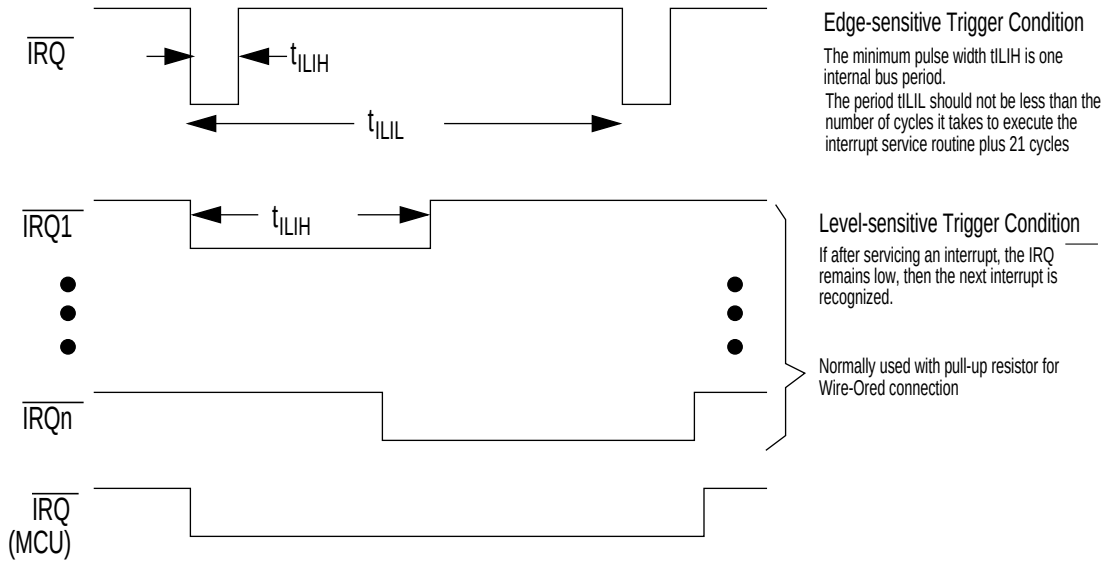

Figure 4-2: External Interrupt

4.4.2 VSYNC Interrupt

The VSYNC interrupt is generated when a specific edge of VSYNC input is detected as described in **SECTION 10**. The interrupt enable bit, VSIE, for the VSYNC interrupt is located at bit 7 of SYNC Processor Control and Status Register (SPCSR) at $000C. The I-bit in the CCR must be cleared in order for the VSYNC interrupt to be enabled. This interrupt will vector to the interrupt service routine located at the address specified by the contents of $3FF8 and $3FF9. The VSYNC Interrupt Flag (VSIF) must be cleared by writing ’0’ to it in the interrupt routine.

4.4.3 DDC12AB Interrupt

The DDC12AB interrupt is generated by the DDC12AB circuit as described in **SECTION 9**. The interrupt enable bit for the DDC12AB interrupt is located at bit 6 of DDC12AB Control Register (DCR) at $0018. The I-bit in the CCR must be cleared in order for the DDC12AB interrupt to be enabled. This interrupt will vector to the interrupt service routine located at the address specified by the contents of $3FF6 and $3FF7.

4.4.4 Multi-Function Timer Interrupt (MFT)

There are two different Multi-Function Timer (MFT) interrupt flags that will cause an interrupt whenever they are set and enabled. The interrupt flags and enable bits are located in the MFT Control and Status Register. Either of these interrupts will vector to the same interrupt service routine, located at the address specified by the contents of $3FF4 and $3FF5. See **Section SECTION 11, MULTI-FUNCTION TIMER** for more informations on MFT interrupts.

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SECTION 5 RESETS

The MCU can be reset from four sources—1 external and 3 internal:

- External $\overline{\text{RESET}}$ pin
- Power-On-Reset (POR)
- Computer Operating Properly Watchdog Reset (COPR)
- Illegal Address Reset (ILADR)

5.1 External Reset ($\overline{\text{RESET}}$)

The $\overline{\text{RESET}}$ pin is the only external reset source. This pin is connected to a Schmitt trigger input gate to provide an upper and lower threshold voltage separated by a minimum amount of hysteresis. This external reset occurs whenever the $\overline{\text{RESET}}$ pin is pulled below the lower threshold and remains in reset until the $\overline{\text{RESET}}$ pin rises above the upper threshold. This active low input will generate the RST signal and reset the CPU and peripherals. Termination of the external $\overline{\text{RESET}}$ input can alter the operating mode of the MCU.

NOTE: Activation of the RST signal is generally referred to as reset of the device, unless otherwise specified.

5.2 Internal Resets

The three internally generated resets are the initial power-on reset, the COP Watchdog Timer reset, and the illegal address reset

5.2.1 Power-On Reset (POR)

The internal POR is generated on power-up to allow the clock oscillator to stabilize. The POR is strictly for power-on condition and is not able to detect a drop in the power supply voltage (brown-out). There is an oscillator stabilization delay of 4065 internal processor bus clock cycles (PH2) after the oscillator becomes active.

The POR will generate the RST signal which will reset the CPU. If any other reset function is active at the end of this 4065 cycles delay, the RST signal will remain in the reset condition until the other reset condition(s) end.

5.2.2 Computer Operating Properly Reset (COPR)

The internal COPR reset is generated automatically (if enabled) by a time-out of the COP Watchdog Timer. This time-out occurs if the counter in the COP Watchdog Timer is not reset (cleared) within a specific time by a program reset sequence. Refer to **SECTION 11** for more information on this time-out feature.

5.2.3 Illegal Address (ILADR) Reset

The MCU monitors all opcode fetches. If an illegal address is accessed during an opcode fetch, an internal reset is generated. Illegal address space consists of all unused locations within the memory space and the I/O registers. (See **Figure 2-1 : The 16K Memory Map of the MC68HC05BD7**.) Because the internal reset signal is used, the MCU comes out of an ILADR Reset in the same operating mode it was in when the opcode was fetched. The ILADR Reset is disabled in Test (Non User) Mode.

SECTION 6 OPERATING MODES

The HC05BD7/HC05BD2 has the following operating modes: single-chip mode (SCM) and self-check mode.

The HC705BD7 has the following operating modes: User mode and bootstrap mode.

6.1 User Mode

In this mode, all address and data bus activity occurs within the MCU so no external pins are required for these functions.

6.2 SELF-CHECK MODE

In this mode, the reset vector is fetched from the 240-byte internal self-check ROM at $3F00:$3FEF. The self-check ROM contains a self-check program to test the functions of internal modules.

6.3 Bootstrap Mode

In this mode, the reset vector is fetched from the 480-byte internal bootstrap ROM at $0E00:$0FDF. The bootstrap ROM contains a small program which reads a program into internal RAM and then passes control to execute EPROM programming.

6.4 Mode Entry

The mode entry is done at the rising edge of the $\overline{\text{RESET}}$ pin. Once the device enters one of the operating modes, the mode can only be changed by an external reset.

At the rising edge of the $\overline{\text{RESET}}$ pin, the device latches the states of $\overline{\text{IRQ}}$ and PB5 pins and places itself in the specified mode. While the $\overline{\text{RESET}}$ pin is low, all pins are configured as Single Chip Mode. The following table shows the states of $\overline{\text{IRQ}}$ and PB5 pins for each mode entry.

Table 6-1: Mode Select Summary

MODE	$\overline{\text{RESET}}$	$\overline{\text{IRQ}}$	PB5
USER MODE		L or H	X
SELF CHECK/BOOTSTRAP		V_{TST}	H

V_{TST} = 1.8 x VDD

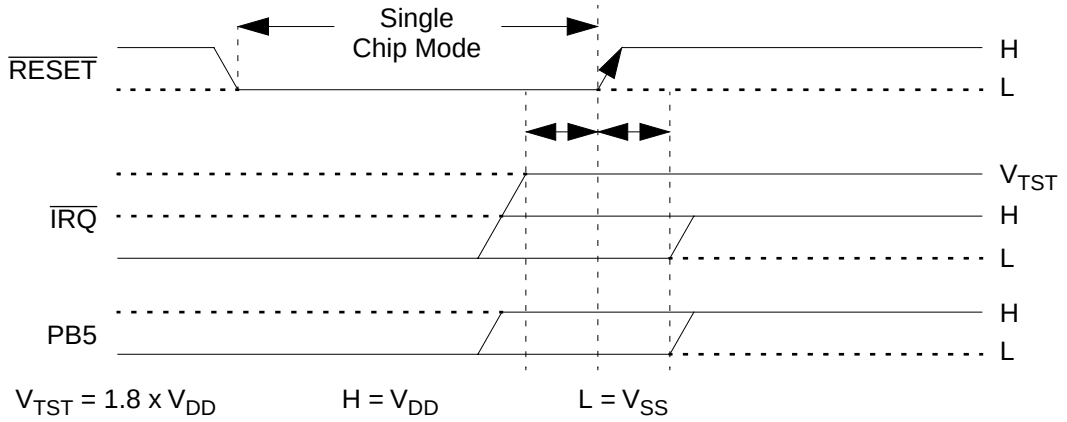


Figure 6-1: Mode Entry Diagram

6.5 EPROM Programming

The 11.5K bytes of USER EPROM is positioned at $1000 through $3DFF with the vector space from $3FF0 to $3FFF. The erased state of EPROM is read as $FF and EPROM power is supplied from VPP and VDD pins.

The Programming Control Register (PCR) is provided for the EPROM programming. The function of EPROM depends on the device operating mode.

In the User Mode, ELAT and PGM bits in the PCR are available for the user read/write and the remaining test bits become read only bits.

Please contact Motorola for Programming boards availability.

6.5.1 Programming Sequence

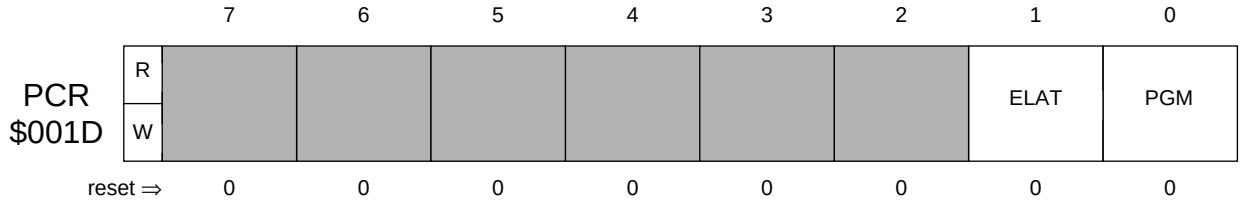
The EPROM programming is as follows:

- Set the ELAT bit
- Write the data to the address to be programmed
- Set the PGM bit
- Delay for the appropriate amount of time
- Clear the PGM and the ELAT bit

The last item may be done on a single CPU write. It is important to remember that an external programming voltage must be applied to the VPP pin while programming, but it should remain between VDD and VSS during normal operation.

6.5.2 Programming Control Register (PCR)

Program control register is provided for EPROM programming the device.



ELAT—EPROM Latch Control

0 - EPROM address and data bus configured for normal read.

1 - EPROM address and data bus configured for programming (writes to EPROM cause address and data to be latched). EPROM is in programming mode and can not be read. This bit is not writable to 1 when no VPP voltage is applied to the VPP pin.

PGM—EPROM Program Command

0 - Programming power to EPROM array is switched off.

1 - Programming power to EPROM array is switched on.

6.6 Low Power Modes

The MC68HC05BD7 has ONLY ONE low-power operational mode. The WAIT instruction provides the only mode that reduces the power required for the MCU by stopping CPU internal clock. The WAIT instruction is not normally used if the COP Watchdog Timer is enabled. **The STOP instruction is not implemented in its normal sense**. The STOP instruction will be interpreted as the NOP instruction by the CPU if it is ever encountered. The flow of the WAIT mode is shown in **Figure 6-2**.

6.6.1 STOP Instruction

Since the execution of a normal STOP instruction results in the stoppage of clocks to all modules, including the COP Watchdog Timer, this instruction is hence not implemented in its usual way to make COP Watchdog Timer meaningful in monitor applications. Execution of the STOP instruction will be the same as that of the NOP instruction. Hence, I bit in the Condition Code Register will not be cleared.

6.6.2 WAIT Instruction

In the WAIT Mode the internal processor clock is halted, suspending all processor and internal bus activity. Other Internal clocks remain active, permitting interrupts to be generated from the Multi-Function Timer, or a reset to be generated from the COP Watchdog Timer. The Timer may be used to generate a periodic exit from the WAIT Mode. Execution of the WAIT instruction automatically clears the I-bit in the Condition Code Register, so that any hardware interrupt can wake up the MCU. All other registers, memory, and input/output lines remain in their previous states.

6.7 COP Watchdog Timer Considerations

The COP Watchdog Timer is always enable in MC68HC05BD7. It will reset the MCU when it times out. For a system that must have intentional uses of the WAIT Mode, care must be taken to prevent such situations from happening during normal operations by arranging timely interrupts to reset the COP Watchdog timer.

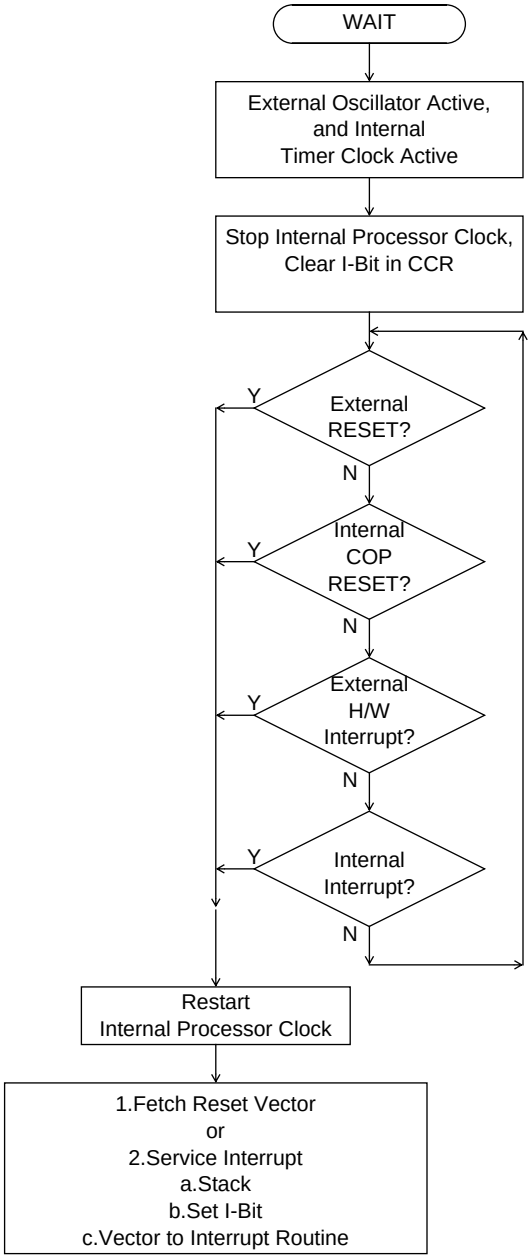


Figure 6-2: WAIT Flowcharts

SECTION 7 INPUT/OUTPUT PORTS

In the User Mode there are 26 bidirectional I/O lines arranged as 4 I/O ports (Port A, B, C, and D). The individual bits in these ports are programmable as either inputs or outputs under software control by the data direction registers (DDRs). Also, if enabled by software, Port C and D will have additional functions as PWM outputs, DDC I/O and Sync Signal Processor outputs.

7.1 Port A

Port A is an 8-bit bidirectional port which does not share any of its pins with other subsystems. The Port A data register is at $00 and the data direction register (DDR) is at $04. Reset does not affect the data register, yet clears the data direction register, thereby returning the ports to inputs. Writing a one to a DDR bit sets the corresponding port bit to output mode.

7.2 Port B

Port B is a 6-bit bidirectional port which does not share any of its pins with other subsystems. PB2 to PB5 are +12V open-drain port pins. The Port B data register is at $01 and the data direction register (DDR) is at $05. Reset does not affect the data register, yet clears the data direction register, thereby returning the ports to inputs. Writing a one to a DDR bit sets the corresponding port bit to output mode.

7.3 Port C

Port C is an 8-bit bidirectional port which shares pins with PWM, Sync Processor, and ADC subsystem. See **SECTION 8** for a detailed description of PWM, **SECTION 10** for a detailed description of SYNC Processor, and **SECTION 12** for a detailed description of ADC. These pins are configured as PWM outputs when the corresponding bits in the CONFIGURATION REGISTER 1 are set. PC6 and PC7 are configured to VSYNO and HSYNO outputs when the corresponding bits in the CONFIGURATION REGISTER 2 are set. And PC2 to PC5 are configured as ADC input channels as the corresponding bit in the CONFIGURATION REGISTER 2 are set. If there is any confliction between the two configuration registers, the CONFIGURATION REGISTER 2 has higher priority. The Port C data register is at $02 and the data direction register (DDR) is at $06. Reset does not affect the data register, but clears the data direction register, thereby returning the ports to inputs. Writing a one to a DDR bit sets the corresponding port to output mode.

7.4 Port D

Port D is a 4-bit bidirectional port. PD0 and PD1 shares their pins with DDC12AB subsystem. See **SECTION 9** for a detailed description of DDC12AB. These two pins are configured to the corresponding functions when the corresponding bits in the CONFIGURATION REGISTER 2 are set. They have open-drain output and hysteresis input level to improve noise immunity. PD2 is a +5V open-drain general I/O pin which

shares its pin with the CLAMP output. See **SECTION 10** for the description of CLAMP signal. It becomes the CLAMP output when the CLAMP bit in SPIOCR register is set. PD3 is a +12V open-drain I/O pin which shares its pin with the SOG input. Also see **SECTION 10** for the description of SOG input. It is configured as SOG input when the SOG bit in SPIOCR register is set. The Port D data register is at $03 and the data direction register (DDR) is at $07. Reset does not affect the data register, yet clears the data direction register, thereby returning the ports to inputs. Writing a one to a DDR bit sets the corresponding port bit to output mode.

7.5 Input/Output Programming

Bidirectional port lines may be programmed as an input or an output under software control. The direction of the pins is determined by the state of the corresponding bit in the port data direction register (DDR). Each port has an associated DDR. Any I/O port pin is configured as an output if its corresponding DDR bit is set. A pin is configured as an input if its corresponding DDR bit is cleared.

During Reset, all DDRs are cleared, which configure all port pins as inputs. The data direction registers are capable of being written to or read by the processor. During the programmed output state, a read of the data register actually reads the value of the output data latch and not the I/O pin. See **Figure 7-1** and .

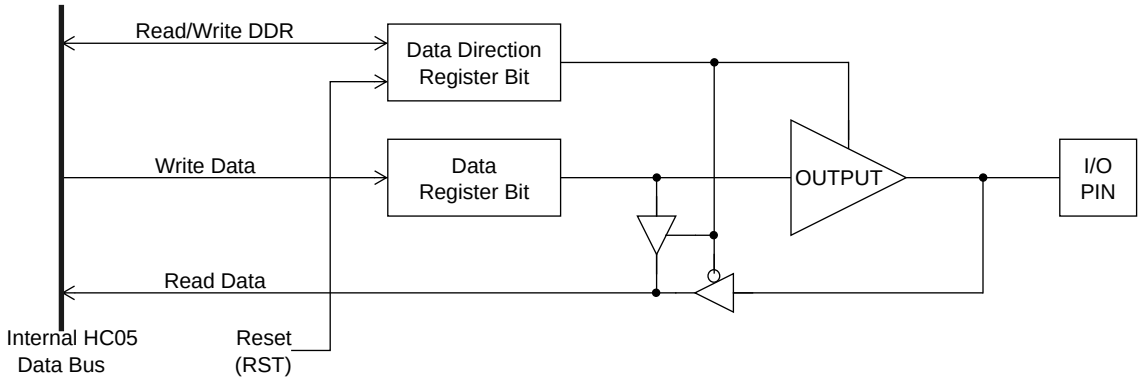


Figure 7-1: Port I/O Circuitry

Table 7-1: I/O Pin Functions

R/$\overline{W}$	DDR	I/O Pin Functions
0	0	The I/O pin is in input mode. Data is written into the output data latch.
0	1	Data is written into the output data latch and output to the I/O pin.
1	0	The state of the I/O pin is read.
1	1	The I/O pin is in output mode. The output data latch is read.

NOTE: A “glitch” can be generated on an I/O pin when changing it from an input to an output unless the data register is first pre-conditioned to the desired state before changing the corresponding DDR bit from a zero to a one.

7.6 Port C and D Configuration Register

Port C and Port D are shared with PWM, ADC, DDC12AB, and SYNC Processor. The configuration registers at $0A and $0B are used to configure those I/O pins. They are default to zero after poWer-on reset. Setting these bits will set the corresponding pins to the corresponding functions. For example, setting SCL and SDA bits of register $0B will configure Port D pins 1 and 0 as DDC12AB pins, regardless of DDR1 and DDR0 settings.

		7	6	5	4	3	2	1	0
CR1 $000A	R	PWM15	PWM14	PWM13	PWM12	PWM11	PWM10	PWM9	PWM8
	W								
reset ⇒		0	0	0	0	0	0	0	0

		7	6	5	4	3	2	1	0
CR2 $000B	R	HSYNO	VSYNO	ADC3	ADC2	ADC1	ADC0	SCL	SDA
	W								
reset ⇒		0	0	0	0	0	0	0	0

When any PWM8-PWM15 bits of CR1 register are set, the corresponding pins of port C become the PWM output if the corresponding bits in CR2 register are clear. When the pin is defined as PWM channel, it become an output only pin. When any ADC3-ADC0 bits of the CR2 register are set, the corresponding pins of port C become the ADC input channels. When HSYNO or VSYNO is set, the PC2 or PC3 becomes the output of HSYNC or VSYNC accordingly, see **SECTION 10** for the detail description of HSYNO and VSYNO outputs. When SCL and SDA bits of the CR2 register are set, the DDC12AB use these two pins as clock and data pins. In summary, the configuration in the CR2 register has higher priority than in the CR1 register.

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SECTION 8 PULSE WIDTH MODULATION

There are 16 PWM channels. Channel 0 to channel 7 are dedicated PWM channels with 5V open-drain option. Channel 8 to channel 15 are shared with ports C under the control of the corresponding configuration register. The channel 8 and channel 9 are 12V open-drain outputs.

8.1 Operation of 8-Bit PWM

Each 8-Bit PWM channel is composed of an 8-bit register which contains a 5-bit PWM in MSB portion and a 3-bit binary rate multiplier (BRM) in LSB portion. There are 16 data registers as shown in **Figure 8-1** located from $20 to $2F. The value programmed in the 5-bit PWM portion will determine the pulse length of the output. The clock to the 5-bit PWM portion is the MCU clock and the repetition rate of the output is hence 62.5 KHz at 2 MHz MCU clock.

The 3-bit BRM will generate a number of narrow pulses which are equally distributed among an 8-PWM-cycle frame. The number of pulses generated is equal to the number programmed in the 3-bit BRM portion. An example of the waveform is shown in **Figure 8-2**.

Combining the 5-bit PWM together with the 3-bit BRM, the average duty cycle at the output will be (M+N/8)/32, where M is the content of the 5-bit PWM portion, and N is the content of the 3-bit BRM portion. Using this mechanism, a true 8-bit resolution PWM type DAC with reasonably high repetition rate can be obtained.

		7	6	5	4	3	2	1	0
PWMR $20-$2F	R	0PWM4	0PWM3	0PWM2	0PWM1	0PWM0	0BRM2	0BRM1	0BRM0
	W								
reset ⇒		0	0	0	0	0	0	0	0

Figure 8-1: PWM Data Register

The value of each PWM Data Register is continuously compared with the content of an internal counter to determine the state of each PWM channel output pin. Double buffering is not used in this PWM design.

T = 1 MCU Clock Period (0.5 μs if MCU clock = 2 MHz)

N	PWM cycles in which narrow pulses are inserted in an 8-cycle frame
XX1	4
X1X	2, 6
1XX	1, 3, 5, 7

Figure 8-2: Relationship Between 5-Bit PWM and 3-Bit BRM

8.2 Open-Drain Option Register

This PWM Open-Drain option Register contains 8 bits which are programmed to change the output drive of individual PWM channel from channel 0 to channel 7 to be open-drain type. This register is located at $0012

		7	6	5	4	3	2	1	0
PWMOR $12	R	7PWMO	6PWMO	5PWMO	4PWMO	3PWMO	2PWMO	1PWMO	0PWMO
	W								
reset ⇒		0	0	0	0	0	0	0	0

Figure 8-3: PWM Open-Drain Option Register

When any bit in this register is one, the corresponding PWM channel output becomes +5V open-drain type. When the bit is zero, the corresponding PWM channel has push-pull output. All eight bits are clear upon reset.

SECTION 9 DDC12AB INTERFACE

9.1 Introduction

This DDC12AB Interface Module is mainly used for monitor to show its identification information to video controller. It contains DDC1 hardware and a two-wire, bidirectional serial bus which is fully compatible with multi-master IIC bus protocol to support DDC2AB interface. In DDC1 type of communication, the module is in transmit mode. For DDC2AB protocol, the module can be either in transmit mode or in receive mode upon host's commands. When DDC1 hardware is enabled, the loaded data is serially clocked out to SDA line by the rising edge of VSYNC input signal continuously. If DDC2 protocol is selected, the module will act as a standard IIC module, and will response only when it is addressed or in master mode. During DDC1 communication, the falling transition in the SCL line can be detected to interrupt cpu for mode switching.

This module not only can be applied in DDC12AB communication, but also can be used as one typical command reception serial bus for factory setup and alignment purpose. It also provides the flexibility of hooking additional devices to an existing system in future expansion without adding extra hardware.

This DDC12AB module uses the SCL clock line and the SDA data line to communicate with external DDC host or IIC interface. These two pins are shared with PD0 and PD1 port pins. The outputs of SDA and SCL pins are all open-drain type. It means no clamping diode connected between the pin and internal VDD. The maximum data rate typically is 100K bps. The maximum communication length and the number of devices that can be connected are limited by a maximum bus capacitance of 400 pF.

9.2 DDC12AB Features

- DDC1 hardware
- Fully compatible with multi-master IIC Bus standard
- Software controllable acknowledge bit generation
- Interrupt driven byte by byte data transfer
- Calling address identification interrupt
- Auto detection of RW bit and switching of transmit or receive mode accordingly
- Detection of START, repeated START, and STOP signals
- Auto generation of START and STOP condition in master mode
- Arbitration loss detection and No-ACK awareness in master mode
- Master clock generator with 8 selectable baud rates
- Automatic recognition of the received acknowledge bit

9.3 Registers

There are six different registers used in the DDC12AB module and the internal configuration of these registers is discussed in the following paragraphs.

9.3.1 DDC Address Register (DADR)

		7	6	5	4	3	2	1	0
DADR $0017	R	DAD7	DAD6	DAD5	DAD4	DAD3	DAD2	DAD1	EXTAD
	W								
	reset	1	0	1	0	0	0	0	0

DAD7-DAD1 Bit 7-Bit 1 These 7 bits can be the DDC2 interface's own specific slave address in slave mode or the calling address when in master mode. So the program must update it as the calling address while entering the master mode and restore its own slave address after the master mode is quitted. This register is cleared as $A0 upon reset.

EXTAD Bit 0 The EXTAD bit is set to expand the calling address of this module. When it is one, the module will acknowledge the general call address $00 and the address comparison circuit will only compare the 4 MSB bits in the DADR register. For example, the DADR contains $A1, that means EXTAD is enabled and the calling address is $A0, therefore, the module can acknowledge the calling address of $00 and $A0 to $AF. When it is clear, the module will only acknowledge to the specific address which is stored in the DADR register. It is clear upon reset.

9.3.2 DDC Control Register (DCR)

		7	6	5	4	3	2	1	0
DCR $0018	R	DEN	DIEN			TXAK	SCLIEN	DDC1EN	
	W								
	reset ⇒	0	0	X	X	0	0	0	X

The DCR provides five control bits. **DCR** is cleared upon reset.

DEN Bit 7 If the DDC module ENable bit (DEN) is set, the DDC module is enabled. If the DEN is clear, the interface is disabled and all flags will restore its power-on default states. Reset clears this bit.

DIEN Bit 6 If the DDC Interrupt ENable bit (DIEN) is set, the interrupt occurs provided the TXIF or RXIF in the status register is set or the ALIF or NAKIF in the DMCR register is set and the I-bit in the Condition Code Register is cleared. If DIEN is cleared, the interrupt of TXIF, RXIF, ALIF, and NAKIF are all disabled. Reset clears this bit.

TXAK	Bit 3	If the transmit acknowledge enable bit (TXAK) is cleared, an acknowledge signal will be sent out to the bus at the 9th clock bit after receiving 8 data bits. When TXAK is set, no acknowledge signal will be generated at the 9th clock (i.e., acknowledge bit = 1). Reset clears this bit.
SCLIEN	Bit 2	If the SCL Interrupt ENable bit (SCLIEN) is set, the interrupt occurs provided the SCLIF in the status register is set and the I-bit in the Condition Code Register is cleared. If SCLIEN is cleared, the interrupt of SCLIF is disabled. Reset clears this bit.
DDC1EN	Bit 1	When DDC1 protocol ENable (DDC1EN) is set, the VSYNC input will be selected as clock input of DDC module. Its rising edge will continuously clock out the data in the shift register. No calling address comparison is performed. The RW bit in the status register will be fixed to be one. If this bit is clear, the SCLIF bit in the status register is also cleared. Reset clears this bit.

9.3.3 DDC Master Control Register (DMCR)

		7	6	5	4	3	2	1	0
DMCR $0016	R	ALIF	NAKIF	BB	MAST	MRW	BR2	BR1	BR0
	W								
reset ⇒		0	0	0	0	0	0	0	0

The DMCR contains two interrupt flags, one bus status flag, two master mode control bits, and three baudrate select bits.

ALIF	Bit 7	The Arbitration Loss Interrupt Flag is set when software attempt to set MAST but the BB has been set by detecting the start condition on the lines or when the DDC12AB module is transmitting a ’one’ to SDA line but detected a ’zero’ from SDA line in master mode, which is so called arbitration loss. This bit can generate an interrupt request to cpu when the DIEN bit in DCR register is set and I-bit in the Condition Code Register is clear. This bit is cleared by writing ’0’ to it or by reset.
NAKIF	Bit 6	The No AcKnowledge Interrupt Flag is only set in master mode when there is no acknowledge bit detected after one data byte or calling address is transferred. This bit can generate an interrupt request to cpu when the DIEN bit in DCR register is set and I-bit in the Condition Code Register is clear. This bit is cleared by writing ’0’ to it or by reset.
BB	Bit 5	The Bus Busy Flag is set after a start condition is detected, and is reset when a stop condition is detected. This bit can supplement the software in initiating the master mode protocol. Reset clears this bit.

MAST	Bit 4	If the software set the MASTer control bit, the module will generate a start condition to the SDA and SCL lines and send out the calling address which is stored in the DADR register. But if the ALIF flag is set when arbitration loss occurs on the lines, the module will discard the master mode by clearing the MAST bit and release both SDA and SCL lines immediately. This bit can also be cleared by writing zero to it or when the NAKIF is set. When the MAST bit is cleared either by NAKIF set or by software, not by ALIF set, the module will generate the stop condition to the lines after the current byte transmission is done. Reset clears this bit.
MRW	Bit 3	This MRW bit will be transmitted out as the bit 0 of the calling address when the module sets the MAST bit to enter the master mode. It will also determine the transfer direction of the following data bytes. When it is one, the module is in master receive mode. When it is zero, the module is in master transmit mode. Reset clears this bit.
BR2-BR0	Bit 2-Bit 0	The three Baud Rate select bits will select one of eight clock rates as the master clock when the module is in master mode. The serial clock frequency is equal to the CPU clock divided by the divider shown in following table. For the CPU clock will be halted while program executes the WAIT instruction, program must not enter WAIT mode when the DDC12AB module is in Master mode in order not to hang up the communication on the lines. These bits are cleared upon reset.

BR2:BR1:BR0	DIVIDER
0 : 0 : 0	20
0 : 0 : 1	40
0 : 1 : 0	80
0 : 1 : 1	160
1 : 0 : 0	320
1 : 0 : 1	640
1 : 1 : 0	1280
1 : 1 : 1	2560

Table 9-1: Pre-scaler of Master Clock Baudrate

9.3.4 DDC Status Register (DSR)

This status register is readable only. All bits are cleared upon reset except bit 3 (RXAK) and bit 1 (TXBE).

		7	6	5	4	3	2	1	0
DSR $0019	R	RXIF	TXIF	MATCH	SRW	RXAK	SCLIF	TXBE	RXBF
	W								
	reset ⇒	0	0	0	0	1	0	1	0

RXIF Bit 7 The data Receive Interrupt Flag (RXIF) is set after the DDRR is loaded with a newly received data. Once the DDRR is loaded with received data, no more received data can be loaded to the DDRR register. The only way to release the DDRR register for loading next received data is that software reads the data from the DDRR register to clear RXBF flag. This bit is cleared by writing ’0’ to it or when the DEN is disabled.

TXIF Bit 6 The data Transmit Interrupt Flag is set before the data of the DDTR register is downloaded to the shift register. It is software’s responsibility to fill the DDTR register with new data when this bit is set. This bit is cleared by writing ’0’ to it or when the DEN is disabled.

MATCH Bit 5 The MATCH flag is set when the received data in the DDRR register is an calling address which matches with the address or its extended addresses (EXTAD=1) specified in the DADR register.

SRW Bit 4 The Slave RW bit will indicate the data direction of DDC protocol. It is updated after the calling address is received in the DDC2 protocol. When it is one, the master will read the data from DDC module, so the module is in transmit mode. When it is zero, the master will send data to the DDC module, the module is in receive mode. When DDC1EN is set, the SRW bit will be one. The reset state of it is zero.

RXAK Bit 3 If the received acknowledge bit (RXAK) is low, it indicates an acknowledge signal has been received after the completion of 8 data bits transmission on the bus. If RXAK is high, it indicates no acknowledge signal has been detected at the 9th clock. Then the module will release the SDA line for the master to generate ’stop’ or ’repeated start’ condition. It is set upon reset.

SCLIF Bit 2 This SCLIF flag is set by the falling edge of SCL line only when DDC1EN is enabled. This bit is cleared by writing zero to it, clearing DDC1EN bit or when the DEN is disable.

TXBE	Bit 1	The Transmit Buffer Empty (TXBE) flag indicates the status of the DDTR register. When the cpu writes the data into the DDTR register, the TXBE flag will be cleared. And it will be set again after the data of the DDTR register has been loaded to the shift register. It is default to be set when the DEN is disable and will be cleared by writing data to the DDTR register when the DEN is enabled.
RXBF	Bit 0	The Receive Buffer Full (RXBF) flag indicates the status of the DDRR register. When the cpu reads the data from the DDRR register, the RXBF flag will be cleared. And it will be set after the data or matched address is transferred from the shift register to the DDRR register. It is cleared when DEN is disabled or DDRR register is read when DEN is enabled.

9.3.5 DDC Data Transmit Register (DDTR)

		7	6	5	4	3	2	1	0
DDTR $001A	R	DTD7	DTD6	DTD5	DTD4	DTD3	DTD2	DTD1	DTD0
	W								
reset ⇒		1	1	1	1	1	1	1	1

The data written into this register after **DEN** is enabled will be automatically downloaded to the shift register when the module detects the calling address is matched and the bit 0 of the received data is one or when the data in the shift register has been transmitted with received acknowledge bit, **RXAK**=0. So if the program doesn't write the data into the **DDTR** register (**TXBE** is cleared) before the matched calling address is detected, the module will pull down the **SCL** line. If the cpu write a data to the **DDTR** register, then the written data will be downloaded to the shift register immediately and the module will release the SCL line, then the **TXBE is** set again and the **TXIF** flag is set to generate another interrupt request for data. So the cpu may need to write the next data to the **DDTR** register to clear **TXBE** flag and for the auto downloading of data to the shift register after the data in the shift register is transmitted over again with **RXAK**=0. If the master receiver doesn't acknowledge the transmitted data, **RXAK**=1, the module will release the **SDA** line for master to generate 'stop' or 'repeated start' conditions. The data stored in the **DDTR** register will not be downloaded to the shift register until next calling from master (**TXBE** remains unchanged).

9.3.6 DDC Data Receive Register (DDRR)

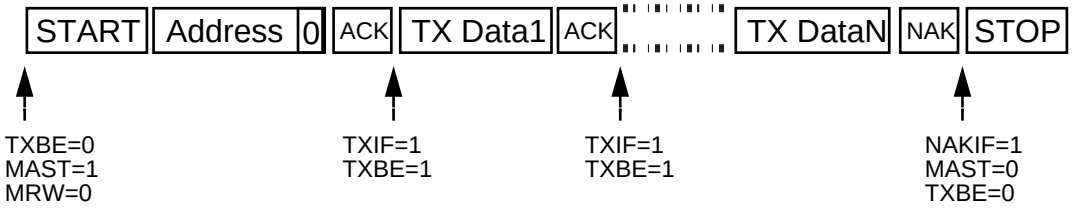
		7	6	5	4	3	2	1	0
DDRR $001B	R	DRD7	DRD6	DRD5	DRD4	DRD3	DRD2	DRD1	DRD0
	W								
reset ⇒		0	0	0	0	0	0	0	0

The **DDC** Data Receive Register (**DDRR**) contains the last received data when the MATCH flag is zero or the calling address from master when the **MATCH** flag is one. The **DDRR** register will be updated after a data byte is received and the **RXBF** is zero. It is a read-only register. The read operation of this register will clear the **RXBF** flag. After the **RXBF** flag is

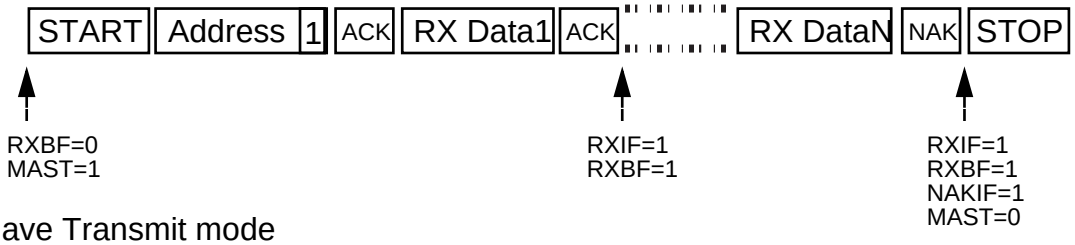
cleared, the register can load the received data again and set the **RXIF** flag to generate interrupt request for reading the newly received data.

9.4 Data Sequence

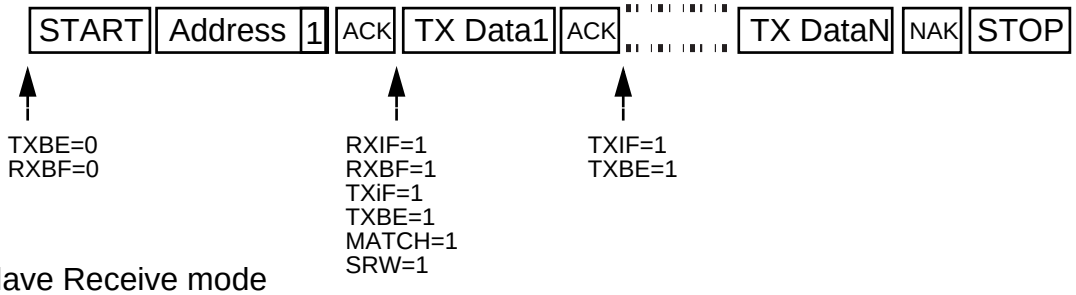
a) Master Transmit mode



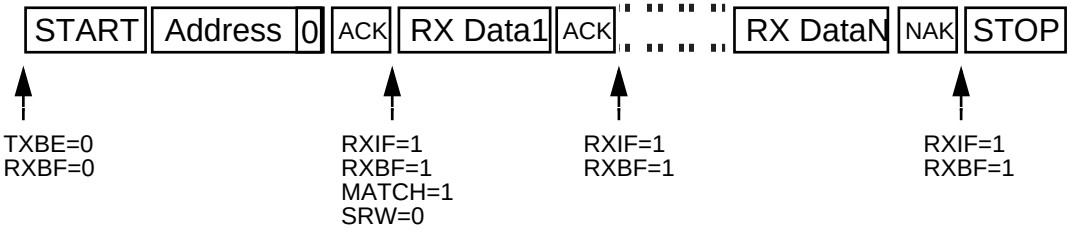
b) Master Receive mode



c) Slave Transmit mode



d) Slave Receive mode



9.5 Program Algorithm

The **Figure 9-1** shows the algorithm of slave mode interrupt routine of DDC12B protocol. The **Figure 9-2** shows the algorithm of master mode setup and interrupt service routine.

When the DDC module detects an arbitration loss in master mode, it will release both SDA and SCL lines immediately. But if there is no further "stop condition" detected, the module will be hanged up. So it is recommended to have time-out software to recover from such ill condition. The software can start the time-out counter by looking at the BB (Bus Busy) in the bit 5 of DMCR and reset the counter when the completion of one byte transmission. If the time-out occurred, program can clear DEN bit to release the bus, and then set DEN bit

and DDC1EN bit to clear BB flag (This is the only way to clear BB flag by software while the module is hanged up due to no "stop condition" received). The program can resume IIC master mode after clearing the BB flag and DDC1EN bit.

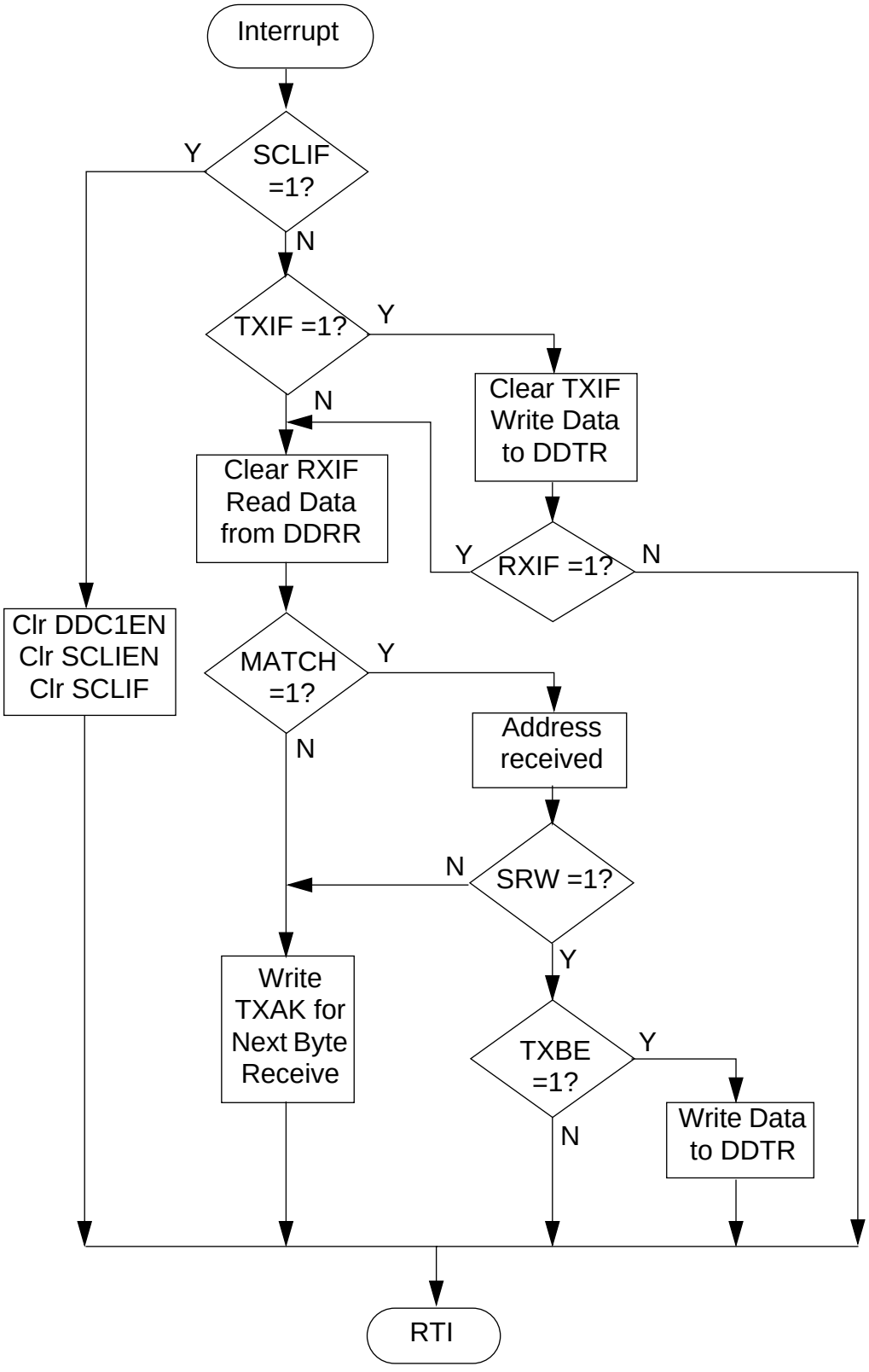
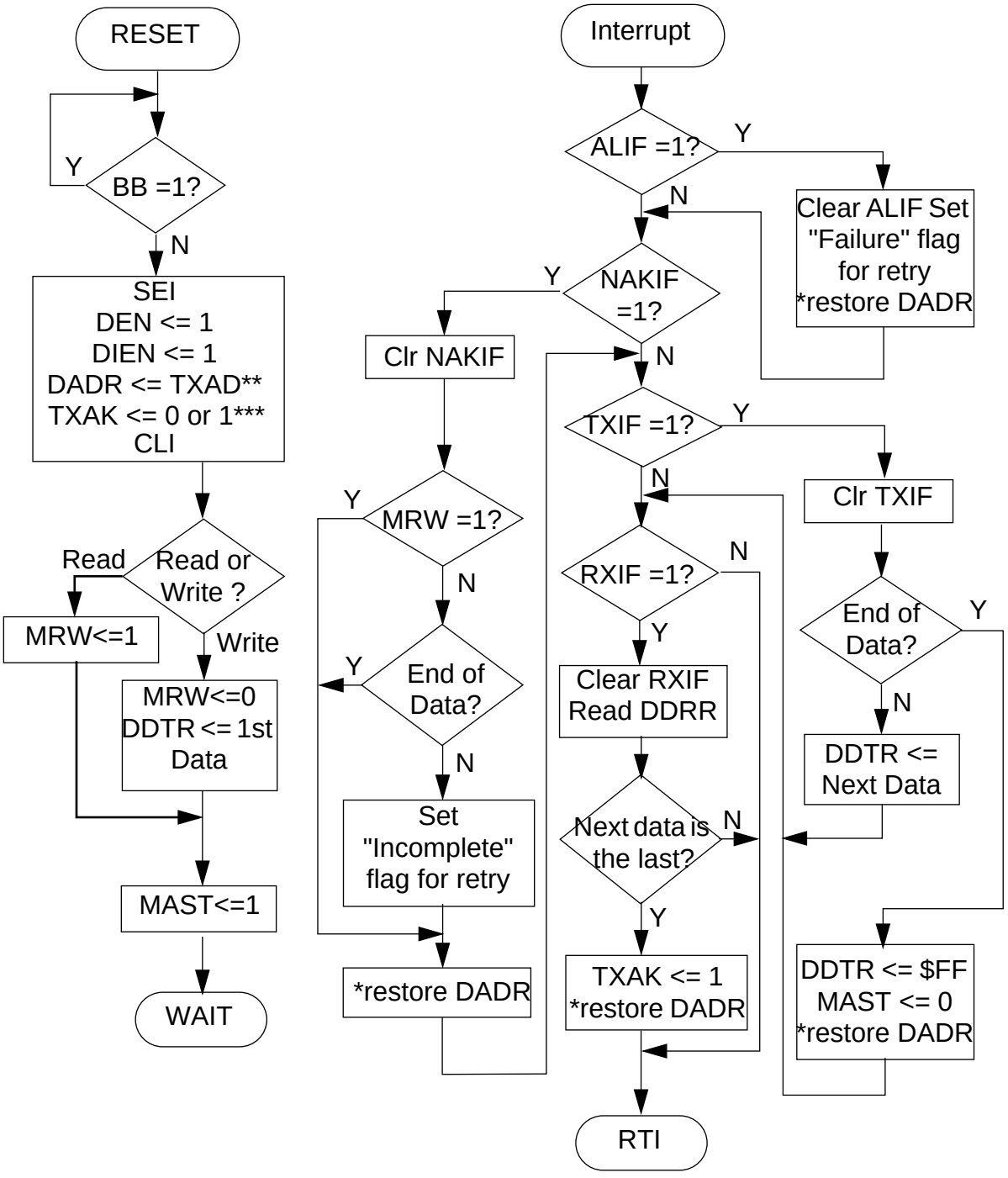


Figure 9-1: Software Flowchart of Slave Mode Interrupt Routine



** TXAD means transmit address

*** TXAK is 1 when master want receive only one byte

(a) Master mode setup

* Restore its own specific slave address

(b) Master mode interrupt routine

Figure 9-2: Software Flowchart in Master mode: (a) Mode setup. (b) Interrupt routine

SECTION 10 SYNC PROCESSOR

10.1 Introduction

The functions of the module include polarity detection, horizontal frequency counter, vertical frequency counter, and polarity controllable **HSYNO** and **VSYNO** outputs of various input sources, such as separate H & V, Composite Sync from **HSYNC**, Sync-On-Green, or internal free running H & V pulses. Besides, it also provides the **CLAMP** pulse output to the external Pre-Amp chip. The **SOGIN** bit in **SPIOCR** register will determine the Composite Sync input pin. All **HSYNC**, **VSYNC**, and **SOG** inputs have internal schmitt trigger to improve noise immunity.

10.2 Functional Blocks

10.2.1 Polarity Detection

The **HSYNC** polarity detection circuit will measure the length of high period of **HSYNC** inputs. If the length of high is longer than 7us and the length of low is shorter than 6us, the **HPOL** bit will be zero, indicates negative polarity. If the length of low is longer than 7us and the length of high is shorter than 6us, the **HPOL** bit is one, positive polarity. The **VSYNC** polarity detection circuit perform the similar structure with **HSYNC** polarity detection circuit. If the length of high is longer than 4ms and the length of low is shorter than 2ms, the **VPOL** bit will be zero, indicates negative polarity. If the length of low is longer than 4ms and the length of high is shorter than 2ms, the **VPOL** bit is one, positive polarity. Both **HSYNC** and **VSYNC** polarity flags are read-only, and will not affect any internal circuitry. When the **COMP** bit in **SPCSR** register is set, the **HPOL** bit will be the same as **VPOL** bit which is detected under the criteria stated in previous statements.

10.2.2 Sync Signal Counters

There are two counters (horizontal frequency counter and vertical frequency counter) to count the number of horizontal sync pulses within 32ms period and the number of system clock cycles between two vertical sync pulses. These two data can be read by the CPU to check the signal frequencies and can be used to determine the video mode. The 13-bit vertical frequency register encompasses vertical frequency range from about 15 Hz to 127 Hz. Due to the asynchronous timing between incoming **VSYNC** and internal processor clock, there will be ±1 count error on the reading from the register for the same vertical frequency. The horizontal counter counts the pulses on **HSYNC** pin, and is uploaded to the $0F and $10 registers every 32.768ms. The step unit in the lower 5-bit register is 0.3125KHz. And the least 7 bits in the HFHR register shows the number of KHz of incoming **HSYNC** signal. The MSB of the HFHR is the overflow flag of H-counter, which will be cleared when the register is read by CPU.

10.2.3 Polarity Controlled HSYNO/VSYNO Outputs

The input **HSYNC** and **VSYNC** signal can be output to PC6 and PC7 when the configuration bit of PC6 and PC7 in register $0B are set for SYNC output. Two

corresponding polarity control bits, bit 3 and bit 2 of register $0C, can change the polarity of **HSYNO**/**VSYNO** outputs. The result **HSYNO** and **VSYNO** outputs can vary while the setting in **SPCSR** and **SPIOCR** register is different. If the **COMP** bit in **SPCSR** register is set, the incoming composite Sync signal will be the HSYNO output and the extracted VSYNC with 6~7us delay will be the VSYNC output. When the **SOUT** bit in **SPIOCR** register is set, the internal free-running **55.556KHz** with 2us pulse will be the **HSYNO** output and the other free-running **72.34Hz** with 108us pulse will be the **VSYNO** output.

10.2.4 CLAMP Pulse Output

The logic will generate a 0.5us - 0.75us pulse at either the leading edge or the trailing edge which is specified by the **BPOR** bit in the **SPIOCR** register. See **Figure 10-1** for its detail timing relation. One control bit to invert the output polarity of CLAMP pulse is located at bit 5 of **SPIOCR**.

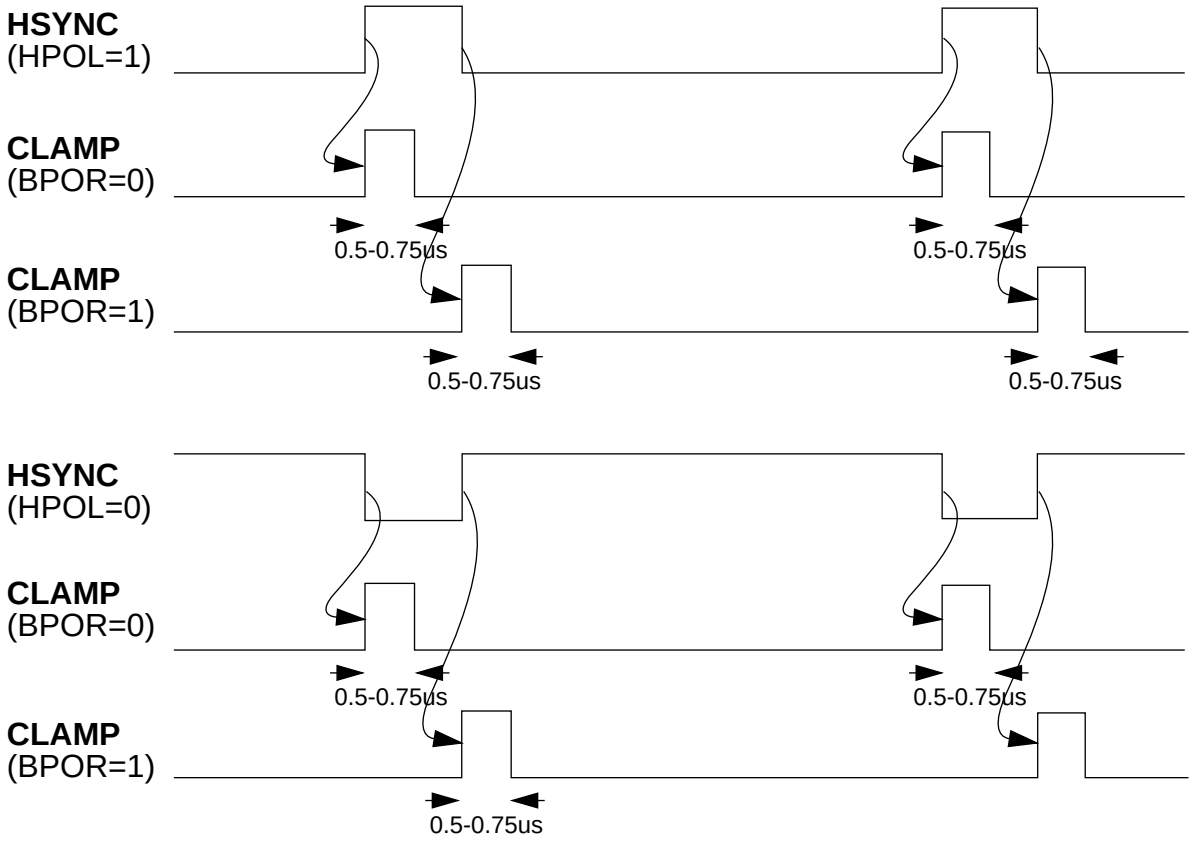


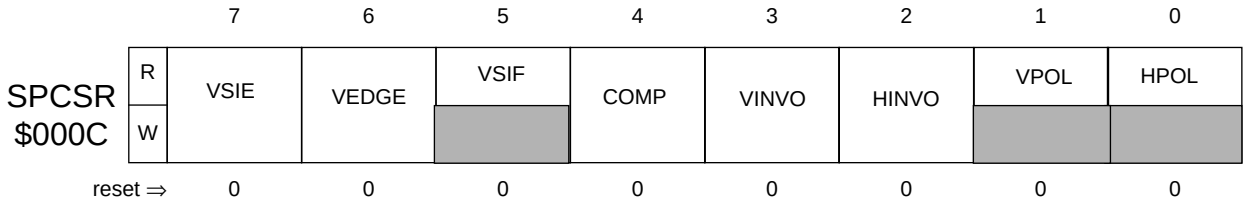
Figure 10-1: CLAMP output waveform

10.3 Registers

There are five registers associated with the SYNC PROCESSOR module as described below.

10.3.1 Sync Processor Control and Status Register (SPCSR)

NOTE: Please don't use BSET or BCLR to manipulate this register when VSIE is set and I-bit is clear, or it will cuase abnormal reset.



VSIE bit 7 — When VSync Interrupt Enable (VSIE) bit is set, the VSIF flag is enabled to generate an interrupt request to the CPU. When VSIE is cleared, the VSIF flag is prevented from generating an interrupt request. Reset clears this bit.

VEDGE bit 6 — The VEDGE bit specifies the triggering edge of VSYNC interrupt. When it is zero, the rising edge of internal VSYNC signal which is either from the VSYNC pin or extracted from the composite input signal will set VSIF flag. When it is one, the falling edge of internal VSYNC signal will set VSIF flag. Reset clears this bit.

VSIF bit 5 — This flag is a read-only bit and is set by the specified edge of internal VSYNC signal which is either from the VSYNC pin or extracted from the composite input signal. The triggering edge is specified by the VEDGE bit, see the above description of VEDGE for details. It is cleared by writing a zero to it or reset.

COMP bit 4 — This COMPosite video input enable bit is set to enable the separator circuit which extracts the VSYNC pulse from composite input in HSYNC pin. The extracted VSYNC pulse will be fed into the vertical counter, vertical polarity detection circuit, and VSYNO output circuit as well. Its measurable timing is the same as the separate VSYNC pin input. Reset clears this bit.

VINVO bit 3 — This bit controls the output polarity of the VSYNO signal. When it is zero, the VSYNO output is identical to the VSYNC input. When it is one, the inverted VSYNC signal is output to VSYNO pin.

HINVO bit 2 This bit controls the output polarity of the HSYNO signal. When it is zero, the HSYNO output is identical to the HSYNC input. When it is one, the inverted HSYNC signal is output to HSYNO pin.

VPOL bit 1 This bit shows the polarity of VSYNC input. If it is one, the VSYNC input has positive polarity. If it is zero, the VSYNC input has negative polarity. Reset clears this bit.

HPOL bit 0 This bit shows the polarity of HSYNC input. If it is one, the HSYNC input has positive polarity. If it is zero, the HSYNC input has negative polarity. Reset clears this bit.

10.3.2 Sync Processor Input/Output Control Register (SPIOCR)

		7	6	5	4	3	2	1	0
SPIOCR $0011	R	VSYNCS	HSYNCS	COINV	HVTST	SOGIN	CLAMPOE	BPOR	SOUT
	W								
reset ⇒		0	0	0	0	0	0	0	0

VSYNCS bit 7 The VSYNCS bit reflects the logical state of VSYNC input. It is a read only bit.

HSYNCS bit 6 The HSYNCS bit reflects the logical state of HSYNC input. It is a read only bit.

COINV bit 5 This Clamp Output INVert bit will invert the CLAMP output. When it is zero, the CLAMP output has default positive going pulse as illustrated in **Figure 10-1**. When it is one, the CLAMP output is inverted as negative pulse generated. Reset clears this bit.

HVTST bit 4 This HV TeST bit is reserved for testing purpose. It can be accessed only in test mode. So user must be careful while developing the program in EVS platform. Reset clears this bit.

SOGIN bit 3 If the SOGIN bit is one, the SOG pin which is shared with PD3 will be selected as the composite sync input when the COMP bit in SPCSR register is one. If it is zero, the HSYNC pin is the default composite input pin when the COMP bit is one. Reset clears this bit.

CLAMPOE bit 2 The CLAMP Output Enable bit is set to configure the PD2 pin as the CLAMP pulse output pin. Reset clear this bit.

BPOR bit 1 The Back PORch bit defines the triggering edge of clamp output. When it is one, the clamp pulse is generated at the trailing edge of HSYNC input. When it is zero, the clamp pulse is generated at the leading edge of HSYNC input. Reset clears this bit.

SOUT bit 0 The SOUT will select the output signals of VSYNO and HSYNO from the internal free-running counter. When it is zero, the incoming HSYNC and VSYNC or extracted VSYNC

will be output to the HSYNO and VSYNO pins. When it is one, the free-running 55.556KHz HSYNC with 2us negative pulse and 72.34Hz VSYNC with 108us negative pulse will be generated to the HSYNO and VSYNO output stages. Reset clears this bit.

10.3.3 Vertical Frequency Registers (VFRs)

VFHR $000D

	7	6	5	4	3	2	1	0
R	VOF	0	0	VF12	VF11	VF10	VF9	VF8
W								
reset ⇒	0	0	0	0	0	0	0	0

VFLR $000E

	7	6	5	4	3	2	1	0
R	VF7	VF6	VF5	VF4	VF3	VF2	VF1	VF0
W								
reset ⇒	0	0	0	0	0	0	0	0

VFR	Max Freq	Min Freq	VFR	Max Freq	Min Freq
$03C0	130.34 Hz	130.07 Hz	$0823	60.04 Hz	59.98 Hz
$03C1	130.21 Hz	129.94 Hz	$0824	60.01 Hz	59.95 Hz
$03C2	130.07 Hz	129.80 Hz	$0825	59.98 Hz	59.92 Hz
$04E2	100.08 Hz	99.92 Hz	$09C4	50.02 Hz	49.98 Hz
$04E3	100.00 Hz	99.84 Hz	$09C5	50.00 Hz	49.96 Hz
$04E4	99.92 Hz	99.76 Hz	$09C6	49.98 Hz	49.94 Hz
$06F9	70.07 Hz	69.99 Hz	$1FFD	15.266 Hz	15.262 Hz
$06FA	70.03 Hz	69.95 Hz	$1FFE	15.264 Hz	15.260 Hz
$06FB	69.99 Hz	69.91 Hz	$1FFF	15.262 Hz	15.258 Hz

This 13-bit read only register pair contains information of the vertical frame frequency. An internal counter counts the number of internal clocks between two **VSYNC** pulses. The most significant 5 bits of counted value will then be transferred to high byte register, $0D, and the least significant 8 bits of counted value is transferred to one intermediate buffer. When the high byte register is read, the 8-bit counted value stored in the intermediate buffer will be uploaded to the low byte register, $0E. So the program must read the high byte register first then low byte register in order to get the complete counted value of one vertical frame. If the counter overflow, the VOF flag will be set while the counter values stored in

the **VFRs** registers are meaningless. The data corresponds to the period of one vertical frame. This register can be read to determine if the frame frequency is valid, and to determine the video mode. The MSB in the **VFHR** register will indicate the overflow condition when the period of **VSYNC** frame exceeds 64.768ms (lower than 15.258Hz). This VOF flag is default to be zero and will be update every vertical frame or set when the counter overflows.

The frame frequency is calculated by 1/(VFR±1 x 8μS) or 1/(VFR±1 x 16 x tcyc).

The table above shows examples for the Vertical Frequency Register, all VFR numbers are in hexadecimal:

10.3.4 Hsync Frequency Registers (HFRs)

		7	6	5	4	3	2	1	0
HFHR $000F	R	HOVER	HFH6	HFH5	HFH4	HFH3	HFH2	HFH1	HFH0
	W								
reset ⇒		0	0	0	0	0	0	0	0

		7	6	5	4	3	2	1	0
HFLR $0010	R	0	0	0	HFL4	HFL3	HFL2	HFL1	HFL0
	W								
reset ⇒		0	0	0	0	0	0	0	0

This 13-bit read-only register pair contains the number of horizontal lines within 32ms and one overflow bit, HOVER. An internal line counter counts the horizontal sync pulses within 32ms window of every 32.768ms period. The most significant 7 bits of counted value will then be transferred to high byte register, $0F, and the least significant 5 bits of counted value is transferred to one intermediate buffer. When the high byte register is read, the 5-bit counted value stored in the intermediate buffer will be uploaded to the low byte register, $10. So the program must read the high byte register first then low byte register in order to get the complete counted value of horizontal pulses. The HOVER bit will be set immediately if the number of incoming horizontal sync pulses in 32ms are more than 4095, that means **HSYNC** frequency is over 128KHz. The HFHR data can be read to determine the number of KHz of **HSYNC** frequency and the HFLR shows the sub-KHz value of **HSYNC** frequency. This makes user easy to read the frequency of **HSYNC** and determine the video mode.

10.4 System Operation

This module is used mainly for user to determine the video mode of incoming **HSYNC** and **VSYNC** of various frequency and polarity. It is designed to assist in determining the video mode including **DPMS** modes. The definition of 'No pulses' of **DPMS** standard can be detected when the value of H counter register is less than one or the **VOF** in the **VFHR** register is set. For the HSYNC counter value will be updated repeatedly every 32.768ms

and also we know the valid VSYNC pulse, more than 40Hz, could arrive in shorter time. So it is recommended that user reads the counter value every 32.768ms period.

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SECTION 11 MULTI-FUNCTION TIMER

11.1 Introduction

This module provides miscellaneous function to the MC68HC05BD7. It includes a timer overflow, real-time interrupt, and watchdog functions. Also included in the module is the capability of selecting the mode of the maskable external interrupt pin, either edge-triggered mode only or both edge-triggered mode and level-triggered mode.

The clock base for this module is derived from bus clock divided by four. For a 2 MHz E (CPU) clock, the clock base is 0.5 MHz. This clock base is then divided by an 8-stage ripple counter to generate the timer overflow. Timer overflow rate is thus E/1024. The output of this 8-stage ripple counter then drives one stage divider to generate real time interrupt. Hence, the clock base for real time interrupt is E/2,048. Real time interrupt rate is selected by RT0 and RT1 bits of Multi-Function Timer Control/Status Register (MFTCSR). The interrupt rates are E/2,048, E/(2,048X2), E/(2,048X4), and E/(2,048X8). The selected real time interrupt rate is then divided by 64 to generate COP reset.

The COP watchdog timer function is implemented by using a COP counter. The minimum COP reset rates are controlled by RT0 and RT1 of MFTCSR. If the COP circuit times out, an internal reset is generated and the normal reset vector is fetched. Preventing a COP time-out is done by writing a ‘0’ to bit 0 of address $3FF0. This write operation resets the divide-by-64 counter stage described in the previous paragraph. The COP counter has to be cleared periodically by software with a period less than COP reset rate. It continues to count even though the CPU is in WAIT mode. In MC68HC05BD7, the COP is always enabled.

11.2 Register

There are two registers in the Multi-Function Timer as discussed below.

11.2.1 Multi-function Timer Control/status Register

NOTE: Please don’t use BSET or BCLR to manipulate this register when I-bit is clear, or it will generate abnormal reset.

		7	6	5	4	3	2	1	0
MFTCSR $0008	R	TOF	RTIF	TOFIE	RTIE	IRQN	INHIRQ	RT1	RT0
	W								
reset ⇒		0	0	0	0	0	0	1	1

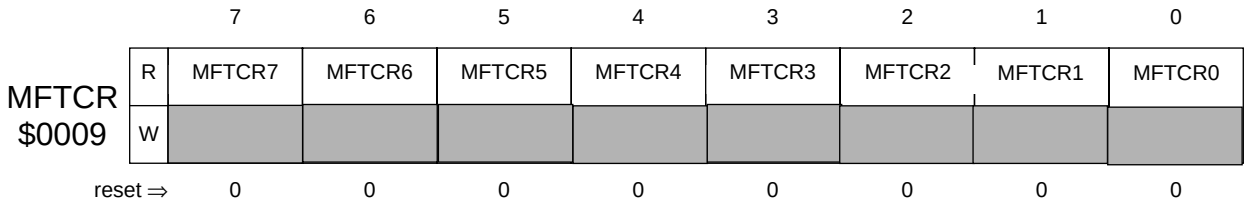
TOF bit 7 Timer Overflow Flag indicates if the 8-bit ripple counter overflows. TOF is set when the 8-bit counter rolls over from

		$FF to $00. A CPU interrupt request will be generated if TOFIE is set. TOF is a clearable, read-only status bit. Clearing the TOF is done by writing a ’0’ to TOF.
RTIF	bit 6	Real Time Interrupt Flag indicates if the output of the RTI circuit goes active. The clock frequency that drives the RTI circuit is E/2,048, giving a maximum interrupt period of 1.024 milliseconds at a bus rate of 2 MHz. A CPU interrupt request will be generated if RTIE is set. RTIF is a clearable, read-only status bit. Clearing the RTIF is done by writing a ’0’ to RTIF.
TOFIE	bit 5	When Timer Over Flow Interrupt Enable (TOFIE) bit is set, the TOF flag is enabled to generate an interrupt request to the CPU. When TOFIE is cleared, the TOF flag is prevented from generating an interrupt request.
RTIE	bit 4	When Real Time Interrupt Enable (RTIE) is set, the RTIF flag is enabled to generate an interrupt request to the CPU. When RTIE is cleared, the RTIF flag is prevented from generating an interrupt request.
IRQN	bit 3	0 = Both level and edge triggering are detected for external interrupt ($\overline{IRQ}$). 1 = Only edge triggering is detected for external interrupt.
INHIRQ	bit 2	The INHibit IRQ bit will inhibit the external interrupt input. When it is set, no active falling edge or low period will be recognized as interrupt request. It is possible for a low state input on the $\overline{IRQ}$ pin to be seen as a falling edge event when the INHIRQ bit changes from one to zero, see **Figure 4-2** for reference. Reset clears this bit.
RT1-0	bit 1,0	These two bits are used to define real time interrupt rate as well as COP reset rate as tabulated in **Table 11-1**. Reset sets these two bits for the slowest watchdog reset rate. Note that the minimal COP reset period is determined by dividing the COP master clock, which is the real time interrupt clock, by 63(63=64-1). The reason is that COP reset operation is asynchronous to COP master clock edge. Therefore it is possible that right after COP reset operation, a COP master clock edge arrives to start counting COP period. The effective count of the divide-by-64 counter is hence 63 rather than 64. RT1, RT0 should only be changed right after COP timer has been reset; otherwise, unpredictable result will occur.

RT1	RT0	Min. COP Reset Period @ 2 MHz E Clock	RTI Period @ 2 MHz
0	0	64.512 ms	1.024 ms
0	1	129.024 ms	2.048 ms
1	0	258.048 ms	4.096 ms
1	1	516.096 ms	8.192 ms

Table 11-1: COP Reset Rates and RTI Rates

11.2.2 MFT Timer Counter Register



This 8-bit free-running counter register, MFTCR, can be read at location $0009. It is cleared by reset.

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SECTION 12 A/D CONVERTER

12.1 Introduction

The Analog-to-Digital Converter (ADC) system consists of four analog input channels and a single 6-bit D/A Converter and Comparator, with continuous conversion. A result flag indicates if the comparator output is above or below the analog Input. ADC is disabled by setting AD5 to AD0 bits of ADC Control/Status Register to all 1's. This disable function is mainly for low power application.

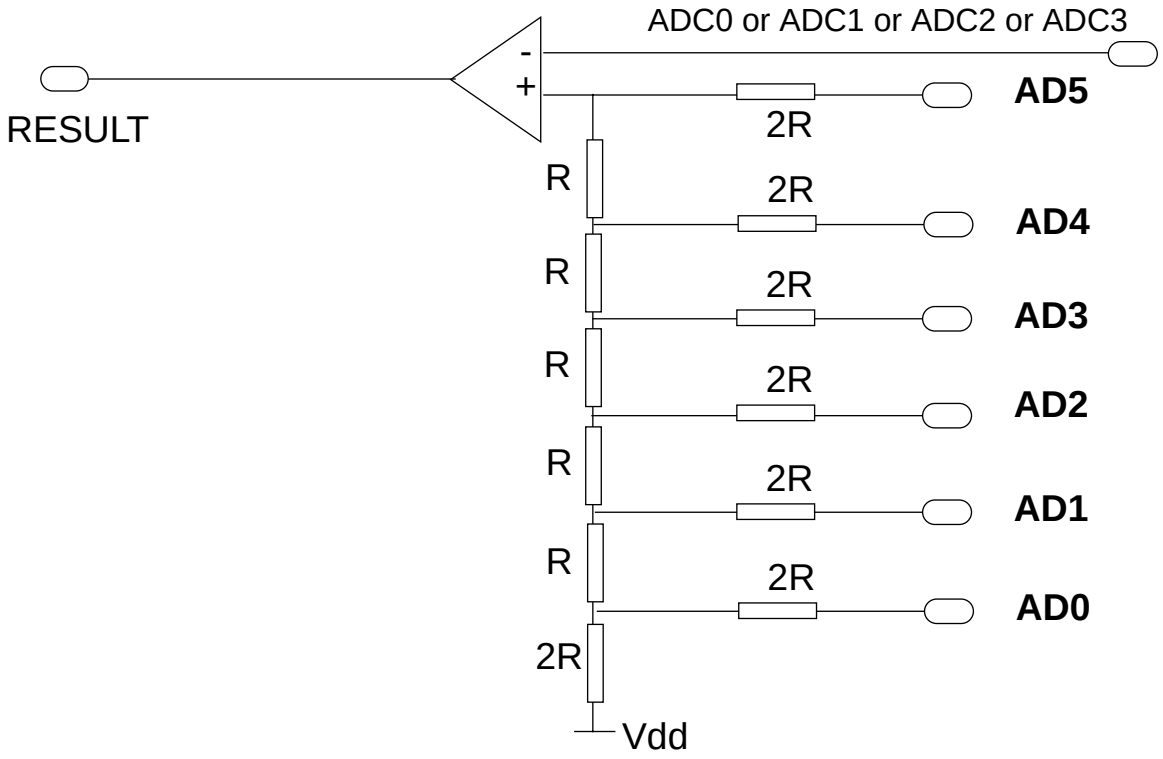


Figure 12-1: Structure of A/D Converter

12.2 Input

The ADC has four multiplexed input channels. Only one of the four channels will be selected by CHSL1 and CHSL0 bits as analog input.

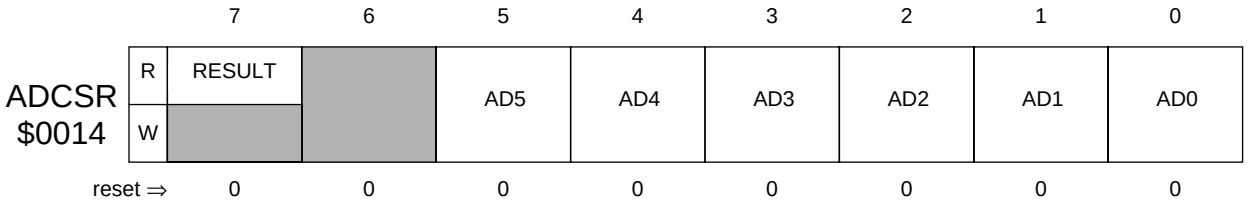
12.2.1 ADC0-ADC3

The ADC0 to ADC3 inputs are multiplexed with the PC2 to PC5 port pins. They are selected as ADC input then the corresponding AD0-AD3 bit in the CR2 register is one. The user can use the CHSL1 and CHSL0 bits to select one of the four channels to do the A/D Conversion and get the approximate digital value of each input channel.

12.3 Registers

12.3.1 ADC Control/status Register

This read/write register, located at address $14, contains six control bits and one status bit.



RESULT - Comparator Status Bit (Read Only)

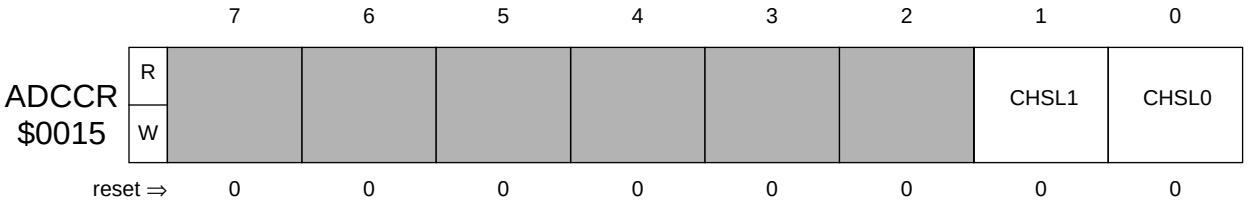
When set, D/A output ≥ ANALOG IN.
When clear, D/A output ≥ ANALOG IN.

AD5:0 - A/D Digital Result

These bits are written by the user to perform successive approximations in software. When a value causes the RESULT bit to change state from the value immediately before or after it, AD5:0 are considered to be the digital equivalent of the analog input. Note that when AD5:0 are all 1's, ADC is virtually turned off to minimize power consumption.

12.3.2 ADC Channel Register

The ADC Channel Register, located at address $15 contains only two bits.



CHSL1:CHSL0 - Channel select bits

These two bit will select one of the four ADC input channels as analog input source. Following table shows its configuration.

CHSL1:CHSL0 = 0 : 0 ==> ADC0
CHSL1:CHSL0 = 0 : 1 ==> ADC1
CHSL1:CHSL0 = 1 : 0 ==> ADC2
CHSL1:CHSL0 = 1 : 1 ==> ADC3

12.4 Program Example

The following example shows how to convert analog input channel 0 by using binary search method. This approach method will guarantee any conversion can be done within 6 iterations, 98us at 2MHz bus clock. For ADCIN1 conversion, change #$00 to #$01. ADCCR is the ADC Channel Register.

```
CR2     EQU     $0B             ; Configuration Register
ADCCR   EQU     $15             ; ADC Channel Register
ADCSR   EQU     $14             ; ADC Control & Status Register
ADCDATA EQU     $50             ; RAM byte to store the conversion result
REFH    EQU     $51             ; RAM byte to store the high end of conversion
REFL    EQU     $52             ; RAM byte to store the low end of conversion
        ORG     $1000
        LDA     #$3C
        STA     CR2             ; Configure PC2-PC5 as ADC inputs
        LDA     #$00
        STA     ADCCR           ; Select the input channel
        LDA     #$00
        STA     REFL            ; initial low end = #$00
        LDA     #$3F
        STA     REFH            ; initial high end =#$3F
DALP    LDA     REFH
        ADD     REFL
        LSRA                    ; A= (REFH + REFL)/2
        STA     ADCSR           ; Store the comparison data to D/A
        CMP     REFL            ; Compare the stored value with REFL
        BEQ     DONE            ; If equal, the A is the result digital value
        BRSET   7,ADCSR,SETHI   ; Check the RESULT flag
        STA     REFL            ; If lower, set A as the low end of conversion
        BRA     DALP
SETHI   STA     REFH            ; If higher, set A as the high end of conversion
        BRA     DALP
DONE    STA     ADCDATA
```

* Input voltage calculation at V_{DD}=5V:

$$ADCDATA \times 0.078125V \leq INPUT \leq (ADCDATA+1) \times 0.078125V$$

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SECTION 13 ELECTRICAL SPECIFICATIONS

13.1 Maximum Ratings

(Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	–0.3 to +7.0	V
Input Voltage	V_{IN}	V_{SS} –0.3 to V_{DD} +0.3	V
$\overline{IRQ}$ Pin	V_{IN}	V_{SS} –0.3 to 2V_{DD} +0.3	V
Current Drain Per Pin Excluding VDD and VSS	V_{IN}	25	mA
Operating Temperature Range MC68HC05BD7 (Standard)	T_A	0 to +70	°C
Storage Temperature Range	T_{STG}	–65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. For proper operation, it is recommended that V_{IN} and V_{OUT} be constrained to the range $V_{SS} \le (V_{IN}$ or $V_{OUT}) \le V_{DD}$. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

13.2 Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance Plastic	θ_{JA}	60	°C/W

13.3 DC Electrical Characteristics

(V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0Vdc, T_A = 0°C to +70°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Output High Voltage (I_{Load} = -5.0 mA) PA0-PA7, PB0-PB1, PC2-PC7, PWM0-PWM7	V_{OH}	V_{DD}–0.8	—	—	V
Output Low Voltage (I_{Load} = 5.0 mA for +5V pins and I_{Load} = 10.0 mA for +12V open-drain pins) PA0-PA7, PB0-PB5, PC0-PC7, PD0-PD3, PWM0-PWM7	V_{OL}	—	—	0.5	V
Input High Voltage PA0-PA7, PB0-PB5, PC0-PC7, PD0-PD1, $\overline{RESET}$, $\overline{IRQ}$, EXTAL (TTL Level) VSYNC, HSYNC, SOG SDA,SCL	V_{IH} V_{IH} V_{IH}	0.8 x V_{DD} 2.0 0.8 x V_{DD}	— — —	V_{DD} V_{DD} V_{DD}	V V V
Input Low Voltage PA0-PA7, PB0-PB5, PC0-PC7, PD0-PD3, $\overline{RESET}$, $\overline{IRQ}$, EXTAL (TTL Level) VSYNC, HSYNC, SOG SDA,SCL	V_{IL}	V_{SS} V_{SS} V_{SS}	— — —	0.2 x V_{DD} 0.8 0.2 x V_{DD}	V V V
Supply Current (see Notes) Run Wait	 I_{DD} I_{DD}	 — —	 8 4	 20 8	 mA mA
I/O Ports Hi-Z Leakage Current PA0-PA7, PB0-PB5, PC0-PC7, PD0-PD3	I_{OZ}	—	—	10	µA
Input Current RESET, IRQ, EXTAL, VSYNC, HSYNC	I_{IN}	—	—	1	µA
Capacitance Ports (as Input or Output), $\overline{RESET}$, $\overline{IRQ}$, EXTAL, XTAL HSYNC, VSYNC	 C_{OUT} C_{IN}	 — —	 — —	 12 8	 pF pF

NOTES:

1. All values shown reflect average measurements.
2. Typical values at midpoint of voltage range, 25°C only.
3. Wait I_{DD}: Only timer system and SSP active.
4. Run (Operating) I_{DD}, Wait I_{DD}: Measured using external square wave clock source to EXTAL (f_{OSC} = 4.2 MHz), all inputs 0.2 VDC from rail; no DC loads, less than 50pF on all outputs, C_L = 20 pF on EXTAL.
5. Wait I_{DD}: All ports configured as inputs, V_{IL} = 0.2 VDC, V_{IH} = V_{DD}-0.2 VDC.
6. Wait I_{DD} is affected linearly by the EXTAL capacitance.

13.4 Control Timing

(V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, T_A = 0˚C to +70˚C, unless otherwise noted)

Characteristic	Symbol	Min	Max	Units
Frequency of Operation Crystal Oscillator Option External Clock Source	 f_{OSC} f_{OSC}	 — dc	 4.2 4.2	 MHz MHz
Internal Operating Frequency Crystal Oscillator (f_{OSC}/2) External Clock (f_{OSC}/2)	 f_{OP} f_{OP}	 — dc	 2.1 2.1	 MHz MHz
Cycle Time (1/f_{op})	t_{CYC}	480	—	ns
Crystal Oscillator Start-up Time (Crystal Oscillator option)	t_{OXON}	—	100	ms
RESET Pulse Width Low	t_{RL}	1.5	—	t_{CYC}
IRQ Interrupt Pulse Width Low (Edge-Triggered)	t_{ILIH}	125	—	ns
IRQ Interrupt Pulse Period	t_{ILIL}	note 1	—	t_{CYC}
EXTAL Pulse Width	t_{OH}, t_{OL}	100	—	ns

NOTE:

1. The minimum period t_{ILIL} should not be less than the number of cycles it takes to execute the interrupt service routine plus 21 t_{CYC}.

13.5 DDC12AB TIMING

(V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0Vdc, T_A = 0˚C to +70˚C, unless otherwise noted

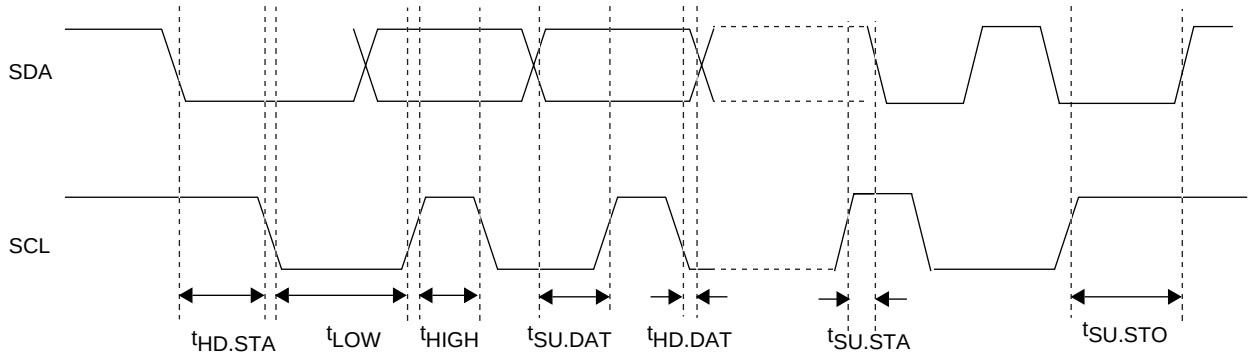
13.5.1 DDC12AB Interface Input Signal Timing

Parameter	Symbol	Min	Max	Units
START condition hold time	$t_{HD.STA}$	2	—	t_{CYC}
Clock low period	t_{LOW}	4	—	t_{CYC}
Clock high period	t_{HIGH}	4	—	t_{CYC}
Data set up time	$t_{SU.DAT}$	250	—	ns
Data hold time	$t_{HD.DAT}$	0	—	ns
START condition set up time (for repeated START condition only)	$t_{SU.STA}$	2	—	t_{CYC}
STOP condition set up time	$t_{SU.STO}$	2	—	t_{CYC}

13.5.2 DDC12AB Interface Output Signal Timing

Parameter	Symbol	Min	Max	Units
SDA / SCL rise time (see NOTE 1)	t_R	—	1.0	µs
SDA / SCL fall time (see NOTE 1)	t_F	—	300	ns
Data set up time	$t_{SU.DAT}$	t_{LOW}	—	ns
Data hold time	$t_{HD.DAT}$	0	—	ns

NOTE:
1. With 200 pF loading on the SDA/SCL pins



13.6 HSYNC/VSYNC Input Timing

(V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0 VDC, T_A = 0°C to +70°C, unless otherwise noted)

Parameter	Symbol	Min	Max	Units
VSYNC input sync pulse	$t_{VI.SP}$	1/2	4096	t_{CYC}
HSYNC input sync pulse	$t_{HI.SP}$	1/2	12	t_{CYC}
VSYNC to VSYNO delay (8pF loading)	t_{VVd}	30	40	ns
HSYNC to HSYNO delay (8pF loading)	t_{HHd}	30	40	ns

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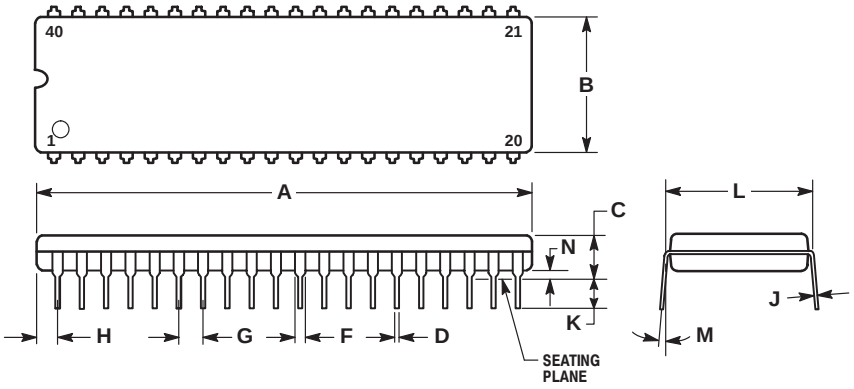
SECTION 14 MECHANICAL SPECIFICATIONS

14.1 Introduction

The MC68HC05BD7 is available in 40-pin DIP and 42-pin SDIP packages.

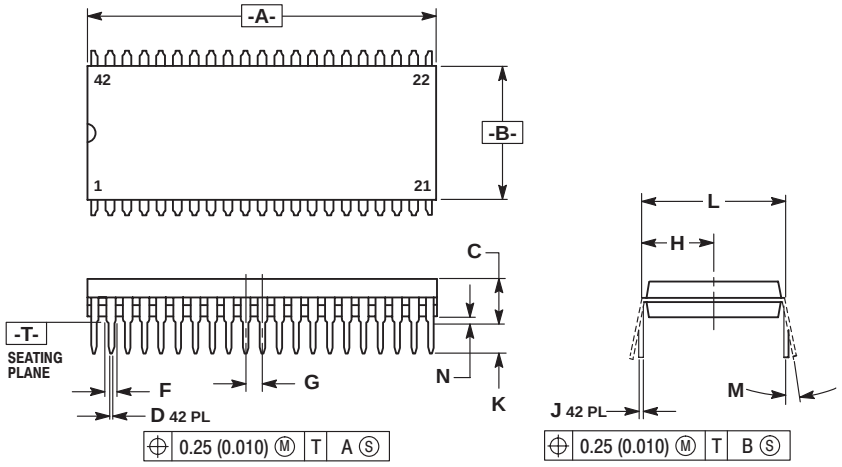
14.2 40-Pin DIP Package (Case 711-03)



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

14.3 42-Pin SDIP Package (Case 858-01)



NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH. MAXIMUM MOLD FLASH 0.25 (0.010).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.435	1.465	36.45	37.21
B	0.540	0.560	13.72	14.22
C	0.155	0.200	3.94	5.08
D	0.014	0.022	0.36	0.56
F	0.032	0.046	0.81	1.17
G	0.070 BSC		1.778 BSC	
H	0.300 BSC		7.62 BSC	
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.600 BSC		15.24 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.02

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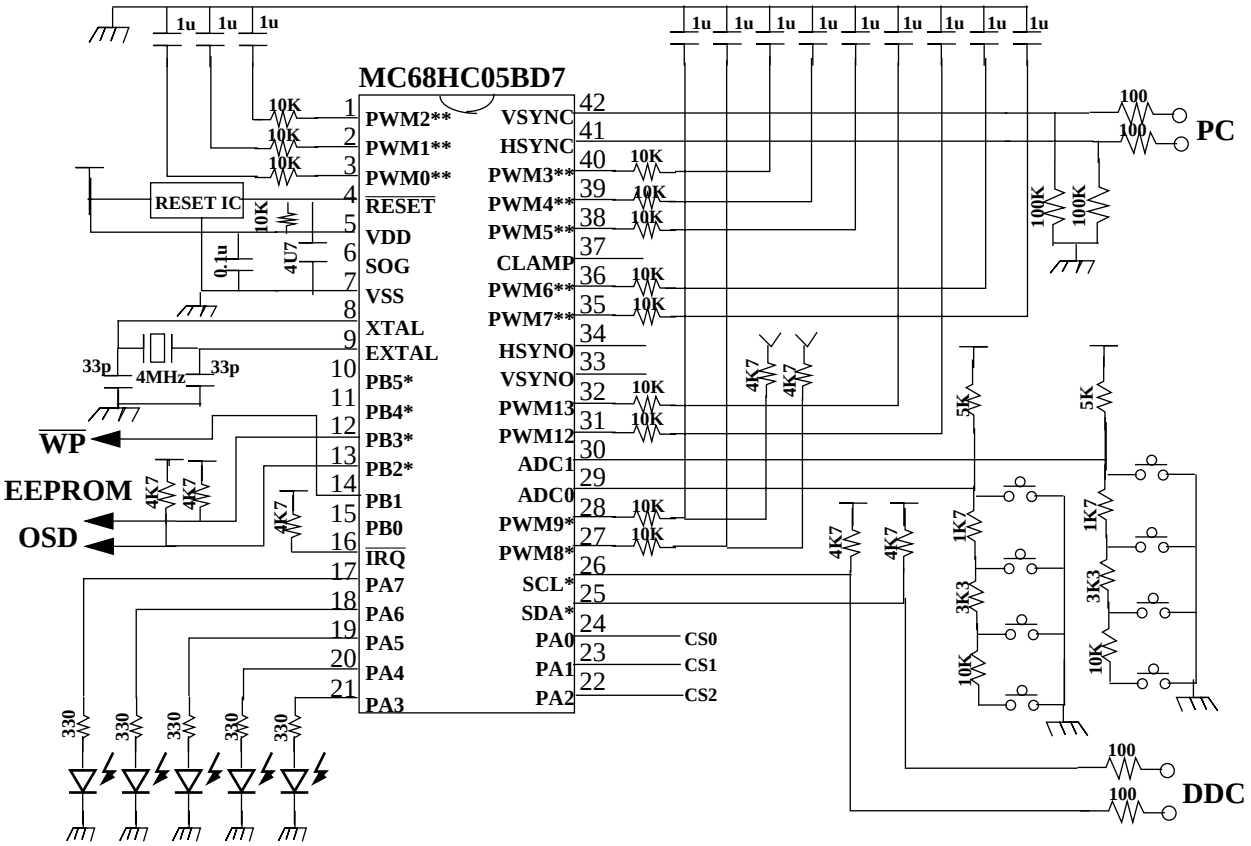
SECTION 15 APPLICATION DIAGRAM



***Note: RESET IC is MC34064**

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