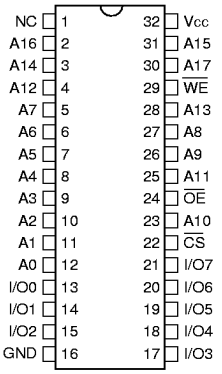
# 256Kx8 SRAM MODULE

## FIG. 1

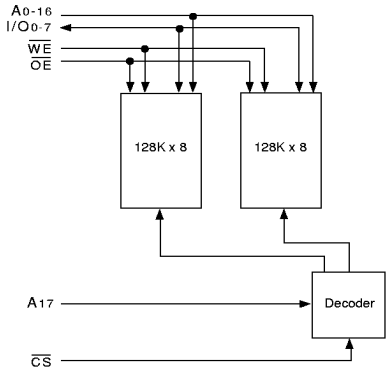
### PIN CONFIGURATION
### TOP VIEW




### PIN DESCRIPTION

| | |
|---|---|
| $A_{0-17}$ | Address Inputs |
| $I/O_{0-7}$ | Data Input/Output |
| $\overline{CS}$ | Chip Select |
| $\overline{OE}$ | Output Enable |
| $\overline{WE}$ | Write Enable |
| $V_{CC}$ | +5.0V Power |
| GND | Ground |
| NC | No Connect |

### BLOCK DIAGRAM




## FEATURES

- Access Times 20, 25, 35, 45ns
- Rad Tolerant Devices Available
- JEDEC Standard Packages:
  - 32 pin, Hermetic Ceramic DIP (Package 300)
  - 32 pin Vertical In Line (Package 304). Package under development.
- Commercial, Industrial and Military Temperature Ranges
- Organized as 256K x 8
- 5 Volt Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Low Power Devices for Battery Back-Up Applications Available

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Operating Temperature | $T_A$ | -55 | +125 | °C |
| Storage Temperature | $T_{STG}$ | -65 | +150 | °C |
| Signal Voltage Relative to GND | $V_G$ | -0.5 | Vcc+0.5 | V |
| Junction Temperature | $T_J$ | | 150 | °C |
| Supply Voltage | Vcc | -0.5 | 7.0 | V |

## RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply Voltage | Vcc | 4.5 | 5.5 | V |
| Input High Voltage | $V_{IH}$ | 2.2 | Vcc + 0.3 | V |
| Input Low Voltage | $V_{IL}$ | -0.5 | +0.8 | V |
| Operating Temp. (Mil.) | $T_A$ | -55 | +125 | °C |

## TRUTH TABLE

| $\overline{CS}$ | $\overline{OE}$ | $\overline{WE}$ | Mode | Data I/O | Power |
|---|---|---|---|---|---|
| H | X | X | Standby | High Z | Standby |
| L | L | H | Read | Data Out | Active |
| L | X | L | Write | Data In | Active |
| L | H | H | Out Disable | High Z | Active |

## CAPACITANCE

(@ $T_A$ = +25°C)

| Parameter | Symbol | Condition | Max | Unit |
|---|---|---|---|---|
| Input capacitance | $C_{IN}$ | $V_{IN}$ = 0V, f = 1.0MHz | 30 | pF |
| Output capicitance | $C_{OUT}$ | $V_{OUT}$ = 0V, f = 1.0MHz | 30 | pF |

This parameter is guaranteed by design but not tested.

## DC CHARACTERISTICS

(Vcc = 5.0V, Vss = 0V, $T_A$ = -55°C to +125°C)

| Parameter | Sym | Conditions | -20 | | -25 | | -35 | | -45 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Input Leakage Current | $I_{LI}$ | Vcc = 5.5, $V_{IN}$ = GND to Vcc | | 10 | | 10 | | 10 | | 10 | µA |
| Output Leakage Current | $I_{LO}$ | $\overline{CS}$ = $V_{IH}$, $\overline{OE}$ = $V_{IH}$, $V_{OUT}$ = GND to Vcc | | 10 | | 10 | | 10 | | 10 | µA |
| Operating Supply Current | Icc | $\overline{CS}$ = $V_{IL}$, $\overline{OE}$ = $V_{IH}$, f = 5MHz, Vcc = 5.5 | | 180 | | 180 | | 180 | | 180 | mA |
| Standby Current | $I_{SB}$ | $\overline{CS}$ = $V_{IH}$, $\overline{OE}$ = $V_{IH}$, f = 5MHz | | 50 | | 50 | | 50 | | 50 | mA |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 8mA, Vcc = 4.5 | | 0.4 | | 0.4 | | 0.4 | | 0.4 | V |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -4.0mA, Vcc = 4.5 | 2.4 | | 2.4 | | 2.4 | | 2.4 | | V |

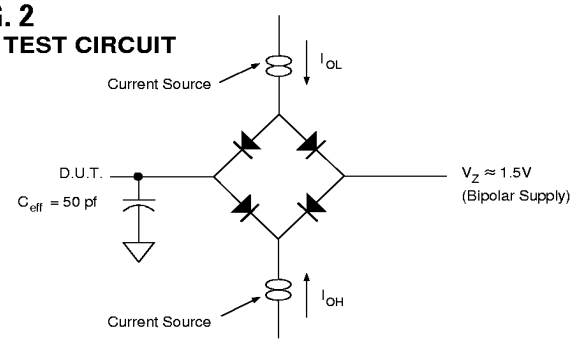
NOTE: DC test conditions: $V_{IH}$ = Vcc -0.3V, $V_{IL}$ = 0.3V

## DATA RETENTION CHARACTERISTICS

($T_A$ = -55°C to +125°C)

| Parameter | Symbol | Conditions | -20 | | | -25 | | | -35 | | | -45 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Data Retention Supply Voltage | $V_{DR}$ | $\overline{CS}$ ≥ Vcc -0.2V | 2.0 | | | 2.0 | | 5.5 | 2.0 | | 5.5 | 2.0 | | 5.5 | V |
| Data Retention Current | $I_{CCDR1}$ | Vcc = 3V | | 4.0 | 7.0 | | 4.0 | 7.0 | | 4.0 | 7.0 | | 4.0 | 7.0 | mA |

## FIG. 2
### AC TEST CIRCUIT




## AC TEST CONDITIONS

| Parameter | Typ | Unit |
|---|---|---|
| Input Pulse Levels | $V_{IL}$ = 0, $V_{IH}$ = 3.0 | V |
| Input Rise and Fall | 5 | ns |
| Input and Output Reference Level | 1.5 | V |
| Output Timing Reference Level | 1.5 | V |

**NOTES:**
$V_Z$ is programmable from -2V to +7V.
$I_{OL}$ & $I_{OH}$ programmable from 0 to 16mA.
Tester Impedance $Z_0$ = 75 Ω.
$V_Z$ is typically the midpoint of $V_{OH}$ and $V_{OL}$.
$I_{OL}$ & $I_{OH}$ are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

## AC CHARACTERISTICS

($V_{CC}$ = 5.0V, $V_{SS}$ = 0V, $T_A$ = -55°C to +125°C)

| Parameter<br>Read Cycle | Symbol | -20 | | -25 | | -35 | | -45 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Read Cycle Time | $t_{RC}$ | 20 | | 25 | | 35 | | 45 | | ns |
| Address Access Time | $t_{AA}$ | | 20 | | 25 | | 35 | | 45 | ns |
| Output Hold from Address Change | $t_{OH}$ | 3 | | 3 | | 3 | | 3 | | ns |
| Chip Select Access Time | $t_{ACS}$ | | 20 | | 25 | | 35 | | 45 | ns |
| Output Enable to Output Valid | $t_{OE}$ | | 10 | | 20 | | 25 | | 35 | ns |
| Chip Select to Output in Low Z | $t_{CLZ}$[1] | 3 | | 3 | | 3 | | 3 | | ns |
| Output Enable to Output in Low Z | $t_{OLZ}$[1] | 0 | | 0 | | 0 | | 0 | | ns |
| Chip Disable to Output in High Z | $t_{CHZ}$[1] | | 15 | | 17 | | 20 | | 30 | ns |
| Output Disable to Output in High Z | $t_{OHZ}$[1] | | 12 | | 15 | | 20 | | 25 | ns |

1. This parameter is guaranteed by design but not tested.

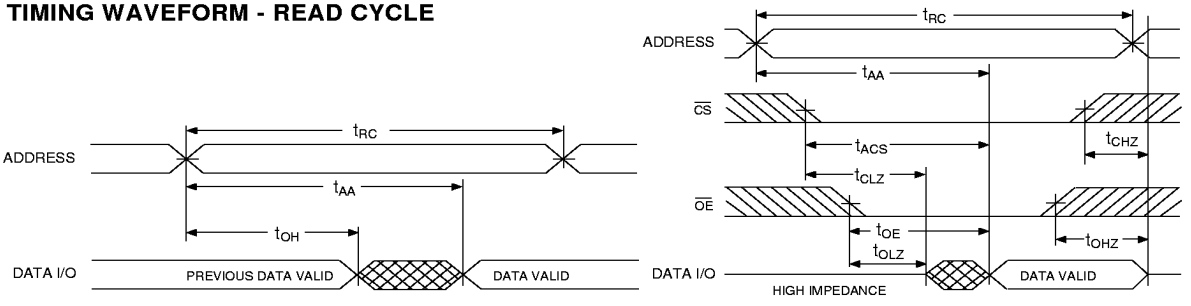
## AC CHARACTERISTICS

($V_{CC}$ = 5.0V, $V_{SS}$ = 0V, $T_A$ = -55°C to +125°C)

| Parameter<br>Write Cycle | Symbol | -20 | | -25 | | -35 | | -45 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Write Cycle Time | $t_{WC}$ | 20 | | 25 | | 35 | | 45 | | ns |
| Chip Select to End of Write | $t_{CW}$ | 16 | | 20 | | 25 | | 30 | | ns |
| Address Valid to End of Write | $t_{AW}$ | 16 | | 20 | | 25 | | 30 | | ns |
| Data Valid to End of Write | $t_{DW}$ | 15 | | 15 | | 20 | | 25 | | ns |
| Write Pulse Width | $t_{WP}$ | 16 | | 20 | | 25 | | 30 | | ns |
| Address Setup Time | $t_{AS}$ | 2 | | 2 | | 2 | | 2 | | ns |
| Address Hold Time | $t_{AH}$ | 2 | | 2 | | 2 | | 2 | | ns |
| Output Active from End of Write | $t_{OW}$[1] | 4 | | 5 | | 5 | | 5 | | ns |
| Write Enable to Output in High Z | $t_{WHZ}$[1] | 0 | 12 | 0 | 15 | 0 | 20 | 0 | 25 | ns |
| Data Hold Time | $t_{DH}$ | 1 | | 1 | | 1 | | 1 | | ns |

1. This parameter is guaranteed by design but not tested.

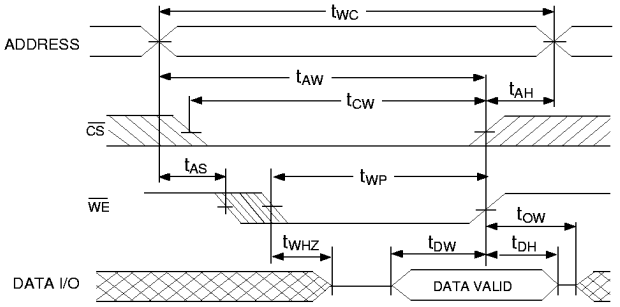
## FIG. 3
### TIMING WAVEFORM - READ CYCLE




READ CYCLE 1 ($\overline{CS}$ = $\overline{OE}$ = $V_{IL}$, $\overline{WE}$ = $V_{IH}$)

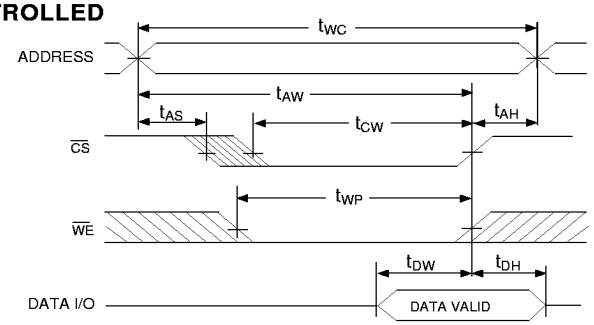
READ CYCLE 2 ($\overline{WE}$ = $V_{IH}$)

## FIG. 4
### WRITE CYCLE - $\overline{WE}$ CONTROLLED



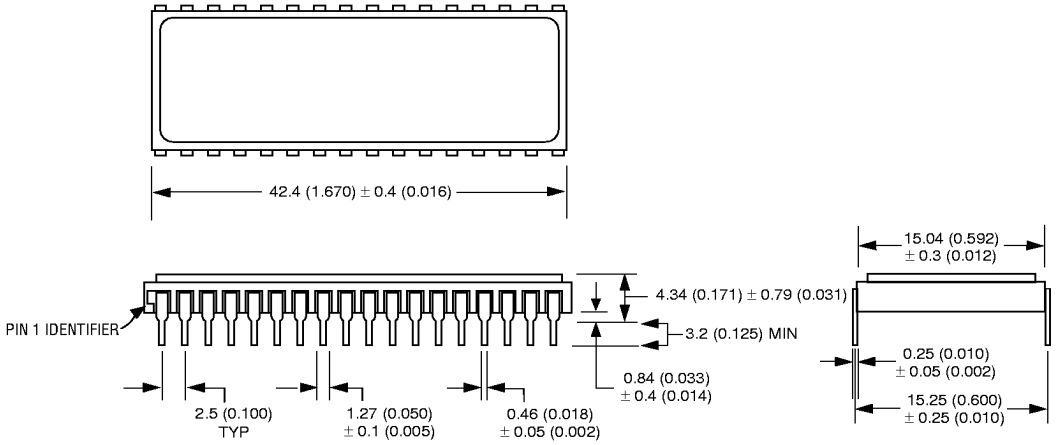

WRITE CYCLE 1, $\overline{WE}$ CONTROLLED

## FIG. 5
### WRITE CYCLE - $\overline{CS}$ CONTROLLED



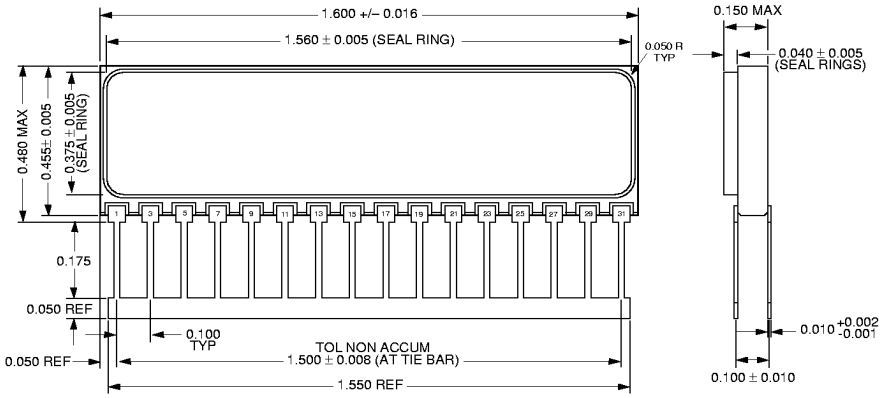

WRITE CYCLE 2, $\overline{CS}$ CONTROLLED

## PACKAGE 300: 32 PIN, CERAMIC DIP, SINGLE CAVITY SIDE BRAZED




ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

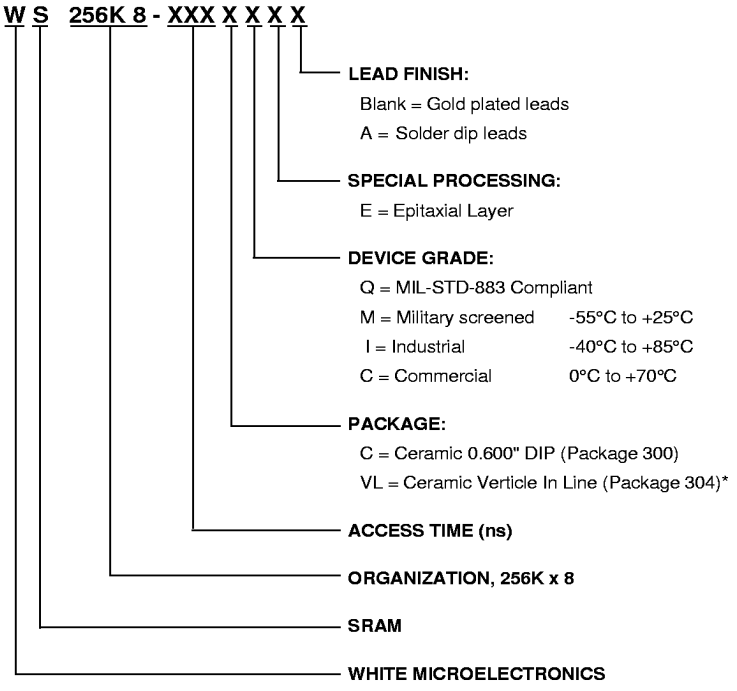
## PACKAGE 304: 32 PIN, CERAMIC VERTICAL IN LINE*




ALL LINEAR DIMENSIONS ARE MILLIMETERS

* *Package under development.*

## ORDERING INFORMATION




* *Package under development.*