2Mx32 12V FLASH MODULE *PRELIMINARY**

FEATURES

- Access Times of 90, 100, 120 nS
- Packaging:
  - 66-pin, PGA Type, 1.385 inch square, Hermetic Ceramic HIP (Package 402)
  - 68 lead, 40mm square Hermetic CQFP (Package 501), 5.1mm (0.200")
  - 68 lead, 40mm Hermetic Low Profile CQFP (Package 502), 3.5mm (0.140")
- Sector Architecture
  - 32 equal size sectors of 64KBytes per each 2Mx8 chip
  - Two step sequence of erase ensures that memory contents are not accidently erased.
- 100,000 Erase/Program Cycles Minimum (0°C to 70°C)
- Organized as 2Mx32, user configurable as 4Mx16 or 8Mx8.
- Commercial, Industrial and Military Temperature Ranges
- 12 Volt Programming. 5V ± 10% Supply.
- Low Power CMOS, 8mA Standby Typical
- Pipelined Command Execution
- Write During Erase
- Automated Byte Write and Block Erase
  - Command User Interface
  - Compatible Status Register (CSR)
  - Global Status Register (GSR)
  - 32 Block Status Registers (BSRs) per Chip
- Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
  WF2M32-XH2X - 13 grams typical
  WF2M32-XG4TX - 20 grams typical

** This data sheet describes a product under development, not fully characterized, and is subject to change without notice.*

FIG. 1 PIN CONFIGURATION FOR WF2M32-XH2X

TOP VIEW

1	12	23	34	45	56
I/O8	$\overline{RP}$	I/O15	I/O24	VCC	I/O31
I/O9	$\overline{CS2}$	I/O14	I/O25	$\overline{CS4}$	I/O30
I/O10	GND	I/O13	I/O26	$\overline{WP}$	I/O29
A14	I/O11	I/O12	A7	I/O27	I/O28
A16	A10	$\overline{OE}$	A12	A4	A1
A11	A9	A17	VPP	A5	A2
A0	A15	$\overline{WE}$	A13	A6	A3
A18	VCC	I/O7	A8	A20	I/O23
I/O0	$\overline{CS1}$	I/O6	I/O16	$\overline{CS3}$	I/O22
I/O1	A19	I/O5	I/O17	GND	I/O21
I/O2	I/O3	I/O4	I/O18	I/O19	I/O20
11	22	33	44	55	66

PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-20	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$1-4	Chip Selects
$\overline{OE}$	Output Enable
$\overline{RP}$	Reset/Powerdown
Vcc	Power Supply
VPP	Program/Erase Supply
GND	Ground
$\overline{WP}$	Write Protect

BLOCK DIAGRAM

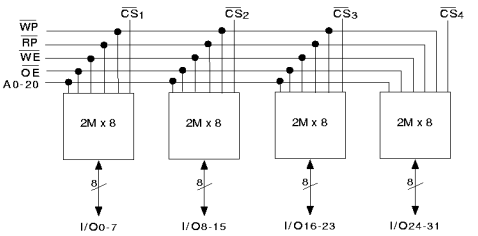
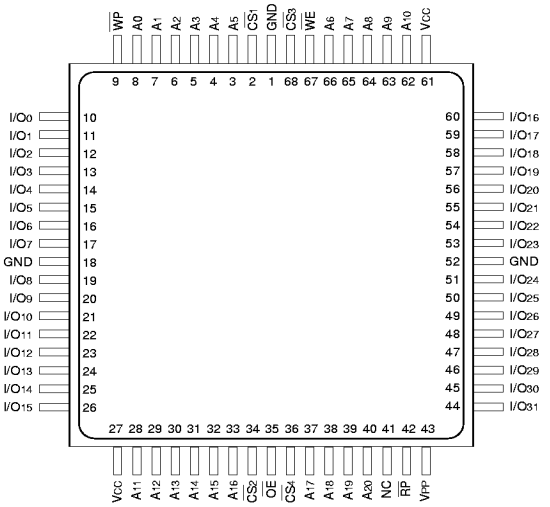


FIG. 2 PIN CONFIGURATION FOR WF2M32-XG4TX

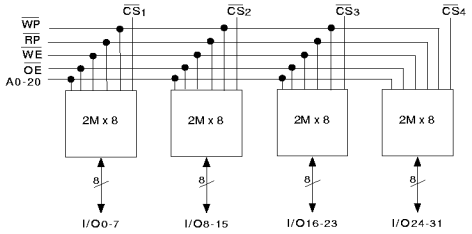
TOP VIEW



PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-20	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
$\overline{RP}$	Reset/Powerdown
Vcc	Power Supply
GND	Ground
VPP	Program/Erase Supply
$\overline{WP}$	Write Protect
NC	Not Connected

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Voltage on Anny Pin with Respect to GND (except Vcc and V_{PP})	-2.0 to +7.0	V
V_{PP} Program Voltage with Respect to GND during Block Erase/Byte Write	-0.2 to +14.0	V
Vcc Supply Voltage with Respect to GND	-0.2 to +7.0	V
Output Short Circuit Current	100	mA

NOTES:
1. Minimum DC voltage is -0.5V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <20nS. Maximum DC voltage on input/output pins is V_{CC} + 0.5V which, during transitions, may overshoot to V_{CC} + 2.0V for periods <20 nS.
2. Maximum DC voltage on V_{PP} may overshoot to +14.0V for periods <20 nS.
3. Output shorted for no more than one second. No more than one output shorted at a time.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a Stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.0	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	°C

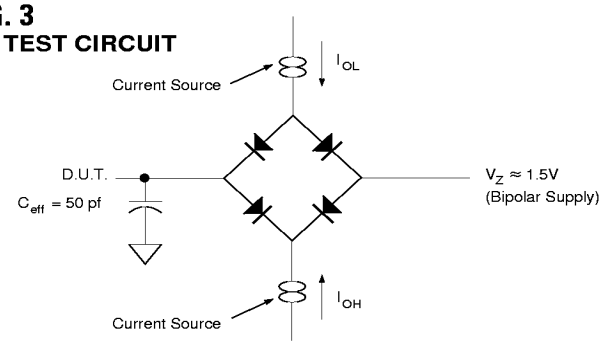
CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{OE}$ capacitance	C_{OE}	V_{IN} = 0 V, f = 1.0 MHz	50	pF
$\overline{WE}_{1-4}$ capacitance HIP (PGA) H2	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz	50	pF
CQFP G4T			50	
$\overline{CS}_{1-4}$ capacitance	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C_{AD}	V_{IN} = 0 V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

FIG. 3
AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	nS
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

DC CHARACTERISTICS - CMOS COMPATIBLE

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = Vcc to GND		10	µA
Output Leakage Current	I_{LO}	V_{CC} = 5.5, V_{OUT} = Vcc to GND		10	µA
Vcc Standby Current	I_{CCS}	V_{CC} = 5.5, $\overline{CS}$ = $\overline{RP}$ = $\overline{WP}$ = V_{IH}, f = 5MHz		16.0	mA
Vcc Read Current	I_{CCR}	V_{CC} = 5.5, $\overline{CS}$ = V_{IL}, f = 5 MHz, I_{OUT} = 0mA		175	mA
Vcc Write Current	I_{CCW}	Write in Progress		175	mA
Vcc Block Erase Current	I_{CCE}	Block Erase in Progress		60	mA
Vcc Powerdown Current	I_{CCD}	$\overline{RP}$ = GND		8	mA
V_{PP} Standby Current	I_{PPS}	V_{PP} < Vcc		80	µA
V_{PP} Powerdown Current	I_{PPD}	$\overline{RP}$ = GND		80	µA
V_{PP} Write Current	I_{PPW}	V_{PP} = V_{PPH}, Write in Progress		60	mA
V_{PP} Block Erase Current	I_{PPE}	V_{PP} = V_{PPH}, Block Erase in Progress		60	mA
Output Low Voltage	V_{OL}	V_{CC} = 4.5, I_{OL} = 5.8 mA		0.45	V
Output High Voltage	V_{OH}	V_{CC} = 4.5, I_{OH} = -2.5 mA	2.4		V
V_{PP} during Erase/Write Operations	V_{PPH}		11.4	12.6	V
Vcc Erase/Write Lock Voltage	V_{LKO}		2.0		V
V_{PPL} During Normal Operations	V_{PPL}		0.0	6.5	V

NOTES:
1. Block Erases/Writes are inhibited when V_{PP} = V_{PPL} and not guaranteed in the range between V_{PPL} and V_{PPH}.
2. DC test conditions V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V

AC CHARACTERISTICS – READ-ONLY OPERATIONS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol		-90		-100		-120		Unit
			Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	90		100		120		nS
Address Access Time	t_{AVQV}	t_{ACC}		90		100		120	nS
Chip Select to Output Valid (1)	t_{ELQV}	t_{CE}		90		100		120	nS
Output Enable to Output Valid (1)	t_{GLQV}	t_{OE}		40		40		45	nS
Chip Select to Output Low Z (2)	t_{ELQX}	t_{LZ}	0		0		0		nS
Chip Select High to Output High Z (2)	t_{EHQZ}	t_{HZ}		35		35		40	nS
Output Enable to Output Low Z (2)	t_{GLQX}	t_{OLZ}	0		0		0		nS
Reset to Output Valid (2)	t_{PHQV}	t_{PWH}		550		550		620	nS
Output Enable High to Output High Z(2)	t_{GHQZ}	t_{DF}		35		35		40	nS
Output Hold from Addresses, $\overline{CS}$ or $\overline{OE}$ Change, Whichever is First[2]	t_{OH}	t_{OH}	0		0		0		nS

NOTES:
1. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CS}$ without impact on t_{CS}.
2. Guaranteed by design, not tested.

AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS - $\overline{WE}$ CONTROLLED

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol		-90		-100		-120		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	90		100		120		nS
Chip Select Setup Time	t_{ELWL}	t_{CS}	0		0		0		nS
Write Enable Pulse Width	t_{WLWH}	t_{WP}	50		50		50		nS
V_{PP} Setup Time (1)	t_{VPWH}	t_{VPS}	100		100		100		nS
Address Setup to $\overline{WE}$ Going High	t_{AVWH}		50		50		50		nS
Data Setup Time	t_{DVWH}	t_{DS}	60		60		60		nS
Data Hold Time	t_{WHDX}	t_{DH}	0		0		0		nS
Address Hold Time	t_{WHAX}	t_{AH}	10		10		10		nS
Chip Select Hold Time	t_{WHEH}	t_{CH}	10		10		10		nS
Write Enable Pulse Width High	t_{WHWL}	t_{WPH}	50		50		50		nS
Duration of Byte Write Operation (1,2,3)	t_{WHQV1}		4.5		4.5		4.5		µS
Duration of Block Erase Operation (1,2,3)	t_{WHQV2}		0.3		0.3		0.3		Sec
Write Recovery before Read	t_{WHGL}		80		80		80		nS
$\overline{RP}$ High Recovery Time (1)	t_{PHWL}	t_{PS}	1		1		1		µS

NOTES:
1. Guaranteed by design, not tested.
2. The on-chip Write State Machine incorporates all byte write and block erase functions and overhead of the flash memory, this includes byte program and verify, block precondition and verify, erase and verify.
3. Byte write and block erase durations are measured to completion (SR. 7 = 1). V_{PP} should be held at V_{PPH} until determination of byte write/block erase success (SR.3/4/5 = 0).

AC CHARACTERISTICS – WRITE OPERATION - $\overline{CS}$ CONTROLLED (1)

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol		-90		-100		-120		Unit
			Min	Max	Min	Max	Min	Max	
Write Enable Cycle Time	t_{AVAV}	t_{WC}	90		100		120		nS
Write Enable Setup Time	t_{WLEL}	t_{WS}	0		0		0		nS
Chip Select Pulse Width	t_{ELEH}	t_{CP}	50		50		50		nS
V_{PP} Setup Time	t_{VPEH}	t_{VPS}	100		100		100		nS
Address Setup to $\overline{CS}$ Going High	t_{AVEH}		50		50		50		nS
Data Setup Time	t_{DVEH}	t_{DS}	60		60		60		nS
Data Hold Time	t_{EHDX}	t_{DH}	0		0		0		nS
Address Hold Time	t_{EHAX}	t_{AH}	10		10		10		nS
Write Enable Hold Time	t_{EHWH}	t_{WH}	10		10		10		nS
Chip Select Pulse Width High	t_{EHEL}	t_{EPH}	50		50		50		nS
Duration of Byte Write Operation (2, 3)	t_{EHQV1}		4.5		4.5		4.5		µS
Duration of Block Erase Operation (2, 3)	t_{EHQV2}		0.3		0.3		0.3		Sec
Write Recovery before Read	t_{EHGL}		80		80		80		nS
$\overline{RP}$ High Recovery to $\overline{CS}$ Low (2)	t_{PHEL}	t_{PS}	1		1		1		µS

NOTES:
1. Chip-Select Controlled Writes: Write operations are driven by the valid combination of $\overline{CS}$ and $\overline{WE}$. In systems where $\overline{CS}$ defines the write pulsewidth (within a longer $\overline{WE}$ timing waveform), all setup, hold and inactive $\overline{WE}$ times should be measured relative to the $\overline{CS}$ waveform.
2. Guaranteed by design, not tested.
3. Byte write and block erase durations are measured to completion (SR.7 = 1, V_{OH}). V_{PP} should be held at V_{PPH} until determination of byte write/block erase success (SR.3/4/5 = 0).

FIG. 4 AC WAVEFORMS FOR WRITE-ERASE-PROGRAM OPERATIONS, $\overline{WE}$ CONTROLLED

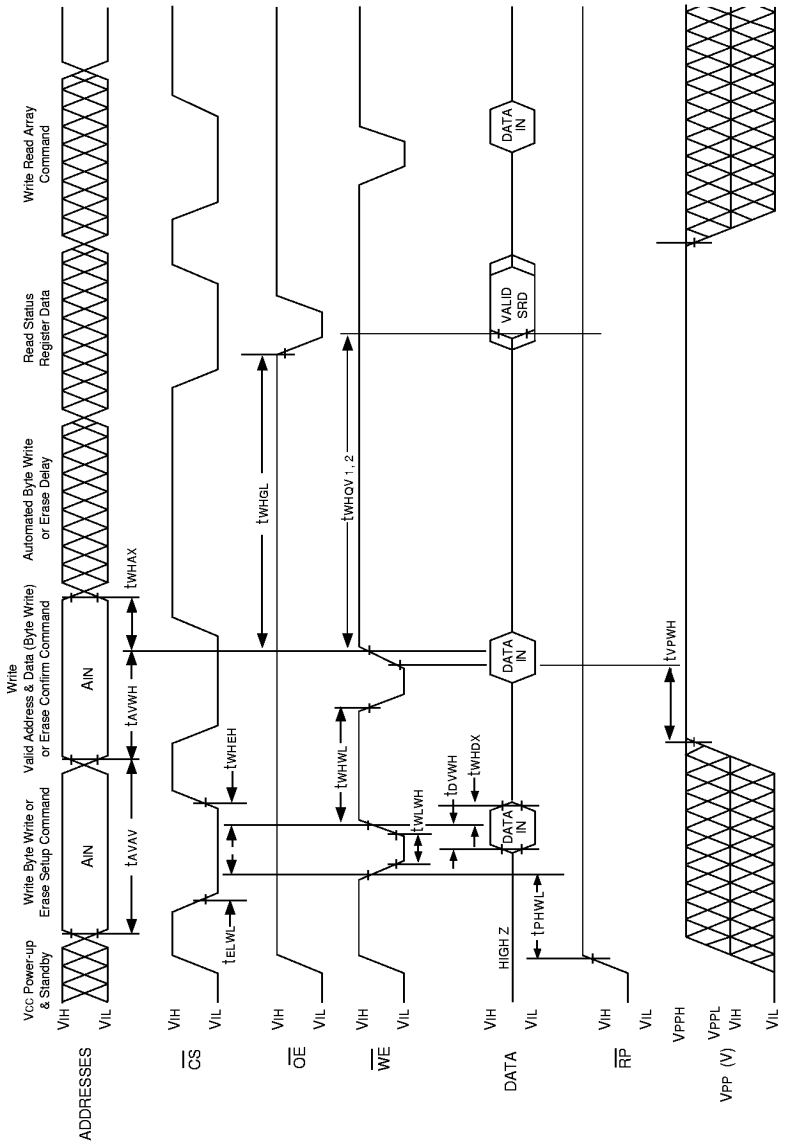


FIG. 5 ALTERNATE AC WAVEFORM FOR WRITE OPERATIONS - $\overline{CS}$ CONTROLLED

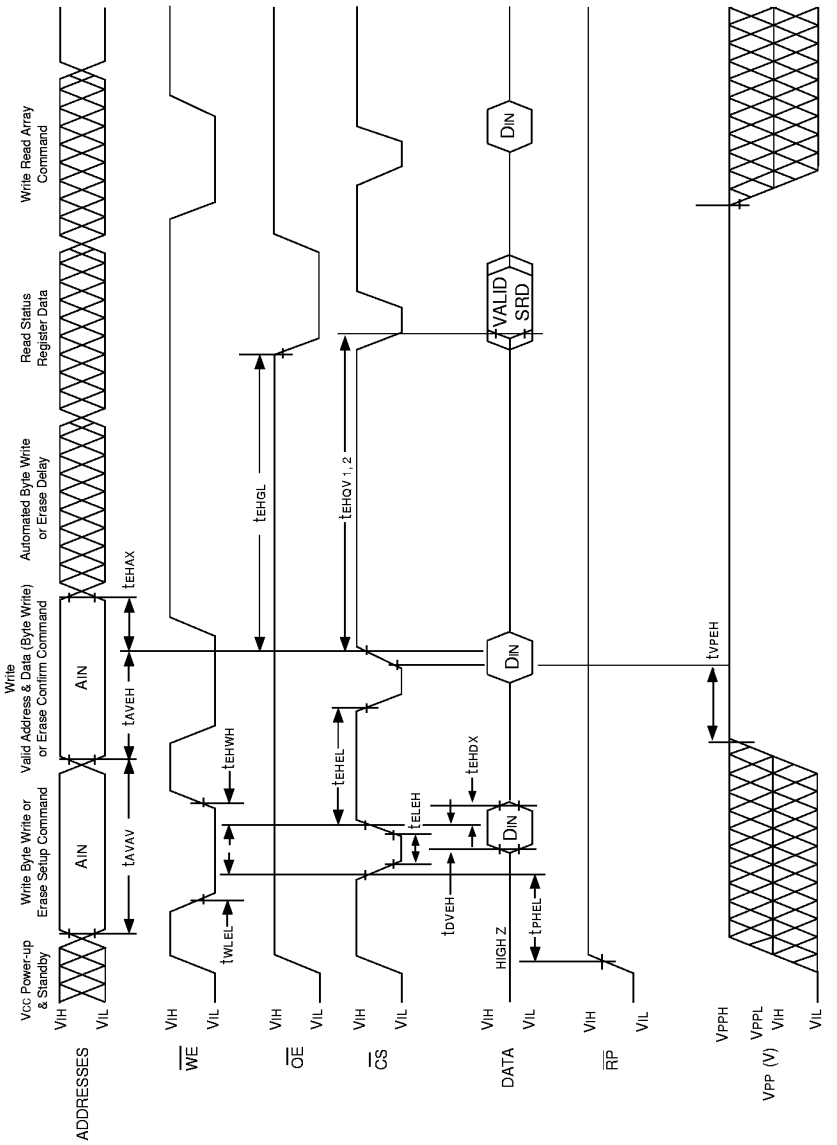
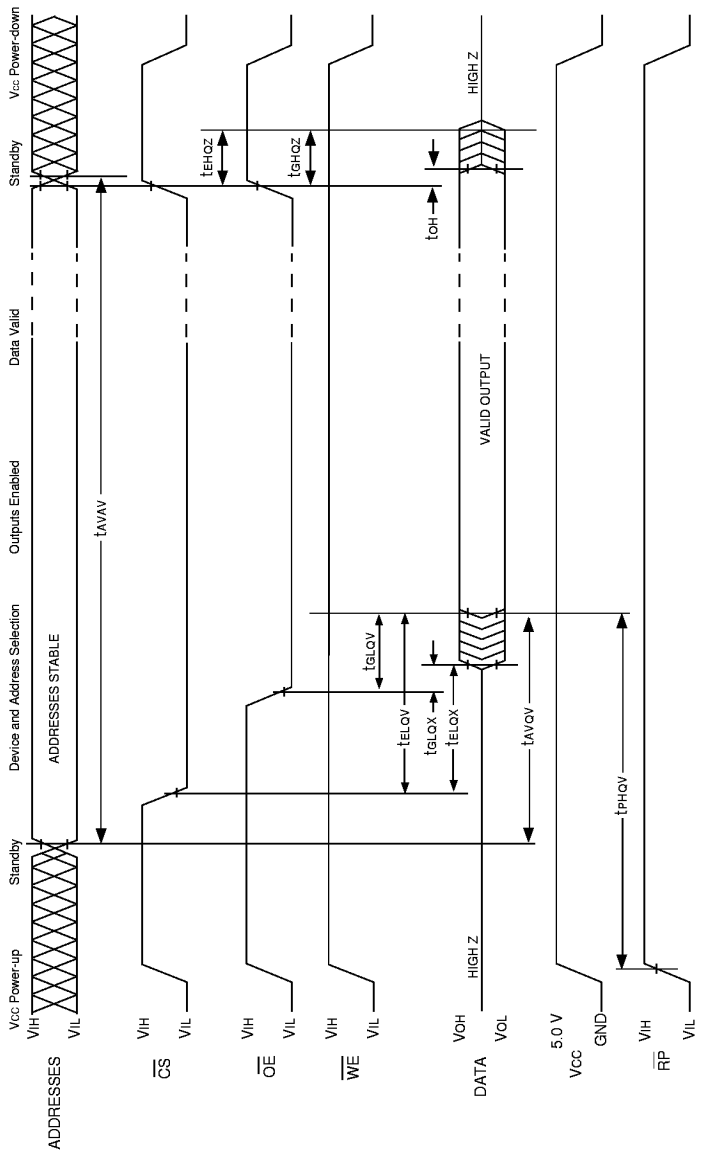


FIG. 6 AC WAVEFORM FOR READ OPERATIONS



PRINCIPLES OF OPERATION

The following Principles of Operation of the WF2M32-XXX MCM is applicable to each of the four memory chips inside the MCM. Chip 1 is distinguished by $\overline{CS_1}$ and I/O_{0-7}, Chip 2 by $\overline{CS_2}$ and I/O_{8-15}, Chip 3 by $\overline{CS_3}$ and I/O_{16-23}, and Chip 4 by $\overline{CS_4}$ and I/O_{24-31}.

The WF2M32-XXX includes write automation to manage write and erase functions. The Write State Machine allows for 100% TTL-level control inputs; fixed power supplies during block erasure and byte write; and minimal processor overhead with RAM-like interface timings.

After initial device powerup the WF2M32-XXX functions as a read-only memory. Manipulation of external memory-control pins allow array read, standby and output disable operations. The status register can also be accessed through the command user interface when $V_{PP} = V_{PPL}$.

This same subset of operations is also available when high voltage is applied to the V_{PP} pin. In addition, high voltage on V_{PP} enables successful block erasure and byte writing of the device. Functions associated with altering memory contents—byte write, block erase—are accessed via the command user interface and verified thru the status register.

Commands are written using standard microprocessor write timings. Command user interface contents serve as input to the write status machine, which controls the block erase and byte write circuitry. Write cycles also internally latch addresses and data needed for byte write or block erase operations.

Interface software to initiate and poll progress of internal byte write and block erase can be stored in any of the blocks. This code is copied to, and executed from, system RAM during actual flash memory update. After successful completion of byte write and/or block erase, code/data reads from the device are again possible via the read array command. Erase suspend/resume capability allows system software to suspend block erase to read data and execute code from any other block.

COMPARISON OF WF1M32 TO WF2M32

A Superset of commands have been added to the basic WF1M32-XXX (formerly WF1024K32-XXX) command-set to achieve higher write performance and provide additional capabilities. These new commands and features include:

- Page Buffer Writes to Flash
- Command Queuing Capability
- Automatic Data Writes During Erase
- Software Locking of Memory Blocks
- Two-Byte Successive Writes in 8-bit Systems
- Erase All Unlocked Blocks

A Block Erase operation erases one of the 32 blocks, which is about 65% improvement over the WF1M32-XXX.

Each block can be written and erased a minimum of 100,000 cycles (0°C to 70°C). Systems can achieve 1 million block erase cycles by providing wear-leveling algorithms and block retirement.

Each chip in WF2M32-XXX incorporates two page buffers of 256 Bytes (128 Words) each to allow page data writes. This feature can improve a system write performance by up to 4.8 times over previous flash memory devices.

All operations are started by a sequence of write commands to the device. Three Status Registers (described in detail later) and a $\overline{RY/BY}$ output pin provide information on the progress of the requested operation.

While the WF1M32 requires an operation to complete before the next operation can be requested, the WF2M32 allows queueing of the next operation while memory executes the current operation. This eliminates system overhead when writing several bytes in a row to the array or erasing several blocks at the same time. The WF2M32 can also perform write operations to one block of memory while performing erase of another block.

The WF2M32 provides user-selectable block locking to protect code or data. Each block has an associated nonvolatile lock-bit which determines the lock status of the block. In addition, the WF2M32 has a master Write Protect pin ($\overline{WP}$) which prevents any modifications to memory blocks whose lock-bits are set.

The WF2M32 contains three types of Status Registers to accomplish various functions:

- A Compatible Status Register (CSR) which is 100% compatible with the WF1M32 flash memory's Status Register. This register, when used alone, provides a straightforward upgrade capability to the WF2M32 from a WF1M32 based design.
- A Global Status Register (GSR) which informs the system of command queue status, page buffer status, and overall Write State Machine (WSM) status.
- 32 Block Status Registers (BSRs) which provide block-specific status information such as the block lock-bit status.

COMMAND USER INTERFACE AND WRITE AUTOMATION

An on-chip state machine controls block erase and byte write, freeing the system processor for other tasks. After receiving the Erase Setup and Erase Confirm commands, the state machine controls block preconditioning and erase, returning progress via the Status Register on each of the four memory chips in the MCM. Byte write is similarly controlled, after destination address and expected data are supplied.

DATA PROTECTION

Depending on the application, the system designer may choose to make the V_{PP} power supply switchable (available only when memory byte writes/block erases are required) or hardwired to V_{PPH}. When $V_{PP} = V_{PPL}$, memory contents cannot be altered. Additionally, all functions are disabled whenever V_{CC} is below the write lockout voltage V_{LKO} or when $\overline{RP}$ is at V_{IL}. The two-step byte write/block erase command user interface write sequence provides additional software write protection.

BUS OPERATION

Flash memory reads, erase and writes in-system via the local CPU. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

READ

The WF2M32-XXX can be read from any of its blocks, and information can be read from the status register of each chip selected. V_{PP} can be at either V_{PPL} or V_{PPH}.

The first task is to write the appropriate read mode command to the command user interface. The device automatically resets to read array mode upon initial device powerup or after exit from deep powerdown. Chip select $\overline{CS}$ is the device selection control, and when active enables the selected memory device. Output Enable ($\overline{OE}$) is the data input/output (I/O_0-I/O_{31}) direction control, and when active drives data from the select memory onto the I/O bus. $\overline{RP}$ and $\overline{WE}$ must also be at V_{IH}. Figure 6 illustrates read bus cycle waveforms.

OUTPUT DISABLE

With $\overline{OE}$ at a logic-high level (V_{IH}), the device outputs are disabled. Output pins (I/O_{0-31}) are placed in a high-impedance state.

STANDBY

$\overline{CS}$ at a logic-high level (V_{IH}) places the device in a standby mode. Standby operation disables much of the device's circuitry and substantially reduces device power consumption. The outputs (I/O_{0-31}) are placed in a high-impedance state independent of the status of $\overline{OE}$. If the device is deselected during block erase or byte write, it will continue functioning and consuming normal active power until the operation is completed.

WRITE

Writes to the command user interface enable reading of device data. They also control inspection and cleaning of the status register. Additionally, when $V_{PP} = V_{PPH}$, the command user interface controls block erasure and byte write. The contents of the interface register serve as input to the internal state machine.

The command user interface itself does not occupy an addressable memory location. The interface register is a latch used to store the command and address and data information needed to execute the command. Erase setup and erase confirm commands require both appropriate command data and an address within the block to be erased. The Byte Write Setup command requires both appropriate command data and the address of the location to be written, while the Byte Write command consists of the data to be written and the address of the location to be written.

The command user interface is written by bringing $\overline{WE}$ to a logic-low level (V_{IL}) while $\overline{CS}$ is low. Address and data are latched on the rising edge of $\overline{WE}$. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the AC Waveforms for Write Operation, Figures 4 and 5, for specific timing parameters.

COMMAND DEFINITIONS

When V_{PPL} is applied to the V_{PP} pin of the chip selected, read operations from the status register, or array blocks are enabled. Placing V_{PPH} on V_{PP} enables successful byte write and block erase operations as well.

Device operations are selected by writing specific commands into the command user interface of the chip selected. Table 2 defines the WF2M32-XXX commands.

READ ARRAY COMMAND

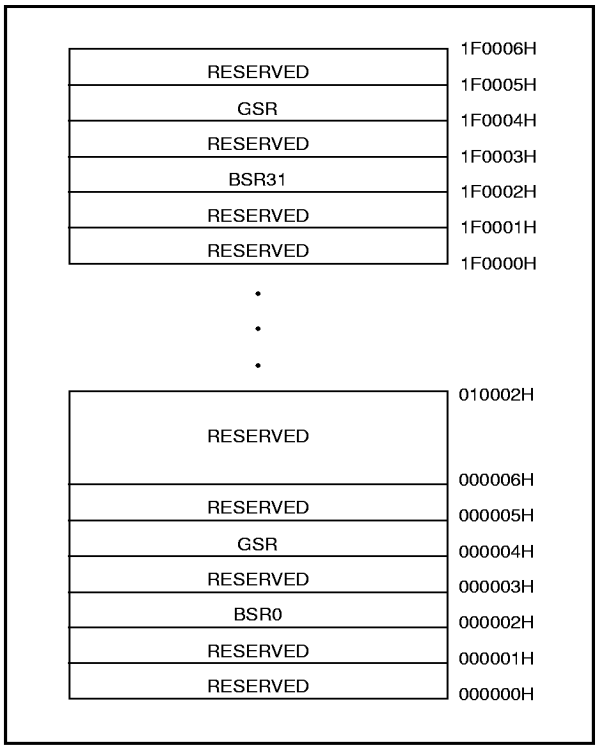
Upon initial device powerup the device defaults to Read Array mode. This operation is also initiated by writing FFH into the command user interface. Microprocessor read cycles retrieve array data. The device remains enabled for reads until the command user interface contents are altered. Once the internal Write State Machine has started a block erase or byte write operation, the device will not recognize the Read Array command, until the WSM has completed its operation. The Read Array command is functional when $V_{PP} = V_{PPL}$ or V_{PPH}.

TABLE 1 - BUS OPERATIONS

Mode	Notes	$\overline{RP}$	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O_{0-7}
Read		V_{IH}	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Output Disable		V_{IH}	V_{IL}	V_{IH}	V_{IH}	High Z
Standby	1	V_{IH}	V_{IL} V_{IH} V_{IH}	X	X	High Z
Deep Power-down	1,2	V_{IL}	X	X	X	High Z
Write	3	V_{IH}	V_{IL}	V_{IH}	V_{IL}	D_{IN}

NOTES:
1. X can be V_{IH} or V_{IL} for address or control pins.
2. $\overline{RP}$ at GND ±0.2V ensures the lowest deep power-down current.
3. Commands for different Erase operations, Data Write operations or Lock-Block operations can only be successfully completed when $V_{PP} = V_{PPH}$.

EXTENDED STATUS REGISTERS MEMORY MAP



NOTE: The above memory map is for each of the four memory chips in the WF2M32-XXX module.

TABLE 2 - COMMAND DEFINITIONS - COMPATIBLE MODE (with WF1M32-XXX)

Command	Notes	First Bus Cycle			Second Bus Cycle		
		Operation	Address	Data	Operation	Address	Data
Read Array		Write	X	FFH	Read	AA	AD
Read Compatible Status Register	1	Write	X	70H	Read	X	CSRD
Clear Status Register	2	Write	X	50H			
Word/Byte Write		Write	X	40H	Write	WA	WD
Alternate Word/Byte Write		Write	X	10H	Write	WA	WD
Block Erase/Confirm		Write	X	20H	Write	BA	DOH
Erase Suspend/Resume		Write	X	BOH	Write	X	DOH

ADDRESS
AA = Array Address
BA = Block Address
WA = Write Address
X = Don't Care

DATA
AD = Array Data
CSRD = CSR Data
WD = Write Data

NOTES:
1. The CSR is automatically available after device enters Data Write, Erase, or Suspend operations.
2. Clears CSR.3, CSR.4, CSR.5. Also clears GSR.5 and all BSR.5 and BSR.2 bits. See Status register definitions.

TABLE 3 - COMMAND DEFINITIONS - ENHANCED MODE

Command	Notes	First Bus Cycle			Second Bus Cycle			Third Bus Cycle		
		Operation	Address	Data	Operation	Address	Data	Operation	Address	Data
Read Extended Status Register	1	Write	X	71H	Read	RA	GSRD BSRD			
Page Buffer Swap	5	Write	X	72H						
Read Page Buffer		Write	X	75H	Read	PA	PD			
Single Load to Page Buffer		Write	X	74H	Write	PA	PD			
Sequential Load to Page Buffer	3,4,6	Write	X	E0H	Write	X	BCL	Write	X	BCH
Page Buffer Write to Flash	3,6	Write	X	0CH	Write	Ao	BC(L,H)	Write	WA	BC(H,L)
Two Byte Write		Write	X	FBH	Write	Ao	WD(L,H)	Write	WA	WD(H,L)
Lock Block/Confirm		Write	X	77H	Write	BA	D0H			
Upload Status Bits/Confirm	2	Write	X	97H	Write	X	D0H			
Upload Device Information		Write	X	99H	Write	X	D0H			
Erase All Unlocked Blocks/Confirm		Write	X	A7H	Write	X	D0H			
Sleep		Write	X	F0H						
Abort		Write	X	80H						

ADDRESS
BA = Block Address
PA = Page Buffer Address
RA = Extended Register Address
WA = Write Address
X = Don't Care

DATA
AD = Array Data
PD = Page Buffer Data
BSRD = BSR Data
GSRD = GSR Data
BC(L,H) = Byte Count (Low, High)
WD(L,H) = Write Data (Low, High)

NOTES:
1. RA can be the GSR address or any BSR address.
2. Upon device power-up, all BSR lock-bits come up locked. The Upload Status Bits command must be written to reflect the actual lock-bit status.
3. BCH/WCH must be at 00H for this product because of the 256-Byte (128 Word) Page Buffer size and to avoid writing the Page Buffer contents into more than one 256-Byte segment within an array block. They are simply shown for future Page Buffer expandability.
4. PA and PD (whose count is given in cycles 2 and 3) are supplied starting in the 4th cycle which is not shown.
5. This command allows the user to swap between available Page Buffers (0 or 1).
6. BCL = 00H corresponds to a Byte count of 1. Similarly, WCL = 00H corresponds to a Word count of 1.

TABLE 4
COMPATIBLE STATUS REGISTER

WSMS	ESS	ES	DWS	VPPS	R	R	R
7	6	5	4	3	2	1	0

CSR.7 = WRITE STATE MACHINE STATUS
1 = Ready
0 = Busy
CSR.6 = ERASE-SUSPEND STATUS
1 = Erase Suspended
0 = Erase in Progress/Completed
CSR.5 = ERASE STATUS
1 = Error in Block Erasure
0 = Successful Block Erase
CSR.4 = DATA WRITE STATUS
1 = Error in Data Write
0 = Data Write Successful
CSR.3 = V_{PP} STATUS
1 = V_{PP} Low Detect; Operation Abort
0 = V_{PP} OK
CSR.2-0 = RESERVED FOR FUTURE ENHANCEMENTS
These bits are reserved for future use and should be masked out when polling the CSR.

NOTES:
1. WSMS bit must be checked to determine completion of an operation (Erase Suspend, Erase or Data Write) before the appropriate Status bit (ESS, ES or DWS) is checked for success.
2. If DWS and ES are set to "1" during an erase attempt, an improper command sequence was entered. Clear the CSR and attempt the operation again.
3. The V_{PPS} bit, unlike an A/D converter, does not provide continuous indication of V_{PP} level. The WSM interrogates the V_{PP}'s level only after the data write or erase command sequences have been entered, and informs the system if V_{PP} has not been switched on. The V_{PPS} is not guaranteed to report accurate feedback between V_{PPL} and V_{PPH}.

READ STATUS REGISTER COMMAND

Each chip of the WF2M32-XXX contains a status register which may be read to determine when a byte write or block erase operation is complete, and whether that operation completed successfully. The status register may be read at any time by writing the read status register command (70H) to the command user interface. After writing this command, all subsequent read operations output data from the status register, until another valid command is written to the command user interface. The contents of the status register are latched on the falling edge of $\overline{OE}$ or $\overline{CS}$, whichever occurs last in the read cycle. $\overline{OE}$ or $\overline{CS}$ must be toggled to V_{IH} before further reads to update the status register latch. The read status register command functions when $V_{PP} = V_{PPL}$ or V_{PPH}.

CLEAR STATUS REGISTER COMMAND

The erase status and byte write status bits are set to "1"s by the Write State Machine on each chip and can only be reset by the clear status register command. These bits indicate various failure conditions (see Table 4). By allowing system software to control the resetting of these bits, several operations may be performed (such as cumulatively writing several bytes or erasing multiple blocks in sequence). The status register may then be polled to determine if an error occurred during that sequence. This adds flexibility to the way the device may be used.

Additionally, the V_{PP} Status bit (CSR.3) of the chip selected MUST be reset by system software before further byte writes or block erases are attempted. To clear the status register, the clear status register command (50H) is written to the command user interface. The clear status register command is functional when $V_{PP} = V_{PPL}$ or V_{PPH}.

ERASE SETUP/ERASE CONFIRM COMMANDS

Erase is executed one block at a time, initiated by a two-cycle command sequence. An erase setup command (20H) is first written to the command user interface, followed by the Erase Confirm command (DOH). These commands require both appropriate sequencing and address within the block to be erased to FFH. Block preconditioning, erase and verify are all handled internally by the Write State Machine, invisible to the system. After the two command erase sequence is written to it, the WF2M32-XXX automatically outputs status register data when read (see Figure 8; Block Erase Algorithm). The CPU can detect the completion of the erase event by analyzing the output of the WSM Status bit of the status register.

When erase is completed, the Erase Status bit should be checked. If erase error is detected, the status register should be cleared. The command user interface remains in read status register mode until further commands are issued to it.

This two-step sequence of setup followed by execution ensures that memory contents are not accidentally erased. Also, reliable block ensure can only occur when $V_{PP} = V_{PPH}$. In the absence of this high voltage, memory contents are protected against erasure. If block erase is attempted while $V_{PP} = V_{PPL}$, the V_{PP} status bit will be set to "1". Erase attempts while $V_{PPL} < V_{PP} < V_{PPH}$ produce spurious results and should not be attempted.

TABLE 5
GLOBAL STATUS REGISTER

WSMS	OSS	DOS	DSS	QS	PBAS	PBS	PBSS
7	6	5	4	3	2	1	0

GSR.7 = WRITE STATE MACHINE STATUS
- 1 = Ready
- 0 = Busy

GSR.6 = OPERATION SUSPEND STATUS
- 1 = Operation Suspended
- 0 = Operation in Progress/Completed

GSR.5 = DEVICE OPERATION STATUS
- 1 = Operation Unsuccessful
- 0 = Operation Successful or Currently Running

GSR.4 = DEVICE SLEEP STATUS
- 1 = Device in Sleep
- 0 = Device Not in Sleep

MATRIX 5/4
- 00 = Operation Successful or Currently Running
- 01 = Device in Sleep Mode or Pending Sleep
- 10 = Operation Unsuccessful
- 11 = Operation Unsuccessful or Aborted

GSR.3 = QUEUE STATUS
- 1 = Queue Full
- 0 = Queue Available

GSR.2 = PAGE BUFFER AVAILABLE STATUS
- 1 = One or Two Page Buffers Available
- 0 = No Page Buffer Available

GSR.1 = PAGE BUFFER STATUS
- 1 = Selected Page Buffer Ready
- 0 = Selected Page Buffer Busy

GSR.0 = PAGE BUFFER SELECT STATUS
- 1 = Page Buffer 1 Selected
- 0 = Page Buffer 0 Selected

NOTES:
1. WSMS bit must be checked to determine completion of an operation (Block Lock, Suspend, Upload Status Bits, Erase or Data Write) before the appropriate Status bit (OSS or DOS) is checked for success.
2. If operation currently running, then GSR.7 = 0.
3. If device pending sleep, then GSR.7 = 0.
4. Operation aborted: Unsuccessful due to Abort command.
5. The device contains two Page Buffers.
6. Selected Page Buffer is currently busy with WSM operation.

NOTE:
1. When multiple operations are queued, checking BSR.7 only provides indication of completion for that particular block. GSR.7 provides indication when all queued operations are completed.

BYTE WRITE SETUP/WRITE COMMANDS

Byte write is executed by a two-command sequence. The byte write setup command (40H) is written to the command user interface of the chip selected, followed by a second write specifying the address and data (latched on the rising edge of $\overline{WE}$) to be written. The WSM then takes over, controlling the byte write and write verify algorithms internally. After the two-command byte write sequence is written to it, the device automatically outputs status register data when read (see Figure 7; Byte Write Algorithm). The CPU can detect the completion of the byte write event by analyzing the output of the WSM Status bit of the status register. Only the read status register command is valid while byte write is active.

When byte write is complete, the byte write status bit should be checked. If byte write error is detected, the status register should be cleared. The internal WSM verify only detects errors for "1"s that do not successfully write to "0"s. The command user interface remains in read status register mode until further commands are issued to it. If byte write is attempted while $V_{PP} = V_{PPL}$, the V_{PP} status bit will be set to "1". Byte write attempts while $V_{PPL} < V_{PP} < V_{PPH}$ produce spurious results and should not be attempted.

TABLE 6
BLOCK STATUS REGISTER

BS	BLS	BOS	BOAS	QS	VPPS	R	R
7	6	5	4	3	2	1	0

BSR.7 = BLOCK STATUS
- 1 = Ready
- 0 = Busy

BSR.6 = BLOCK-LOCK STATUS
- 1 = Block Unlocked for Write/Erase
- 0 = Block Locked for Write/Erase

BSR.5 = BLOCK OPERATION STATUS
- 1 = Operation Unsuccessful
- 0 = Operation Successful or Currently Running

BSR.4 = BLOCK OPERATION ABORT STATUS
- 1 = Operation Aborted
- 0 = Operation Not Aborted

MATRIX 5/4
- 00 = Operation Successful or Currently Running
- 01 = Not a Valid Combination
- 10 = Operation Unsuccessful
- 11 = Operation Aborted

BSR.3 = QUEUE STATUS
- 1 = Queue Full
- 0 = Queue Available

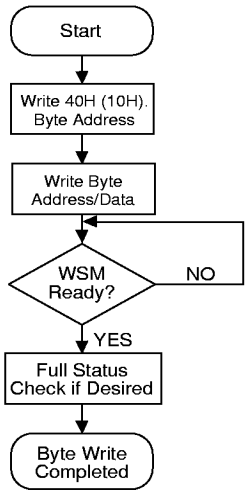
BSR.2 = V_{PP} STATUS
- 1 = V_{PP} Low Detect, Operation Abort
- 0 = V_{PP} OK

BSR.1-0 = RESERVED FOR FUTURE ENHANCEMENTS

NOTES:
1. BS must be checked to determine completion of an operation (Block Lock, Suspend, Erase or Data Write) before the appropriate Status bit (BOS, BLS) is checked for success.
2. The BOAS bit will not be set until BSR.7 = 1.
3. Operation halted via Abort command.
4. These bits are reserved for future use; mask them out when polling the BSRs.

NOTE:
1. When multiple operations are queued, checking BSR.7 only provides indication of completion for that particular block. GSR.7 provides indication when all queued operations are completed.

FIG. 7
AUTOMATED BYTE WRITE ALGORITHM



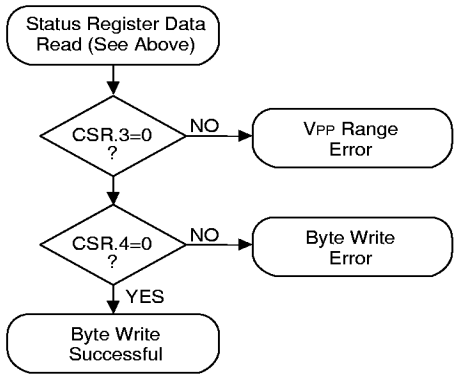
Bus Operation	Command	Comments
Write	Byte Write Setup	Data = 40H (10H) Address = Byte to be Written
Write	Byte Write	Data to be written Address = Byte to be Written
Standby/Read		Check WSMS bit V_{OH} = Ready, V_{OL} = Busy or Read Status Register Check CSR.7 1 = Ready, 0 = Busy Toggle $\overline{OE}$ or $\overline{CS}$ to update Status Register

Repeat for subsequent bytes

Full status check can be done after each byte or after a sequence of bytes

Write FFH after the last byte write operation to reset the device to Ready Array Mode

FULL STATUS CHECK PROCEDURE



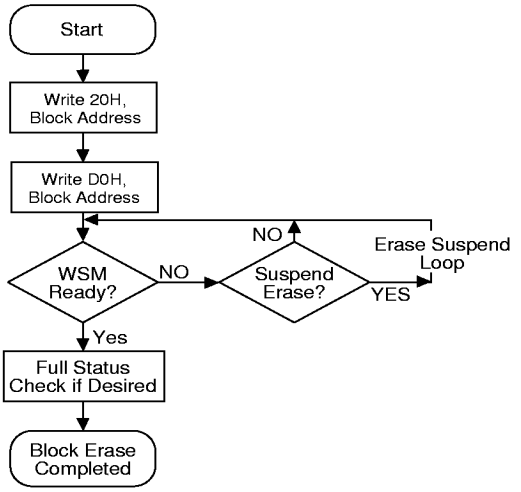
Bus Operation	Command	Comments
Optional Read		CPU may already have read Status Register data in WSM Ready polling above
Standby		Check CSR.3 1 = V_{PP} Low Detect
Standby		Check CSR.4 Both 1 = Byte Write Error

CSR.3 MUST be cleared, if set during a block erase attempt, before further attempts are allowed by the Write State Machine.

CSR.4 is only cleared by the clear status register command, in cases where multiple bytes are written before full status is checked.

If error is detected, clear the status register before attempting retry or other error recovery.

FIG. 8
AUTOMATED BLOCK ERASE ALGORITHM



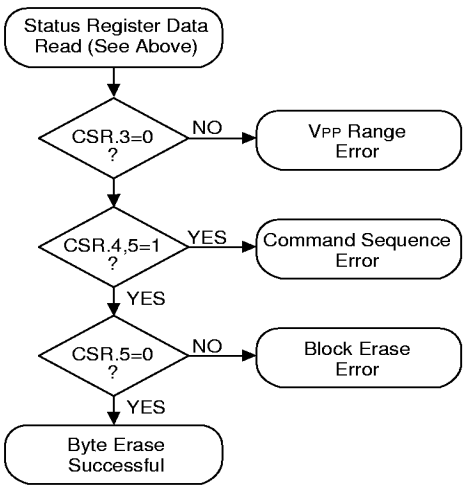
Bus Operation	Command	Comments
Write	Erase Setup	Data = 20H Address = Within block to be erased
Write	Erase	Data = D0H Address = Within block to be erased
Standby/Read		Check WSMS bit V_{OH} = Ready, V_{OL} = Busy or Read Compatible Status Register Check CSR.7 1 = Ready, 0 = Busy Toggle $\overline{OE}$ or $\overline{CS}$ to update Compatible Status Register

Repeat for subsequent bytes

Full status check can be done after each byte or after a sequence of bytes

Write FFH after the last byte write operation to reset the device to Ready Array Mode

FULL STATUS CHECK PROCEDURE



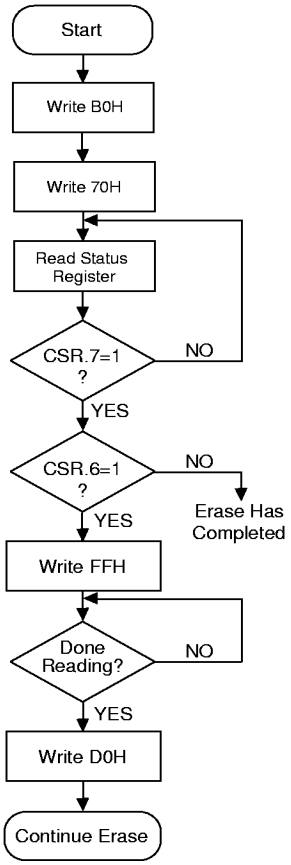
Bus Operation	Command	Comments
Optional Read		CPU may already have read Compatible Status Register data in WSM Ready polling above
Standby		Check CSR.3 1 = V_{PP} Low Detect
Standby		Check CSR.4, 5 Both 1 = Command Sequence Error
Standby		Check CSR.5 1 = Block Erase Error

CSR.3 MUST be cleared, if set during a block erase attempt, before further attempts are allowed by the Write State Machine.

CSR.5 is only cleared by the clear status register command, in cases where multiple bytes are written before full status is checked.

If error is detected, clear the status register before attempting retry or other error recovery.

FIG. 9
ERASE SUSPEND/RESUME ALGORITHM



Bus Operation	Command	Comments
Write	Erase Suspend	Data = B0H
Write	Read Status Register	Data = 70H
Standby/Read		Read Compatible Status Register
		Check CSR.7 1 = Ready, 0 = Busy Toggle $\overline{OE}$ or $\overline{CS}$ to update Status Register
Standby		Check CSR.6 1 = Suspended
Write	Read Array	Data = FFH
Read		Read array data from block other than that being erased.
Write	Erase Resume	Data = D0H

ERASE SUSPEND/ERASE RESUME COMMANDS

The erase suspend command allows block erase interruption in order to read data from another block of memory. Once the erase process starts, writing the erase suspend command (B0H) to the command user interface requests that the WSM suspend the erase sequence at a predetermined point in the erase algorithm. The WF2M32-XXX continues to output status register data when read, after the erase suspend command is written to it. Polling the WSM status and erase suspend status bits will determine when the erase operation has been suspended (both will be set to "1").

At this point, a read array command can be written to the command user interface to read data from blocks other than that which is suspended. The only other valid commands at this time are read status register (70H) and erase resume (D0H), at which time the WSM will continue with the erase process. The erase suspend status and WSM status bits of the status register will be automatically cleared. After the erase resume command is written to it, the device automatically outputs status register data when read (see Figure 9). V_{PP} must remain at V_{PPH} while in erase suspend.

V_{CC}, V_{PP}, RP TRANSITIONS AND THE COMMAND/STATUS REGISTERS

Byte write and block erase completion are not guaranteed if V_{PP} drops below V_{PPH}. If the V_{PP} Status bit of the Status Register (SR.3) is set to "1", a Clear Status Register command MUST be issued before further byte write/block erase attempts are allowed by the WSM. Otherwise, the Byte Write (SR.4) or Erase (SR.5) Status bits of the Status Register will be set to "1"s if error is detected. RP transitions to V_{IL} during byte write and block erase also abort the operations. Data is partially altered in either case, and the command sequence must be repeated after normal operation is restored. Device poweroff, or RP transitions to V_{IL}, clear the Status Register to initial value 10000 for the upper 5 bits.

The Command User Interface latches commands as issued by system software and is not altered by V_{PP} or $\overline{CS}$ transitions or WSM actions. Its state upon powerup, after exit from deep powerdown or after V_{CC} transitions below V_{LKO}, is Read Array Mode.

After byte write or block erase is complete, even after V_{PP} transitions down to V_{PPL}, the Command User interface must be reset to Read Array mode via the Read Array command if access to the memory array is desired.

POWER UP/DOWN PROTECTION

The WF2M32-XXX is designed to offer protection against accidental block erasure or byte writing during power transitions. Upon power-up, the device is indifferent as to which power supply, V_{PP} or V_{CC}, powers up first. Power supply sequencing is not required. Internal circuitry in the device ensures that the Command User interface is reset to the Read Array mode on power up.

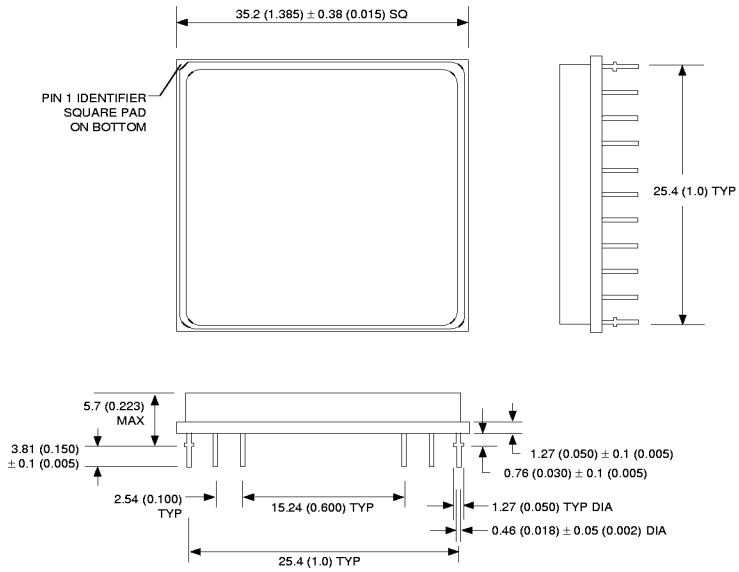
POWERDOWN AND RESET

The WF2M32-XXX offers a deep power-down feature, entered when $\overline{RP}$ is a V_{IL}. During read modes, RP-low deselects the memory, places output drivers in a high-impedance state and turns off all internal circuits. The device requires time t_{PWH} (see AC Characteristics-Read-Only Operations) after return from powerdown until initial memory access outputs are valid. After this wakeup interval, normal operation is restored. The Command User Interface is reset to Read Array, and the upper 5 bits of the Status Register are cleared to value 10000, upon return to normal operation.

During block erase or bytewrite modes. $\overline{RP}$ low will abort either operation. Memory contents of the block being altered are no longer valid as the data will be partially written or erased. Time t_{PS} after $\overline{RP}$ goes to logic-high (V_{IH}) is required before another command can be written.

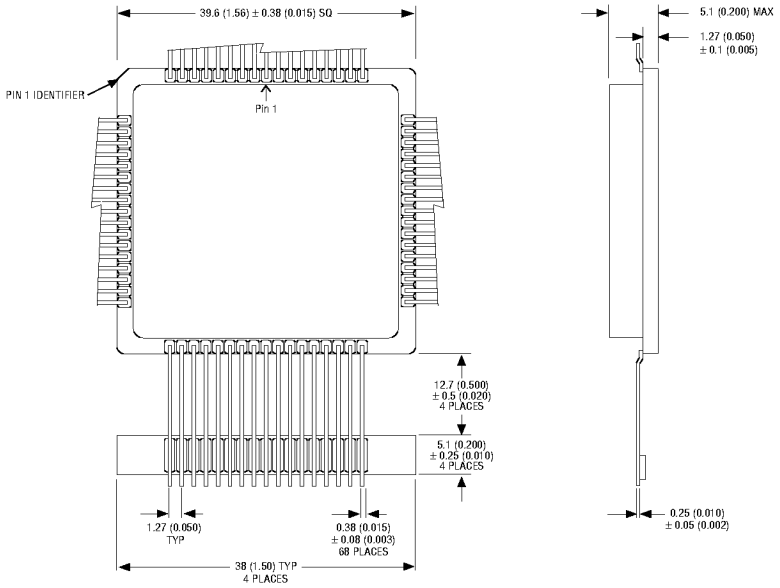
This use of $\overline{RP}$ during system reset is important with automated write/erase devices. When the system comes out of reset it expects to read from the flash memory. Automated flash memories provide status information when accessed during write/erase modes. If a CPU reset occurs with no flash memory reset, proper CPU initialization would not occur because the flash memory would be providing the status information instead of array data. These flash memories allow proper CPU initialization following a system reset through the use of the $\overline{RP}$ input. In this application $\overline{RP}$ is controlled by the same $\overline{RESET}$ signal that resets the system CPU.

PACKAGE 402: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H2)



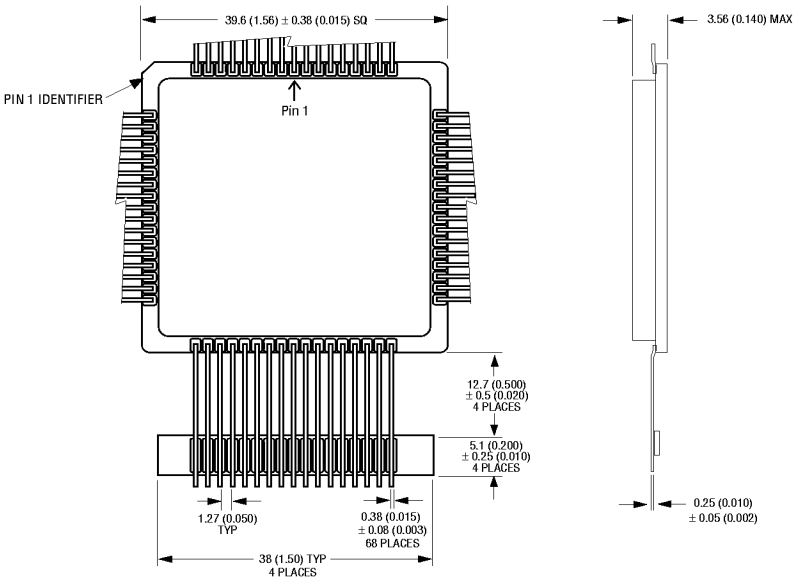
ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 501: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G4)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 502: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G4T)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W F 2M32 - XXX X X

V_{PP} PROGRAMMING VOLTAGE
Blank = 12V

DEVICE GRADE:
M = Military Screened -55°C to +125°C
I = Industrial -40°C to +85°C
C = Commercial 0 to +70°C

PACKAGE TYPE:
H2 = Ceramic Hex In line Package, HIP (Package 402)
G4T = 40mm Ceramic Quad Flat Pack, Low Profile CQFP (Package 502)

ACCESS TIME in nS

ORGANIZATION, 2M x 32
User configurable as 4M x 16 or 8M x 8

Flash PROM

WHITE MICROELECTRONICS