



Solid State Devices, Inc.

14701 Firestone Blvd * La Mirada, Ca 90638
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SFF116N10M SFF116N10Z

116 AMP , 100 Volts, 15 mΩ Avalanche Rated N-channel MOSFET

DESIGNER'S DATA SHEET

Part Number / Ordering Information ^{1/}
SFF116N10

— = Not Screened
 TX = TX Level
 TXV = TXV Level
 S = S Level

— = Straight Leads
 DB = Down Bend
 UB = Up Bend

M = TO-254
 Z = TO-254Z

Screening ^{2/}

Lead Option ^{3/}

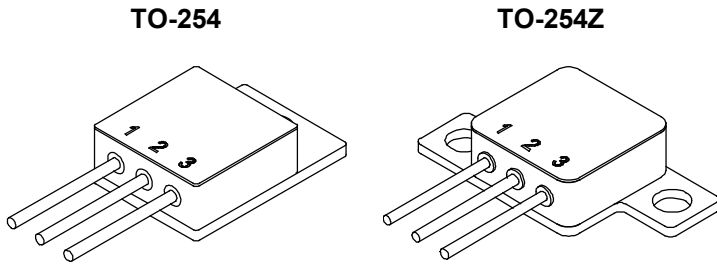
Package ^{3/ 4/}

- Features:**
- Rugged poly-Si gate
 - Lowest ON-resistance in the industry
 - Avalanche rated
 - Hermetically Sealed, Isolated Package
 - Low Total Gate Charge
 - Fast Switching
 - TX, TXV, S-Level screening available
 - Improved ($R_{DS(ON)}$ Q_G) figure of merit

Maximum Ratings		Symbol	Value	Units
Drain - Source Voltage		V_{DSS}	100	V
Gate – Source Voltage	continuous transient	V_{GS}	± 20 ± 30	V
Max. Continuous Drain Current (package limited)	@ $T_C = 25^\circ C$	I_{D1}	55	A
Max. Instantaneous Drain Current (Tj limited)	@ $T_C = 25^\circ C$	I_{D2}	116	A
	@ $T_C = 175^\circ C$	I_{D3}	80	A
Max. Avalanche current	@ L= 0.1 mH	I_{AR}	60	A
Single and Repetitive Avalanche Energy	@ L= 0.1 mH	E_{AS}	2500	mJ
		E_{AR}	80	
Total Power Dissipation	@ $T_C = 25^\circ C$	P_D	150	W
Operating & Storage Temperature		T_{OP} & T_{STG}	-55 to +175	$^\circ C$
Maximum Thermal Resistance (Junction to Case)		$R_{\theta JC}$	1.0 (typ.0.75)	$^\circ C / W$

NOTES:

- *Pulse Test: Pulse Width = 300μsec, Duty Cycle = 2%.
- 1/ For ordering information, price, and availability - contact factory.
- 2/ Screening based on MIL-PRF-19500. Screening flows available on request.
- 3/ For package outlines / lead bending options / pinout configurations - contact factory.
- 4/ Maximum current limited by package configuration
- 5/ Unless otherwise specified, all electrical characteristics @25°C.





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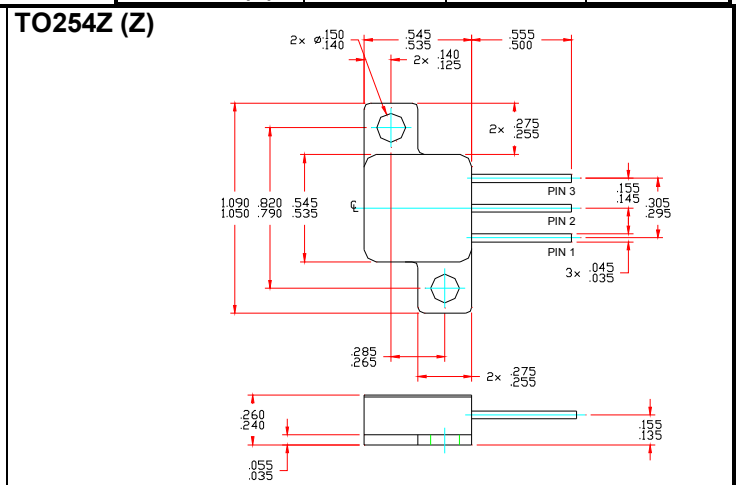
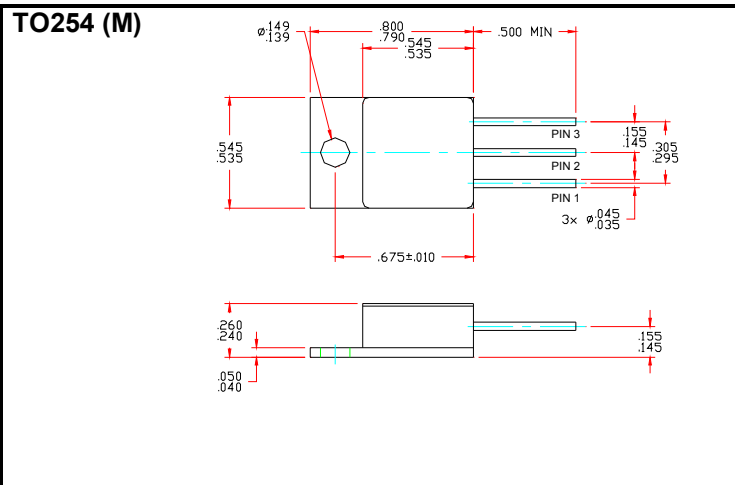
SFF116N10M SFF116N10Z

Electrical Characteristics ^{5/}	Symbol	Min	Typ	Max	Units
Drain to Source Breakdown Voltage $V_{GS} = 0V, I_D = 250\mu A$	BV_{DSS}	100	110	—	V
Drain to Source On State Resistance $V_{GS} = 10V, I_D = 50A, T_j = 25^\circ C$ $V_{GS} = 10V, I_D = 50A, T_j = 125^\circ C$ $V_{GS} = 10V, I_D = 50A, T_j = 150^\circ C$	$R_{DS(on)}$	— — —	10 16 20	15 25 —	mΩ
Gate Threshold Voltage $V_{DS} = V_{GS}, I_D = 1.0mA, T_j = 25^\circ C$ $V_{DS} = V_{GS}, I_D = 1.0mA, T_j = 125^\circ C$ $V_{DS} = V_{GS}, I_D = 1.0mA, T_j = -55^\circ C$	$V_{GS(th)}$	3.0 2.0 —	4.5 3.5 5.0	5.0 — 6	V
Gate to Source Leakage $V_{GS} = \pm 20V, T_j = 25^\circ C$ $V_{GS} = \pm 20V, T_j = 125^\circ C$	I_{GSS}	— —	10 30	±100 —	nA
Zero Gate Voltage Drain Current $V_{DS} = 100V, V_{GS} = 0V, T_j = 25^\circ C$ $V_{DS} = 100V, V_{GS} = 0V, T_j = 125^\circ C$ $V_{DS} = 100V, V_{GS} = 0V, T_j = 175^\circ C$	I_{DSS}	— — —	0.01 2.5 25	25 250 —	μA μA μA
Forward Transconductance $V_{DS} = 15V, I_D = 35A, T_j = 25^\circ C$	g_{fs}	10	60	—	Mho
Total Gate Charge $V_{GS} = 12V$	Q_g	—	125	250	nC
Gate to Source Charge $V_{DS} = 35V$	Q_{gs}	—	35	75	nC
Gate to Drain Charge $I_D = 50A$	Q_{gd}	—	65	120	
Turn on Delay Time $V_{GS} = 11V$	$t_{d(on)}$	—	39	50	nsec
Rise Time $V_{DS} = 50V$	t_r	—	67	80	
Turn off Delay Time $I_D = 35A$	$t_{d(off)}$	—	80	100	
Fall Time $R_G = 2.35\Omega, pw = 3\mu s$	t_f	—	67	80	
Diode Forward Voltage $I_F = 35A, V_{GS} = 0V$	V_{SD}	—	0.82	1.2	V
Diode Reverse Recovery Time $I_F = 50A, di/dt = 100A/\mu sec$	t_{rr}	—	240	300	nsec
Reverse Recovery Charge	Q_{rr}	—	0.85	—	μC
Input Capacitance $V_{GS} = 0V$	C_{iss}	—	4800	—	pF
Output Capacitance $V_{DS} = 25V$	C_{oss}	—	2050	—	
Reverse Transfer Capacitance $f = 1 MHz$	C_{rss}	—	600	—	

Available Part Numbers:

Consult Factory

PIN ASSIGNMENT (Standard)			
Package	Drain	Source	Gate
TO-254 (M)	Pin 1	Pin 2	Pin 3
TO-254Z (Z)	Pin 1	Pin 2	Pin 3



NOTE: All specifications are subject to change without notification. SCD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: FT0037B

DOC