



PI74FCT16823T PI74FCT162823T PI74FCT162H823T

Fast CMOS 18-Bit Registers

Product Features:

Common Features:

- PI74FCT16823T and PI74FCT162823T are high-speed, low power devices with high current drive.
- $V_{CC} = 5V \pm 10\%$
- Hysteresis on all inputs
- Packages available:
 - 56-pin 240 mil wide plastic TSSOP (A)
 - 56-pin 300 mil wide plastic SSOP (V)

PI74FCT16823T Features:

- High output drive: $I_{OH} = -32 \text{ mA}$; $I_{OL} = 64 \text{ mA}$
- Power off disable outputs permit “live insertion”
- Typical V_{OLP} (Output Ground Bounce) $< 1.0V$ at $V_{CC} = 5V$, $T_A = 25^\circ C$

PI74FCT162823T Features:

- Balanced output drivers: $\pm 24 \text{ mA}$
- Reduced system switching noise
- Typical V_{OLP} (Output Ground Bounce) $< 0.6V$ at $V_{CC} = 5V$, $T_A = 25^\circ C$

PI74FCT162H823T Features:

- Bus Hold retains last active bus state during 3-state
- Eliminates the need for external pull-up resistors

Product Description

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

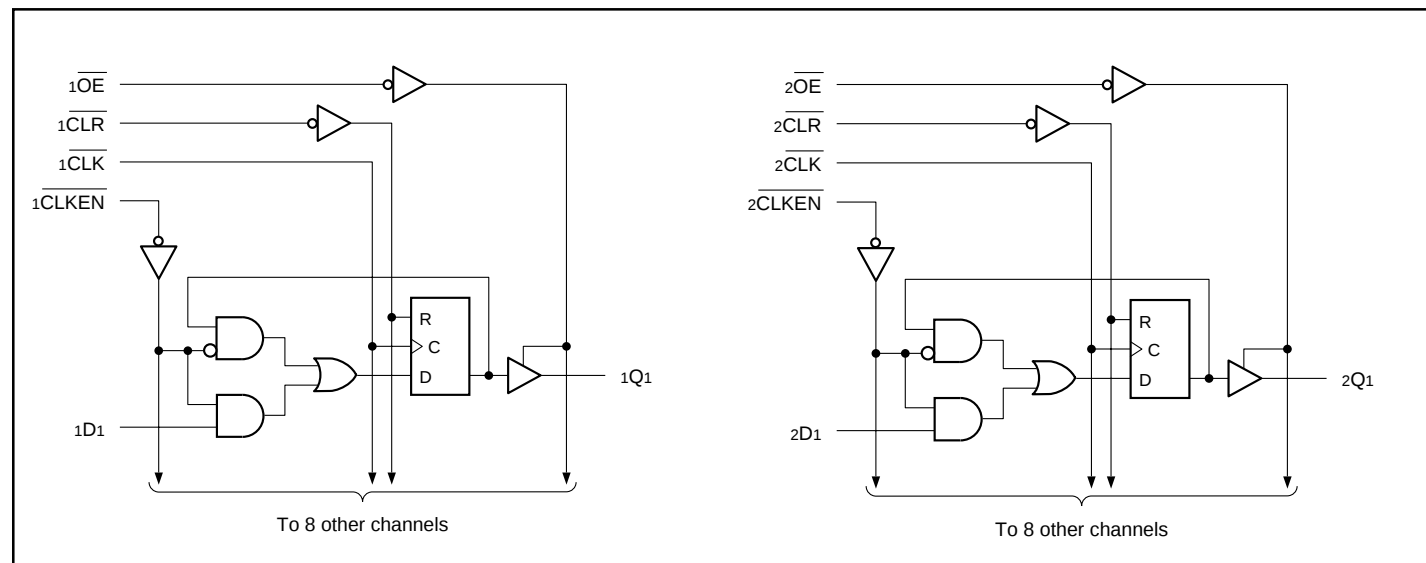
The PI74FCT16823T, PI74FCT162823T and PI74FCT162H823 are 18-bit wide registers with clock enable ($\overline{xCLKEN}$) and clear ($\overline{xCLR}$) controls that make these devices especially suitable for parity bus interfacing in high-performance systems. The devices can be operated as two 9-bit registers or one 18-bit register using the control inputs. Signal pins are arranged in a flow-through organization for ease of layout and hysteresis is designed into all inputs to improve noise margin.

The PI74FCT16823T output buffers are designed with a Power-Off disable function allowing “live insertion” of boards when the devices are used as backplane drives.

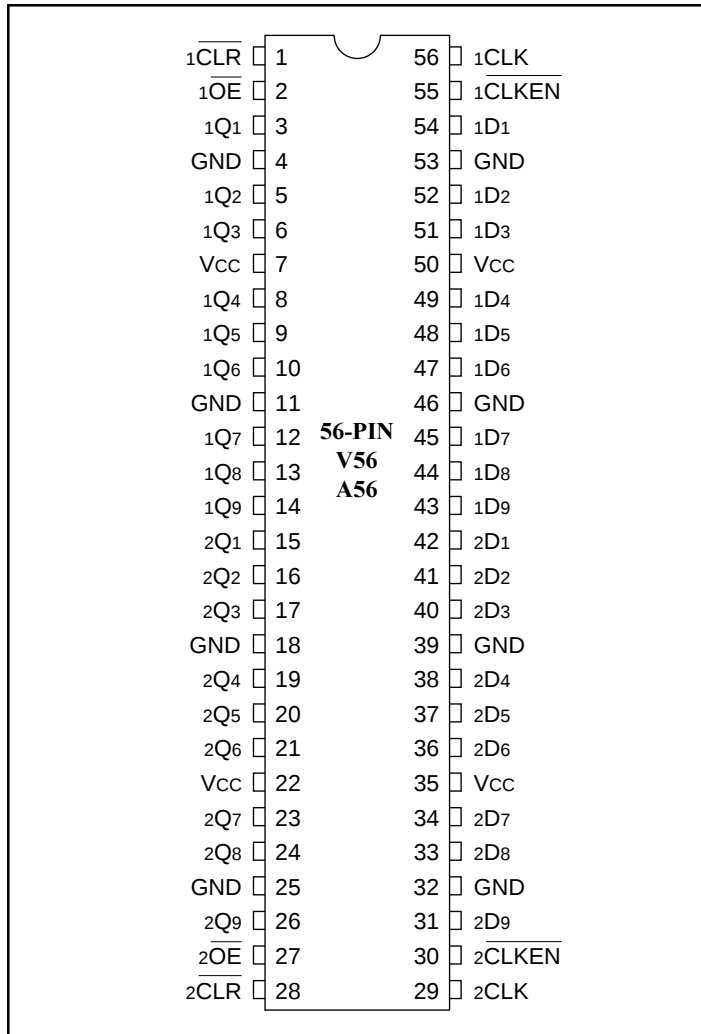
The PI74FCT162823T has $\pm 24 \text{ mA}$ balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

The PI74FCT162H823T has “Bus Hold” which retains the input's last state whenever the input goes to high-impedance preventing “floating” inputs and eliminating the need for pull-up/down resistors.

Logic Block Diagram



Product Pin Configuration



Product Pin Description

Pin Name	Description
xDx	Data Inputs ⁽¹⁾
xCLK	Clock Inputs
xCLKEN	Clock Enable Inputs (Active LOW)
xCLR	Asynchronous Clear Inputs (Active LOW)
xOE	Output Enable Inputs (Active LOW)
xQx	3-State Outputs

Note: 1. For the PI74FCT162H823T, these pins have “Bus Hold.” All other pins are standard, outputs, or I/Os.

PI74FCT16823 Truth Table(1)

Function	Inputs					Outputs
	xOE	xCLR	xCLKEN	xCLK	xDx	xQx
High-Z	H	X	X	X	X	Z
Clear	L	L	X	X	X	L
Hold	L	H	H	X	X	Q ⁽²⁾
Load	H	H	L	↑	L	Z
	H	H	L	↑	H	Z
	L	H	L	↑	L	L
	L	H	L	↑	H	H

- H = High Voltage Level
L = Low Voltage Level
X = Don't Care
Z = High Impedance
NC = No Change
↑ = LOW-to-HIGH Transition
- Output level before indicated steady-state input conditions were established.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–40°C to +85°C
Supply Voltage to Ground Potential (Inputs & V _{CC} Only)	–0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
I _{IH}	Input HIGH Current	Standard Input, V _{CC} = Max.	V _{IN} = V _{CC}			1	μA
I _{IH}	Input HIGH Current	Standard I/O, V _{CC} = Max.	V _{IN} = V _{CC}			1	μA
I _{IH}	Input HIGH Current	Bus Hold Input ⁽⁴⁾ , V _{CC} = Max.	V _{IN} = V _{CC}			±100	μA
I _{IH}	Input HIGH Current	Bus Hold I/O ⁽⁴⁾ , V _{CC} = Max.	V _{IN} = V _{CC}			±100	μA
I _{IL}	Input LOW Current	Standard Input, V _{CC} = Min.	V _{IN} = GND			–1	μA
I _{IL}	Input LOW Current	Standard I/O, V _{CC} = Min.	V _{IN} = GND			–1	μA
I _{IL}	Input LOW Current	Bus Hold Input ⁽⁴⁾ , V _{CC} = Min.	V _{IN} = GND			±100	μA
I _{IL}	Input LOW Current	Bus Hold I/O ⁽⁴⁾ , V _{CC} = Min.	V _{IN} = GND			±100	μA
I _{BHH}	Bus Hold	Bus Hold Input ⁽⁴⁾ , V _{CC} = Min.	V _{IN} = 2.0V	–50			μA
I _{BHL}	Sustain Current		V _{IN} = 0.8V	+50			μA
I _{OZH} ⁽⁵⁾	High-Impedance	V _{CC} = Max.	V _{OUT} = 2.7V			1	μA
I _{OZL} ⁽⁵⁾	Output Current (3-STATE OUTPUTS)	V _{CC} = Max.	V _{OUT} = 0.5V			–1	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = –18 mA			–0.7	–1.2	V
I _{OS}	Short Circuit Current	V _{CC} = Max. ⁽³⁾ , V _{OUT} = GND		–80	–140	–200	mA
I _O	Output Drive Current	V _{CC} = Max. ⁽³⁾ , V _{OUT} = 2.5V		–50		–180	mA
V _H	Input Hysteresis				100		mV

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. Pins with Bus Hold are identified in the pin description.
5. This specification does not apply to bi-directional functionalities with Bus Hold.

PI74FCT16823T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
VOH	Output HIGH Voltage	VCC = Min., VIN = VIH or VIL	IOH = -3.0 mA	2.5	3.5		V
			IOH = -15.0 mA	2.4	3.5		
			IOH = -32.0 mA	2.0	3.0		
VOL	Output LOW Voltage	VCC = Min., VIN = VIH or VIL	IOL = 64 mA		0.2	0.55	V
IOFF	Power Down Disable	VCC = 0V, VIN or VOUT ≤ 4.5V		—	—	±100	μA

PI74FCT162823T/162H823T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
VOH	Output HIGH Voltage	VCC = Min., VIN = VIH or VIL	IOH = -24.0 mA	2.4	3.3		V
VOL	Output LOW Voltage	VCC = Min., VIN = VIH or VIL	IOL = 24 mA		0.3	0.55	V
IODL	Output LOW Current	VCC = 5V, VIN = VIH OR VIL, VOUT = 1.5V ⁽³⁾		60	115	150	mA
IODH	Output HIGH Current	VCC = 5V, VIN = VIH OR VIL, VOUT = 1.5V ⁽³⁾		-60	-115	-150	mA

Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
CIN	Input Capacitance	VIN = 0V	4.5	6	pF
COUT	Output Capacitance	VOUT = 0V	5.5	8	pF

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at VCC = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	500	μA
ΔI _{CC}	Supply Current per Input @ TTL HIGH	V _{CC} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	1.5	mA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{CC} = Max., Outputs Open x $\overline{\text{OE}}$ = x $\overline{\text{CLKEN}}$ = GND One Input Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		75	120	μA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _{CP} = 10 MHz 50% Duty Cycle x $\overline{\text{OE}}$ = x $\overline{\text{CLKEN}}$ = GND fi = 5 MHz One Bit Toggling	V _{IN} = V _{CC} V _{IN} = GND		0.8	2.7	mA
			V _{IN} = 3.4V V _{IN} = GND		1.3	3.2	
		V _{CC} = Max., Outputs Open f _{CP} = 10 MHz 50% Duty Cycle x $\overline{\text{OE}}$ = x $\overline{\text{CLKEN}}$ = GND Eighteen Bits Toggling fi = 2.5 MHz 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		4.2	7.1 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND		9.2	22.1 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}

$$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$$

I_{CC} = Quiescent Current
ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V).
D_H = Duty Cycle for TTL Inputs High.
N_T = Number of TTL Inputs at D_H.
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL).
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_i = Input Frequency
N_i = Number of Inputs at f.
All currents are in milliamps and all frequencies are in megahertz.

PI74FCT16823T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	16823AT		16823BT		16823CT		16823DT		16823ET		Unit
			Com.		Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
tPLH tPHL	Propagation Delay xCLK to xQx	C _L = 50 pF R _L = 500Ω	1.5	10.0	1.5	7.5	1.5	6.0	1.5	5.0	1.5	4.4	ns
		C _L = 300 pF ⁽³⁾ R _L = 500Ω	1.5	20.0	1.5	15.0	1.5	12.5	1.5	8.5	1.5	8.0	ns
tPHL	Propagation Delay xCLR to xQx	C _L = 50 pF R _L = 500Ω	1.5	14.0	1.5	9.0	1.5	8.0	1.5	5.0	1.5	4.4	ns
tPZH tPZL	Output Enable Time xOE to xQx	C _L = 50 pF R _L = 500Ω	1.5	12.0	1.5	8.0	1.5	7.0	1.5	4.8	1.5	4.4	ns
		C _L = 300 pF ⁽³⁾ R _L = 500Ω	1.5	23.0	1.5	15.0	1.5	12.5	1.5	10.0	1.5	9.0	ns
tPHZ tPLZ	Output Disable Time ⁽³⁾ xOE to xQx	C _L = 5 pF ⁽³⁾ R _L = 500Ω	1.5	7.0	1.5	6.5	1.5	6.2	1.5	5.0	1.5	4.0	ns
		C _L = 50 pF R _L = 500Ω	1.5	8.0	1.5	7.5	1.5	6.5	1.5	5.0	1.5	4.0	ns
tsu	Setup Time HIGH or LOW, xDx to xCLK	C _L = 50 pF R _L = 500Ω	4.0	—	3.0	—	3.0	—	3.0	—	1.5	—	ns
th	Hold Time HIGH or LOW, xDx to xCLK		2.0	—	1.5	—	1.5	—	1.5	—	0	—	ns
tsu	Setup Time HIGH or LOW, xCLKEN to xCLK		4.0	—	3.0	—	3.0	—	3.0	—	2.5	—	ns
th	Hold Time HIGH or LOW, xCLKEN to xCLK		2.0	—	0	—	0	—	0	—	0	—	ns
tw	xCLK Pulse Width HIGH or LOW ⁽³⁾		7.0	—	6.0	—	6.0	—	6.0	—	3.0	—	ns
tw	xCLR Pulse Width LOW ⁽³⁾		6.0	—	6.0	—	6.0	—	6.0	—	3.0	—	ns
tREM	Recovery Time ⁽³⁾ xCLR to xCLK		6.0	—	6.0	—	6.0	—	6.0	—	3.0	—	ns
tsk(o)	Output Skew ⁽⁴⁾		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

PI74FCT162823T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	162823AT		162823BT		162823CT		162823DT		162823ET		Unit
			Com.		Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
tPLH tPHL	Propagation Delay xCLK to xQx	C _L = 50 pF R _L = 500Ω	1.5	10.0	1.5	7.5	1.5	6.0	1.5	5.0	1.5	4.4	ns
		C _L = 300 pF ⁽³⁾ R _L = 500Ω	1.5	20.0	1.5	15.0	1.5	12.5	1.5	8.5	1.5	8.0	ns
tPHL	Propagation Delay xCLR to xQx	C _L = 50 pF R _L = 500Ω	1.5	14.0	1.5	9.0	1.5	8.0	1.5	5.0	1.5	4.4	ns
tPZH tPZL	Output Enable Time xOE to xQx	C _L = 50 pF R _L = 500Ω	1.5	12.0	1.5	8.0	1.5	7.0	1.5	4.8	1.5	4.4	ns
		C _L = 300 pF ⁽³⁾ R _L = 500Ω	1.5	23.0	1.5	15.0	1.5	12.5	1.5	10.0	1.5	9.0	ns
tPHZ tPLZ	Output Disable Time ⁽³⁾ xOE to xQx	C _L = 5 pF ⁽³⁾ R _L = 500Ω	1.5	7.0	1.5	6.5	1.5	6.2	1.5	5.0	1.5	4.0	ns
		C _L = 50 pF R _L = 500Ω	1.5	8.0	1.5	7.5	1.5	6.5	1.5	5.0	1.5	4.0	ns
tsu	Setup Time HIGH or LOW, xDx to xCLK	C _L = 50 pF R _L = 500Ω	4.0	—	3.0	—	3.0	—	3.0	—	1.5	—	ns
th	Hold Time HIGH or LOW, xDx to xCLK		2.0	—	1.5	—	1.5	—	1.5	—	0	—	ns
tsu	Setup Time HIGH or LOW, xCLKEN to xCLK		4.0	—	3.0	—	3.0	—	3.0	—	2.5	—	ns
th	Hold Time HIGH or LOW, xCLKEN to xCLK		2.0	—	0	—	0	—	0	—	0	—	ns
tw	xCLK Pulse Width HIGH or LOW ⁽³⁾		7.0	—	6.0	—	6.0	—	6.0	—	3.0	—	ns
tw	xCLR Pulse Width LOW ⁽³⁾		6.0	—	6.0	—	6.0	—	6.0	—	3.0	—	ns
tREM	Recovery Time ⁽³⁾ xCLR to xCLK		6.0	—	6.0	—	6.0	—	6.0	—	3.0	—	ns
tsk(o)	Output Skew ⁽⁴⁾		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

PI74FCT162H823T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	162H823AT		162H823BT		1628H23CT		162H823DT		162H823ET		Unit
			Com.		Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
tPLH tPHL	Propagation Delay xCLK to xQx	C _L = 50 pF R _L = 500Ω	1.5	10.0	1.5	7.5	1.5	6.0	1.5	5.0	1.5	4.4	ns
		C _L = 300 pF ⁽³⁾ R _L = 500Ω	1.5	20.0	1.5	15.0	1.5	12.5	1.5	8.5	1.5	8.0	ns
tPHL	Propagation Delay xCLR to xQx	C _L = 50 pF R _L = 500Ω	1.5	14.0	1.5	9.0	1.5	8.0	1.5	5.0	1.5	4.4	ns
tPZH tPZL	Output Enable Time xOE to xQx	C _L = 50 pF R _L = 500Ω	1.5	12.0	1.5	8.0	1.5	7.0	1.5	4.8	1.5	4.4	ns
		C _L = 300 pF ⁽³⁾ R _L = 500Ω	1.5	23.0	1.5	15.0	1.5	12.5	1.5	10.0	1.5	9.0	ns
tPHZ tPLZ	Output Disable Time ⁽³⁾ xOE to xQx	C _L = 5 pF ⁽³⁾ R _L = 500Ω	1.5	7.0	1.5	6.5	1.5	6.2	1.5	5.0	1.5	4.0	ns
		C _L = 50 pF R _L = 500Ω	1.5	8.0	1.5	7.5	1.5	6.5	1.5	5.0	1.5	4.0	ns
tsu	Setup Time HIGH or LOW, xDx to xCLK	C _L = 50 pF R _L = 500Ω	4.0	—	3.0	—	3.0	—	3.0	—	1.5	—	ns
th	Hold Time HIGH or LOW, xDx to xCLK		2.0	—	1.5	—	1.5	—	1.5	—	0	—	ns
tsu	Setup Time HIGH or LOW, xCLKEN to xCLK		4.0	—	3.0	—	3.0	—	3.0	—	2.5	—	ns
th	Hold Time HIGH or LOW, xCLKEN to xCLK		2.0	—	0	—	0	—	0	—	0	—	ns
tw	xCLK Pulse Width HIGH or LOW ⁽³⁾		7.0	—	6.0	—	6.0	—	6.0	—	3.0	—	ns
tw	xCLR Pulse Width LOW ⁽³⁾		6.0	—	6.0	—	6.0	—	6.0	—	3.0	—	ns
tREM	Recovery Time ⁽³⁾ xCLR to xCLK		6.0	—	6.0	—	6.0	—	6.0	—	3.0	—	ns
tsk(o)	Output Skew ⁽⁴⁾		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.