HT82810
Date Time Stamp

Features

- Operating voltage: 2.4V~5.0V
- Low power consumption
- 16-second voice capacity (based on a 6kHz sampling rate)
- Maximum 63 sections of voice
- Repeat function: one section is played repeatedly
- Random function: one section is selected randomly from a max. of 8 sections and is then activated
- CPU/Manual control selection
- Parallel/Serial address type
- Built-in D/A converter
- Forced standby
- Automatic standby
- Auto power-down output
- RC oscillator
- HT82810 voltage type D/A output

Application

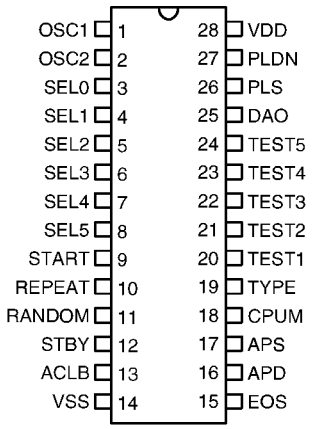
- Toys
- Alarm clock
- Public address system
- Alert and warning system
- Answering machine

General Description

The HT82810 is a single chip PCM voice synthesizer LSI implemented in CMOS technology. It provides 16-second voice capacity at a 6kHz sampling rate. The 16-second capacity can be divided into a max. of 63 sections in which customer's prompt messages are stored. Play back functions (single section, repeat, random) are controlled manually or by CPU. For CPU control, there are parallel and serial types for addressing the section selection. It provides internal/external power down control for power saving and provides pull-low resistor control for external interface convenience.

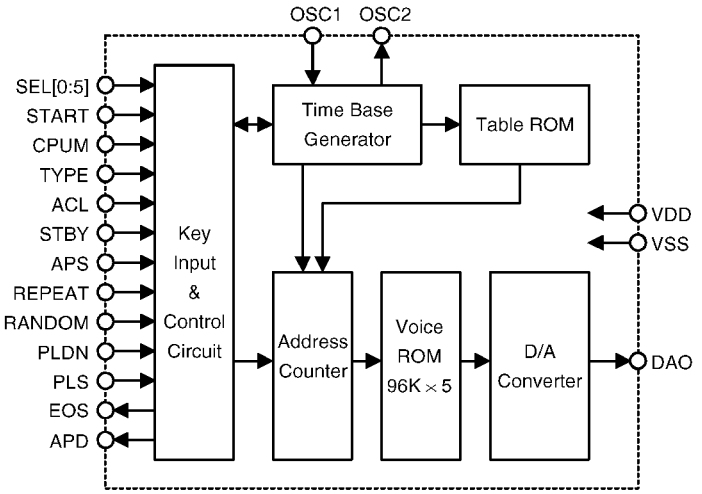
The chip is suitable for voice prompt systems, especially for use as date time stamp for answering machine.

Pin Assignment



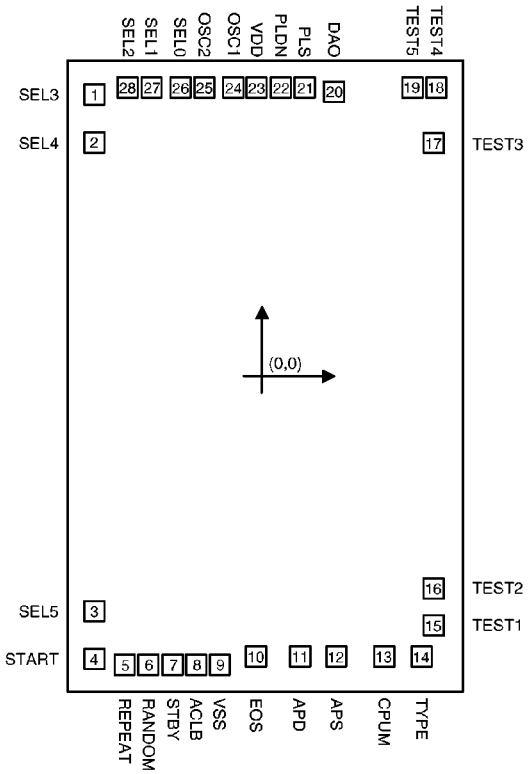
HT82810
– 28 SDIP/SOP

Block Diagram



Pad Coordinates

Unit: mil



Pad No.	X	Y	Pad No.	X	Y
1	–998.3	1679.95	15	1023.3	–1486.45
2	–998.3	1394.15	16	1023.3	–1266.85
3	–998.3	–1401.15	17	1023.3	1390.55
4	–998.3	–1686.95	18	1039.8	1721.95
5	–817.9	–1721.95	19	896.8	1721.95
6	–677.9	–1721.95	20	429.2	1695.35
7	–531	–1721.95	21	255.6	1721.95
8	–391	–1721.95	22	112.6	1721.95
9	–251	–1721.95	23	–32.4	1721.95
10	–35.8	–1671.45	24	–171.4	1721.95
11	228.2	–1671.45	25	–342.9	1721.95
12	443.4	–1671.45	26	–485.9	1721.95
13	729.2	–1671.45	27	–657.4	1721.95
14	952.7	–1671.45	28	–800.4	1721.95

Chip size: 95×149 (mil)^2

* The IC substrate should be connected to VSS in the PCB layout artwork.

Pin Description

Pin No.	Pin Name	I/O	Internal Connection	Description
1	OSC1	I	—	A resistor is connected between OSC1 and OSC2 for RC oscillation. A clock is entered to OSC1 but OSC2 is left open for an external clock.
2	OSC2	O	—	
3~8	SEL[0:5]	I	*Pull-Low or None	A binary code is set to the SEL pins for playing section selection. The max. number of sections that can be selected is 63. The SEL pins also determine the number of base sections (2~8) for random playing.
9	START	I	*Pull-Low or None	Input pin for starting a sound output

Pin No.	Pin Name	I/O	Internal Connection	Description
10	REPEAT	I	Floating	Repeat function enable, active high To terminate repeating, reset the REPEAT pin or use the STBY or ACLB pin.
11	RANDOM	I	Floating	Random function enable, active high The amount of base sections is determined by SEL[0:5]
12	STBY	I	Pull-High	If a high level is applied to the STBY pin, the chip will enter the standby mode and stop oscillation. When APS=high, this pin will be ignored.
13	ACLB	I	Pull-High	Reset the system when in low level or low pulse. Oscillation is still in process and DAO remains at $1/2V_{DD}$.
14	VSS	I	—	Negative power supply (GND)
15	EOS	O	CMOS	Busy output & active low when sounds are output EOS=1 when in standby EOS=0 during sound output
16	APD	O	CMOS	Indicate output of audio power down APD=1 when in the standby mode. Otherwise APD=0
17	APS	I	Pull-High	Automatic standby control The system enters the standby state if APS=1 and a sound output ends. It quits the standby mode once there is another sound output.
18	CPUM	I	Pull-High	CPU/manual control selection: CPUM=1: CPU control CPUM=0: manual control
19	TYPE	I	Pull-Low	Parallel/serial type selection TYPE=1: serial type (section addresses are input serially from SEL0) TYPE=0: parallel type (section addresses are input parallel from SEL[0:5])
20 21	TEST2 TEST3	I	Pull-High	For IC test only
22~24	TEST4~ TEST6	O	—	For IC test only
25	DAO	O	PMOS Open Drain	Sound output of voltage type for driving external op amplifier
26	PLS	I	CMOS	Pull-Low selection input of the START and SEL [0:5] pins in the manual mode Address clocks are serially input (refer to the functional description for details)

Pin No.	Pin Name	I/O	Internal Connection	Description
27	PLDN	I	CMOS	Control of pull-low resistor as to SEL [0:5] and START pins in manual control, see functional description for more detail.
28	VDD	I	—	Positive power supply

Absolute Maximum Ratings*

Supply Voltage ..... –0.3V to 6V
Input Voltage ..... V_{SS}–0.3V to V_{DD}+0.3V
Storage Temperature ..... –50°C to 125°C
Operating Temperature ..... –20°C to 70°C

*Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

(Ta=25°C)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	2.4	—	5	V
I_{DD}	Operating Current	5V	No load, f_{OSC}=96kHz	—	—	900	μA
I_{STB}	Standby Current	5V	—	—	1	5	μA
I_{WAT}	Waiting-state Current	5V	No load, f_{OSC}=96kHz	—	—	900	μA
R_{PL}	SEL[0:5] & START Pull-Low Resistor	5V	—	50	100	200	kΩ
R_{PH1}	STBY Pull-High Resistor	5V	—	50	200	500	kΩ
R_{PH2}	ACLB Pull-High Resistor	5V	—	5	10	25	kΩ
I_{OH}	EOS & APD Source Current	5V	V_{OH}=4.5V	–1	–2	—	mA
I_{OL}	EOS & APD Sink Current	5V	V_{OL}=0.5V	2	5	—	mA
V_{IH1}	High Level Input Voltage 1	5V	CPUM, APS, PLDN, PLS	4.7	—	5	V
V_{IH2}	High Level Input Voltage 2	5V	Other than upper pins	2.3	—	5	V
V_{IL1}	Low Level Input Voltage 1	5V	CPUM, APS, PLDN, PLS	0	—	0.8	V

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{IL2}	Low Level Input Voltage 2	5V	Other than upper pins	0	—	0.5	V
f_{OSC}	Oscillating Frequency	5V	R=430kΩ	72	96	120	kHz

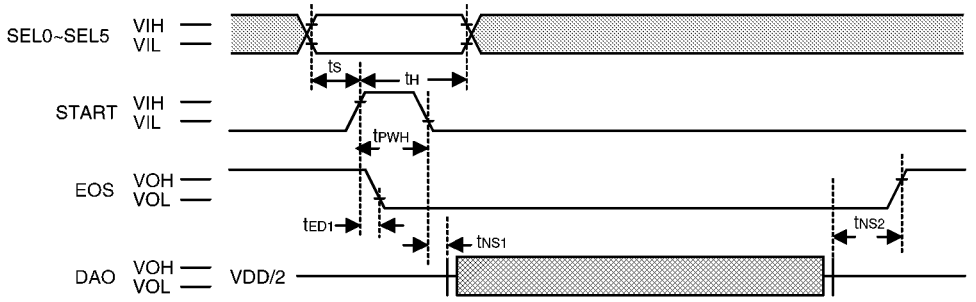
A.C. Characteristics

(f_{OSC}=96kHz)

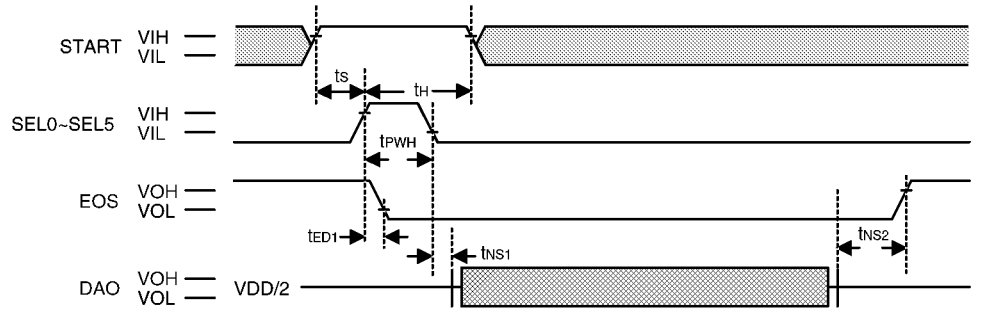
• Parallel address type in CPU control

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_S	Setup Time	400	—	—	ns
t_H	Hold Time	360	—	—	ns
t_{PWH}	START Pulse Width	600	—	—	ns
t_{ED1}	EOS Delay Time	—	—	900	ns
t_{NS1}	No Voice Time 1	—	2	—	ms
t_{NS2}	No Voice Time 2	10	—	40	ms

START trigger

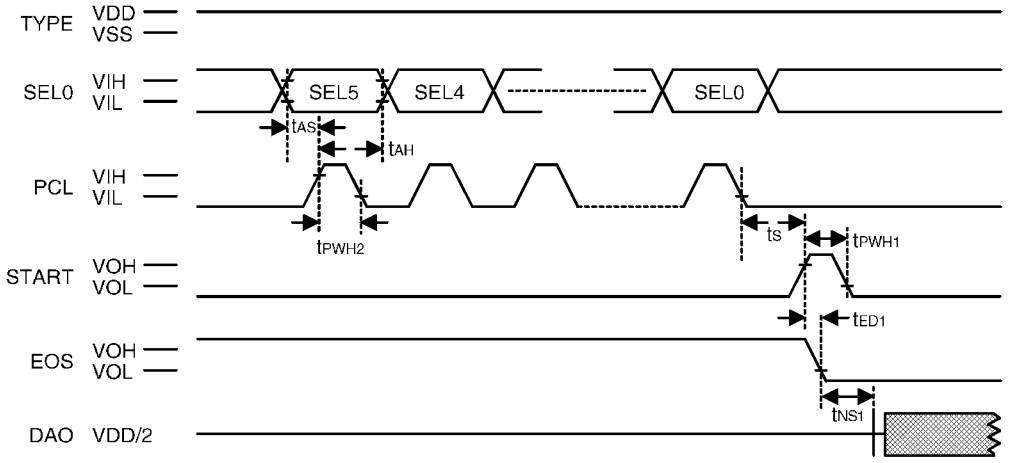


SEL0~5 trigger



• Serial address type in CPU control

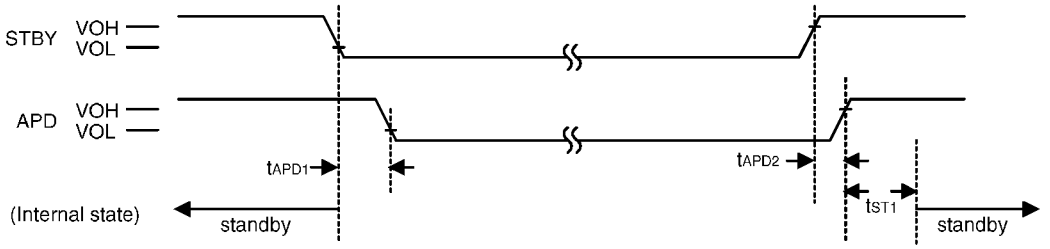
Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{AS}	Setup Time	400	—	—	ns
t_{AH}	Hold Time	400	—	—	ns
t_S	Setup Time	400	—	—	ns
t_{PWH1}	START Pulse Width	600	—	—	ns
t_{PWH2}	PCL Pulse Width	600	—	—	ns
t_{ED1}	EOS Delay Time	—	—	900	ns
t_{NS1}	No Voice Time 1	—	2	—	ms



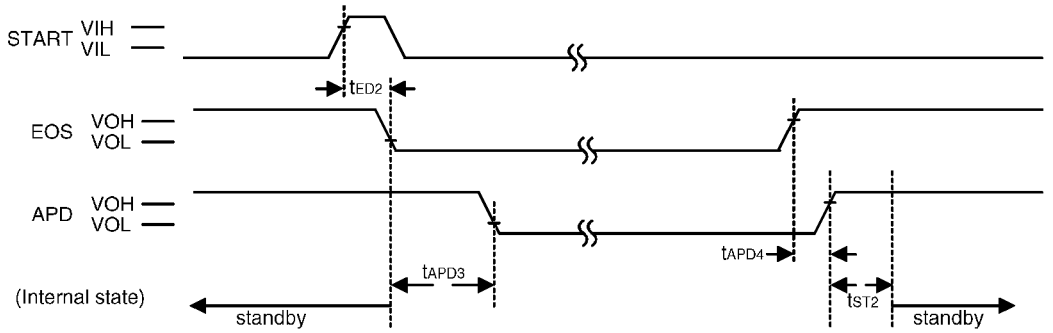
• Standby state and APD output in CPU control

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{APD1}	APD Delay Time 1	—	—	10	ms
t_{APD2}	APD Delay Time 2	—	—	900	ns
t_{APD3}	APD Delay Time 3	—	—	10	ms
t_{APD4}	APD Delay Time 4	—	—	20	μs
t_{ED2}	EOS Delay Time 2	—	—	900	ns
t_{ST1}	Standby Delay Time 1	—	—	20	ms
t_{ST2}	Standby Delay Time 2	—	—	20	

Standby state by the STBY pin (APS=L level)



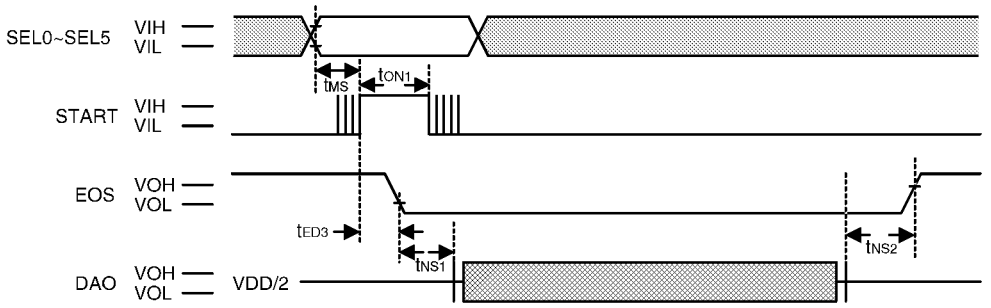
Standby state by the APS pin (APS=H level)



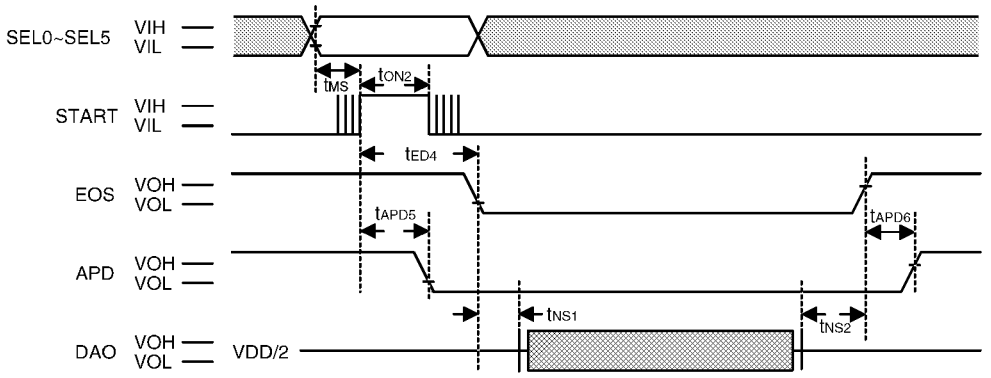
• Timing on manual control

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{MS}	Manual Control Set Up Time	0	—	—	ns
t_{ON1}	Switch On Time 1	32	—	—	ms
t_{ON2}	Switch On Time 2	32	—	—	
t_{ED3}	EOS Delay Time 3	—	—	32	
t_{ED4}	EOS Delay Time 4	—	—	1	ms
t_{NS1}	No Speech Time 1	—	2	—	ms
t_{NS2}	No Speech Time 2	10	—	40	
t_{APD5}	APD Delay Time 5	—	—	2	
t_{APD6}	APD Delay Time 6	—	—	20	μs

Not during automatic power standby function (APS=low)

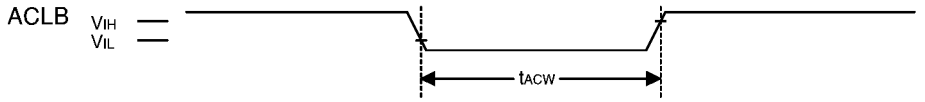


During automatic power standby function (APS=high)



• ACLB pulse width

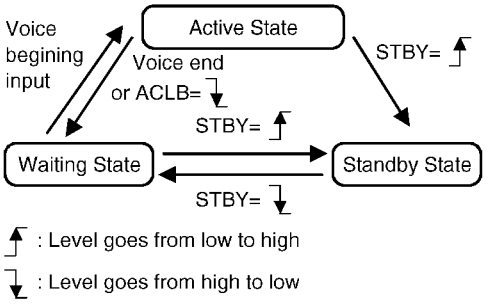
Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{ACW}	ACLB Pulse Width	500	—	—	ns



Functional Description

The HT82810 is a single chip PCM voice synthesizer LSI with 16-second voice capacity at a 6kHz sampling rate. It can operate in a CPU interface or manual mode as determined by the CPUM pin. When CPUM is high, the HT82810 runs in CPU control mode. When CPUM is low, manual control is the operating mode . In addition, the HT82810 includes three internal states namely, standby state, waiting state and active state.

The state diagram is shown below:



Standby state

The standby state function is provided to reduce power consumption. The system will change to standby state by activating the STBY and APS pins. The conditions setting the standby state are shown below:

- When the STBY is set high and the APS is set low, the HT82810 goes into the standby state. During this time, voice synthesis will not be re-initiated by any voice start input, i.e. the whole chip is disabled.
- When the APS pin is set high
  - * And when the voice currently talking is finished, the internal circuit is automatically set in the standby state.
  - * And when the ACLB is set low, the voice presently talking is forcefully terminated and the system goes into the standby state.

In the standby state, the following five conditions will occur:

- The oscillation stops
- The EOS and APD pins are changed to high level
- The DAO pin is fixed to low
- The internal circuit is reset to the initial state
- The SEL [0:5] and START pins are open

	State of Inner Circuit	DAO Voice Output Pin	EOS Output Pin Level	APD Output Pin Level
Standby state	* Reset to initial status * Oscillation stop	GND-level	High	High
Waiting state	* Reset to initial status * In oscillation	VDD/2 level	High	Low
Active state	* Operating state * In oscillation	Voice waveform output	Low	Low

Waiting state

The waiting state functions as a transition between the active and standby states. If the current state is the standby state, the active state cannot be initiated without transitionally shifting to the waiting state. On the other hand, if the active state is finished and the system tries to go to the standby state, transitionally shifting to the waiting state can avoid any unnecessary noises, such as "pop". Otherwise, the "pop" noise would be emitted if the active state is directly changed to the standby state.

Active state

The active state indicates that voice is output.

- Setting a section (phrase)

  To set a section, SEL0~SEL5 are employed. With SEL0~SEL5 the total number of sections selectable is 63.

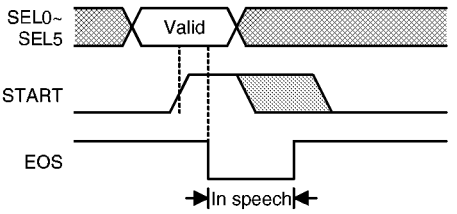
Phrase No.	SEL5	SEL4	SEL3	SEL2	SEL1	SEL0
1	0	0	0	0	0	1
2	0	0	0	0	1	0
⋮	⋮	⋮	⋮	⋮	⋮	⋮
62	1	1	1	1	1	0
63	1	1	1	1	1	1

- Starting a voice

  The HT82810 provides two kinds of operating modes, i.e., CPU control mode and manual control mode, which are determined by the CPUM pin. When the CPUM is high, the system is in CPU control mode, whereas the system is in manual control mode when CPUM is low. For each control mode, two kinds of active start inputs are provided namely, START trigger and SEL trigger. Voice is output from the DAO and the EOS is changed from high to low when a trigger input is given. The following is the individual description for these modes.

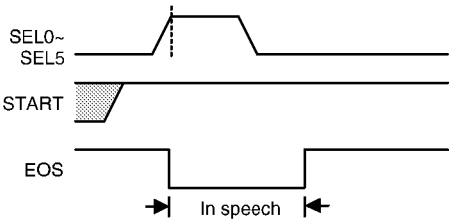
  * Manual Control (CPUM is connected to VSS):
    - START trigger

      In the manual control mode, voice begins after the SEL0~SEL5 pins are set and the START pin is set high. The START and the SEL0~SEL5 inputs are debounced.



    - SEL trigger

      When the START pin is fixed to high level and SEL0~SEL5 are set to low level, voice is initiated by the rising edge on SEL0~SEL5. Notice that the low to high transition time of SEL0~SEL5 should be less than the input debounce time. However, this method of trigger input is inhibited with the random function.

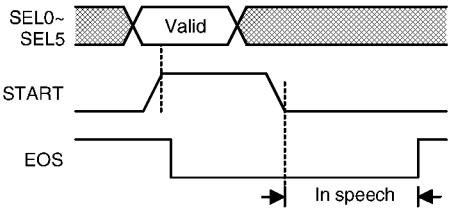


  * CPU Control (CPUM is connected to VDD):

    In the CPU control mode, there are parallel address and serial address types for section selection. When TYPE is high, the chip runs in serial type and when TYPE is low, it runs in parallel type .

    - START trigger in parallel address type

      The section set at the SEL0~SEL5 pins is loaded to HT82810 during the impulse rising of the START pin. However, at the falling edge of the START pin, the voice is initiated.

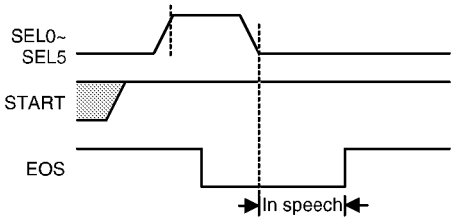


– START trigger in serial address type

In serial address type, the SEL0 and PLS control signals are used to write the presented section address data serially. When TYPE is high, the address data on pin SEL0 is clocked into the device serially on the rising edge of the PLS signal. After the address is written, the section voice is output at the falling edge of the START pin (see Figure 1).

– SEL trigger

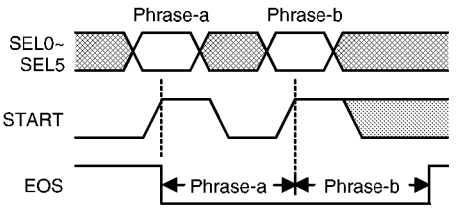
When the START pin is set to high level and all the SEL0~SEL5 pins are set to low level, the system goes into the waiting state. After a positive pulse is input to one of the SEL0~SEL5 pins, voice then begins at the pulse falling edge. In this way, the max. number of sections that can be selected is six.



• Changing voice sections during voice

* Controlled by START pin

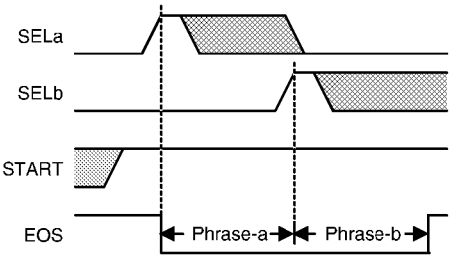
As the following diagram shows, when section-a is currently being activated, a new section-b is assigned by the SEL0~SEL5 pins. Then, the section-a is terminated by a new START pulse. During this time, speech of the new section-b begins. This is valid for



both manual and CPU control.

* Controlled by SEL[0:5]

All the SEL0~SEL5 pins are first set to low level and the START pin is maintained at high level. The high level or a pulse is then given to one of the SEL0~SEL5 pins in the manual and the CPU control, respectively.



Thereby the section currently being activated is terminated and a new section speech starts.

Note:

SELa, SELb are one of SEL0~SEL5 respectively. For CPU mode, the voice is initiated by the falling edge of SEL pulses.

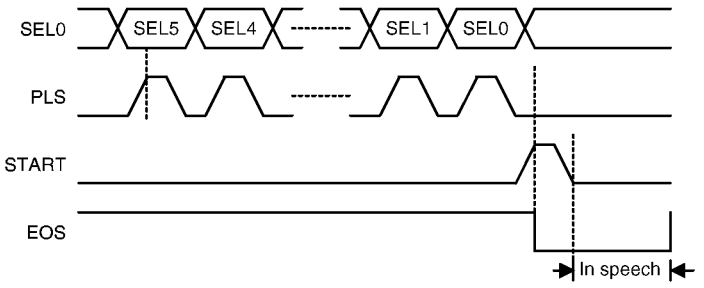


Figure 1

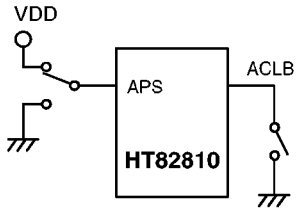
• Ending the voice

When active, the EOS (busy) pin outputs a low level and is then changed to high level upon completion of the voice. The voice can be forcefully terminated by one of the following three methods (however, the EOS remains high even after the voice is forcefully terminated):

* Using ACLB

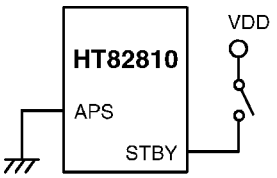
The ACLB pin is provided for initialization. By setting the ACLB low, voice can be forcefully terminated. After voice is terminated, the HT82810 goes into the waiting or standby state as determined by the APS pin.

APS=0: Waiting state
APS=1: Standby state



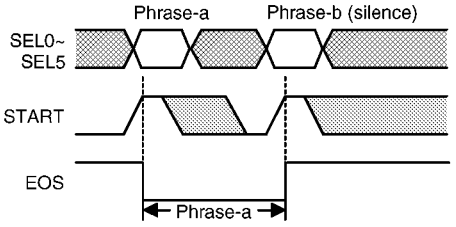
* Using STBY

By setting the STBY high, voice can be forcefully terminated when the APS is set low. The HT82810 then enters the standby state after voice is terminated.



* Using silence section

During voice output, the output can be terminated by assigning the silence section.



• Repeating a section

In the manual control mode, an assigned section can be repeatedly synthesized by setting the REPEAT high and triggering START or SEL. On the other hand, in CPU control mode, voice can be initiated and repeated by triggering START only.

Repeat function can be terminated by the STBY (STBY=high) or the ACLB (ACL=low) input, or resetting the repeat function (REPEAT=low). With the STBY and ACLB pins set, voice can be terminated immediately. However, by resetting the REPEAT pin, the currently activated section cannot be terminated until the whole section is finished.

• Random function

By setting the RANDOM pin high and activating the START trigger, one section can be randomly selected. The maximum base number for a random section is eight. The base number is set by the input of the SEL0~SEL5 pins. Shown below is a table displaying the setting of the SEL0~SEL5 pins. However, it should be noted that the random function cannot be used with the APS or repeat functions.

SEL5	SEL4	SEL3	SEL2	SEL1	SEL0	Qty of section	No. of section
0	0	0	*	*	*	8	56~63
0	0	1	1	1	1	7	56~62
0	0	1	1	1	0	6	56~61
0	0	1	1	0	1	5	56~60
0	0	1	1	0	0	4	56~59
0	0	1	0	1	1	3	56~58
0	0	1	0	1	0	2	56~57

• Input resistors

The pull-low resistors are connected to the START and SEL0~SEL5 pins depending on the inputs at the PLDN, PLS, CPUM and RANDOM pins, as shown in Table 1.

Conditions				START		SEL[0:5]	
CPUM	**RANDOM**	**PLDN**	**PLS**	**Non-Standby**	**Standby**	**Non-Standby**	**Standby**
1	X	X	X	None	None	None	None
0	X	0	X	None	None	None	None
0	1	1	0	Pull-low	Pull-low	None	None
0	1	1	1	None*	Pull-low	None	None
0	0	1	0	Pull-low	Pull-low	None*	Pull-low
0	0	1	1	None*	Pull-low	Pull-low	Pull-low

Table 1

1=high, 0=low, X=Don't care

Notice:

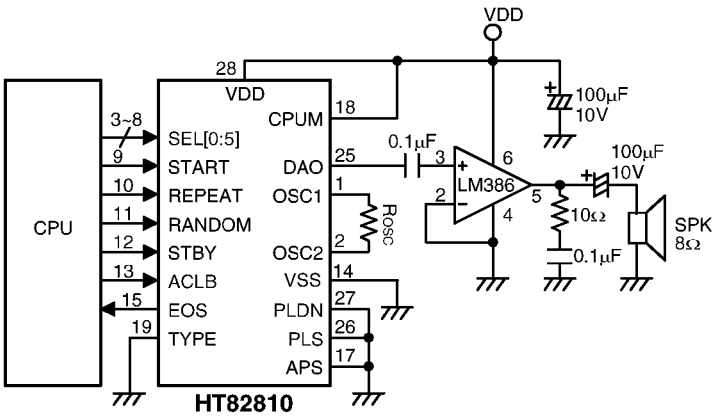
None: Pull-low resistor is not connected

Pull-down: Pull-low resistor is connected

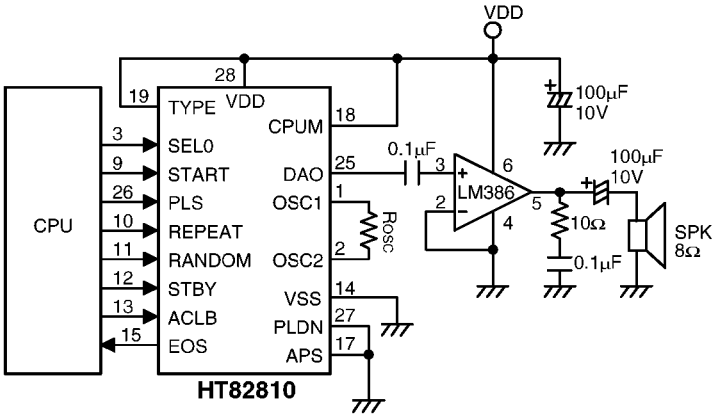
*: Active pull-low resistors which is effective only when the chip is active

Application Circuits

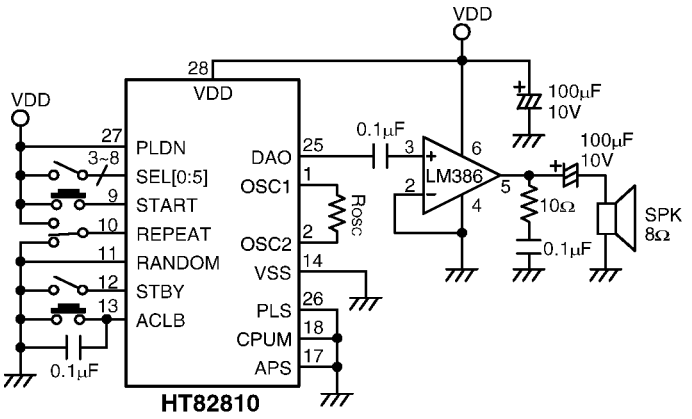
CPU control (Parallel address type)



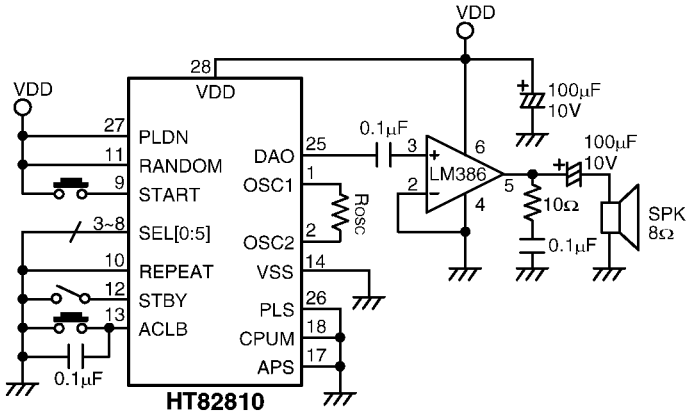
CPU control (serial address type)



Manual control with repeat selection



Manual control with random selection



HT82811 (English)

Section	Voice Content	Section	Voice Content
1	One	20	Twenty
2	Two	21	Thirty
3	Three	22	Forty
4	Four	23	Fifty
5	Five	24	Oh
6	Six	25	A.M.
7	Seven	26	P.M.
8	Eight	27	Sun–
9	Nine	28	Mon–
10	Ten	29	Tues–
11	Eleven	30	Wednes–
12	Twelve	31	Thurs–
13	Thir–	32	Fir–
14	Four–	33	Satur–
15	Fif–	34	–day
16	Six–	35	–teen
17	Seven–	36	Please set the day and time
18	Eight–	37	The telephone number is
19	Nine–	38	