

1.25G Spring-Latch SFP Transceiver

(30km transmission)

Members of Flexon™ Family

- ◆ Compatible with FCC 47 CFR Part 15, Class B
- ◆ Compatible with FDA 21 CFR 1040.10 and 1040.11, Class I
- ◆ Compatible with Telcordia GR-468-CORE



Description

Fiberxon's FTM-5112C-SL30G, 1.25Gbps SFP transceivers are high performance, cost effective modules. They are designed for Gigabit Ethernet applications for 30km distance with SMF.

The transceiver consists of two sections: The transmitter section incorporates a DFB laser. And the receiver section consists of a PIN photodiode integrated with a trans-impedance preamplifier (TIA). All modules satisfy class I laser safety requirements.

The optical output can be disabled by a TTL logic high-level input of Tx Disable. Tx Fault is provided to indicate that degradation of the laser. Loss of signal (LOS) output is provided to indicate the loss of an input optical signal of receiver.

The standard serial ID information compatible SFP MSA describes the transceiver's capabilities, standard interfaces, manufacturer and other information. The host equipment can access this information via the 2-wire serial CMOS EEPROM protocol. For further information, please refer to SFP Multi-Source Agreement (MSA).

FTM-5112C-SL30G is compliant with RoHS.

Features

- ◆ 1.25Gbps bi-directional data links
- ◆ 30km transmission distance with SMF
- ◆ 1550nm DFB laser transmitter
- ◆ SFP MSA package with LC optical receptacle
- ◆ With lever latch for high density application
- ◆ Single +3.3V power supply
- ◆ Hot-pluggable capability
- ◆ Low power dissipation
- ◆ Very low EMI and excellent ESD protection
- ◆ Class I laser product
- ◆ Monitoring interface compatible with SFF-8472
- ◆ Operation case temperature: 0°C to 70°C

Applications

- ◆ Switch to Switch interface
- ◆ Switched backplane applications
- ◆ Router/Server interface
- ◆ Other optical transmission systems

Standard

- ◆ Compatible with SFP MSA
- ◆ Compatible with IEEE 802.3

Regulatory Compliance

The transceivers have been tested according to American and European product safety and electromagnetic compatibility regulations (See Table 1). For further information regarding regulatory certification, please refer to Flexon™ regulatory specification and safety guidelines, or contact with Fiberxon, Inc. America sales office listed at the end of the documentation.

Table 1 - Regulatory Compliance

Feature	Standard	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883E Method 3015.7	Class 2(>2000 V)
Electrostatic Discharge (ESD) to the Duplex LC Receptacle	IEC 61000-4-2 GR-1089-CORE	Compatible with standards
Electromagnetic Interference (EMI)	FCC Part 15 Class B EN55022 Class B (CISPR 22B) VCCI Class B	Compatible with standards
Immunity	IEC 61000-4-3	Compatible with standards
Laser Eye Safety	FDA 21CFR 1040.10 and 1040.11 EN60950, EN (IEC) 60825-1,2	Compatible with Class I laser product.
Component Recognition	UL and CSA	Compatible with standards
RoHS	2002/95/EC 4.1&4.2	Compliant with standards

Absolute Maximum Ratings

Stress in excess of the maximum absolute ratings can cause permanent damage to the module.

Table 2 - Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_S	-40	+85	°C
Supply Voltage	V_{CC}	-0.5	3.6	V
Operating Relative Humidity	-	5	95	%

Recommended Operating Conditions

Table 3- Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Case Temperature	T_C	0		+70	°C
Power Supply Voltage	V_{CC}	3.13		3.47	V

Power Supply Current	I_{CC}	220	300	mA
Date Rate	Gigabit Ethernet	1.25		Gbps
Fiber Length on 9/125 μ m SMF	L	30 ^{note}		km

Note:

The transmission distance is indicative only. Please refer to the Optical Characteristics in Table 4 to calculate the exact distance based on specific conditions in your application.

Optical and Electrical Characteristics

Table 4 - Optical and Electrical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes	
Transmitter							
Centre Wavelength	λ_C	1480	1550	1580	nm		
Average Output Power	P_{Out}	-9.5		-3	dBm	1	
P_{Out} @TX Disable Asserted	P_{Out}			-45	dBm	1	
Spectral Width (-20dB)	$\Delta\lambda$			1	nm		
Side Mode Suppression Ratio	SMSR	30			dB		
Extinction Ratio	EX	9			dB		
Rise/Fall Time (20%~80%)	t_r/t_f			0.26	ns	2	
Total Jitter	1.25G T_J			0.431	UI	3	
Output Optical Eye		IEEE 802.3z Compliant					4
Data Input Swing Differential	V_{IN}	300		2400	mV	5	
Input Differential Impedance	Z_{IN}	90	100	110	Ω		
TX Disable	Disable	2.0		Vcc	V		
	Enable	0		0.8	V		
TX Fault	Fault	2.0		Vcc+0.3	V		
	Normal	0		0.8	V		
Receiver							
Centre Wavelength	λ_C	1260		1580	nm		
Receiver Sensitivity				-20	dBm	6	
Receiver Overload		-3			dBm	6	
Return Loss		12			dB		
LOS De-Assert	LOS_D			-20	dBm		
LOS Assert	LOS_A	-31			dBm		
LOS Hysteresis		1		4	dB		
Data Output Swing Differential	V_{OUT}	370		2000	mV	5	
LOS	High	2.0		Vcc+0.3	V		
	Low	0		0.8	V		

Notes:

1. The optical power is launched into SMF.
2. Unfiltered, measured with a PRBS 2^7-1 test pattern @1.25Gbps
3. Measured with a PRBS 2^7-1 test pattern@1.25Gbps, meet the specified maximum output jitter

requirements if the specified maximum input jitter is present.

4. Measured with a PRBS 2⁷-1 test pattern @1.25Gbps.
5. CML logic, internally AC coupled.
6. Measured with a PRBS 2⁷-1 test pattern @1.25Gbps, worst-case extinction ratio, BER $\leq 1 \times 10^{-12}$.

EEPROM Information

The SFP MSA defines a 256-byte memory map in EEPROM describing the transceiver's capabilities, standard interfaces, manufacturer, and other information, which is accessible over a 2-wire serial interface at the 8-bit address 1010000X (A0h). The memory contents refer to Table 5.

Table 5 - EEPROM Serial ID Memory Contents (A0h)

Addr.	Field Size (Bytes)	Name of Field	Hex	Description
0	1	Identifier	03	SFP
1	1	Ext. Identifier	04	MOD4
2	1	Connector	07	LC
3—10	8	Transceiver	00 00 00 02 12 00 01 01	Transmitter Code
11	1	Encoding	01	8B10B
12	1	BR, nominal	0D	1.25Gbps
13	1	Reserved	00	
14	1	Length (9um)-km	1E	30km
15	1	Length (9um)	FF	
16	1	Length (50um)	00	
17	1	Length (62.5um)	00	
18	1	Length (copper)	00	
19	1	Reserved	00	
20—35	16	Vendor name	46 49 42 45 52 58 4F 4E 20 49 4E 43 2E 20 20 20	"FIBERXON INC." (ASC II)
36	1	Reserved	00	
37—39	3	Vendor OUI	00 00 00	
40—55	16	Vendor PN	46 54 4D 2D 35 31 31 32 43 2D 53 4C 33 30 47 20	"FTM-5112C-SL30G" (ASC II)
56—59	4	Vendor rev	xx xx 20 20	ASC II ("31 30 20 20" means 1.0 revision)
60-61	2	Wavelength	06 0E	1550nm
62	1	Reserved	00	
63	1	CC BASE	xx	Check sum of bytes 0 - 62
64—65	2	Options	00 1A	LOS, TX_FAULT and TX_DISABLE
66	1	BR, max	00	
67	1	BR, min	00	
68—83	16	Vendor SN	xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx	ASC II
84—91	8	Vendor date	xx xx xx xx xx xx 20 20	Year(2 bytes), Month(2 bytes), Day (2 bytes)

		code		
92	1	Diagnostic type	68	Diagnostics(Int.Cal)
93	1	Enhanced option	B0	Diagnostics(Optional Alarm/warning flags, Soft TX_FAULT and Soft TX_LOS monitoring)
94	1	SFF-8472	02	Diagnostics(SFF-8472 Rev 9.4)
95	1	CC_EXT	xx	Check sum of bytes 64 - 94
96—255	160	Vendor specific		

Note: The “xx” byte should be filled in according to practical case. For more information, please refer to the related document of SFP Multi-Source Agreement (MSA).

Monitoring Specification

The digital diagnostic monitoring interface also defines another 256-byte memory map in EEPROM, which makes use of the 8 bit address 1010001X (A2h). Please see Figure 1. For detail EEPROM information, please refer to the related document of SFF-8472 Rev 9.4. The monitoring specification of this product is described in Table 6.

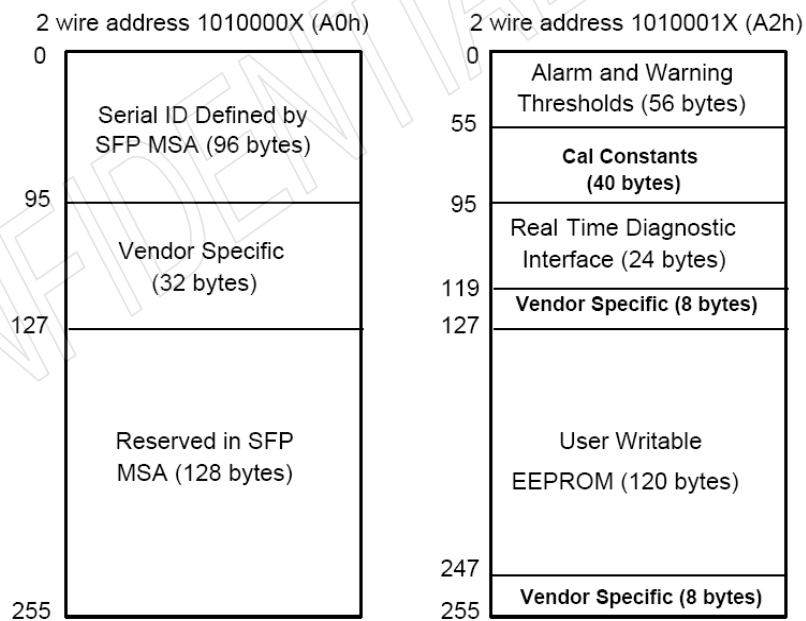


Figure 1, EEPROM Memory Map Specific Data Field Descriptions

Table 6 - Monitoring Specification

Parameter	Range	Accuracy	Calibration*
Temperature	-5 to +90°C	±3°C	Internal
Voltage	2.97 to 3.63V	±3%	Internal
Bias Current	3 to 100mA	±10%	Internal
TX Power	-9.5 to -3dBm	±3dB	Internal

RX Power	-20 to -3dBm	±3dB	Internal
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Recommended Host Board Power Supply Circuit

Figure 2 shows the recommended host board power supply circuit.

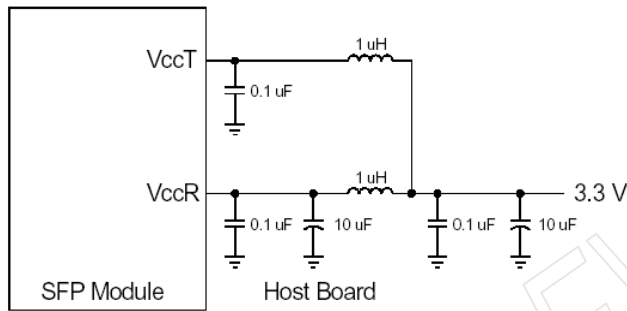


Figure 2, Recommended Host Board Power Supply Circuit

Recommended Interface Circuit

Figure 3 shows the recommended interface circuit.

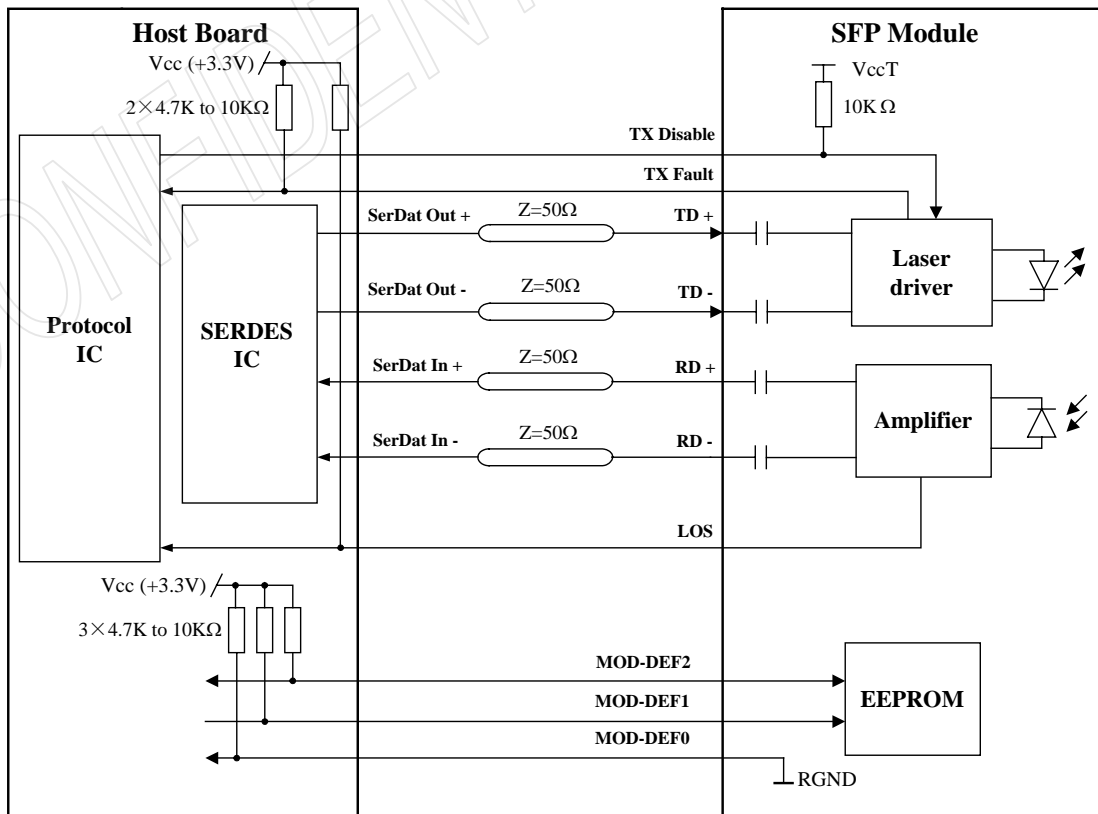


Figure 3, Recommended Interface Circuit

Pin Definitions

Figure 4 below shows the pin numbering of SFP electrical interface. The pin functions are described in Table 7 with some accompanying notes.

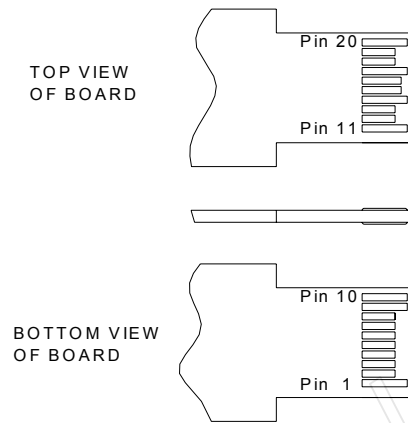


Figure 4, Pin View

Table 7– Pin Function Definitions

Pin No.	Name	Function	Plug Seq.	Notes
1	VeeT	Transmitter Ground	1	
2	TX Fault	Transmitter Fault Indication	3	Note 1
3	TX Disable	Transmitter Disable	3	Note 2
4	MOD-DEF2	Module Definition 2	3	Note 3
5	MOD-DEF1	Module Definition 1	3	Note 3
6	MOD-DEF0	Module Definition 0	3	Note 3
7	Rate Select	Not Connected	3	
8	LOS	Loss of Signal	3	Note 4
9	VeeR	Receiver Ground	1	
10	VeeR	Receiver Ground	1	
11	VeeR	Receiver Ground	1	
12	RD-	Inv. Received Data Out	3	Note 5
13	RD+	Received Data Out	3	Note 5
14	VeeR	Receiver Ground	1	
15	VccR	Receiver Power	2	
16	VccT	Transmitter Power	2	
17	VeeT	Transmitter Ground	1	
18	TD+	Transmit Data In	3	Note 6
19	TD-	Inv. Transmit Data In	3	Note 6
20	VeeT	Transmitter Ground	1	

Notes:

- TX Fault is an open collector output, which should be pulled up with a 4.7k~10k Ω resistor on the host board to a voltage between 2.0V and Vcc+0.3V. Logic 0 indicates normal operation; logic 1 indicates a laser fault of some kind. In the low state, the output will be pulled to less than 0.8V.
- TX Disable is an input that is used to shut down the transmitter optical output. It is pulled up within the module with a 4.7k~10k Ω resistor. Its states are:

Low (0~0.8V):	Transmitter on
(>0.8V, <2.0V):	Undefined
High (2.0~3.465V):	Transmitter Disabled
Open:	Transmitter Disabled
- MOD-DEF 0,1,2 are the module definition pins. They should be pulled up with a 4.7k~10k Ω resistor on the host board. The pull-up voltage shall be VccT or VccR.
 - MOD-DEF 0 is grounded by the module to indicate that the module is present
 - MOD-DEF 1 is the clock line of two wire serial interface for serial ID
 - MOD-DEF 2 is the data line of two wire serial interface for serial ID
- LOS is an open collector output, which should be pulled up with a 4.7k~10k Ω resistor on the host board to a voltage between 2.0V and Vcc+0.3V. Logic 0 indicates normal operation; logic 1 indicates loss of signal. In the low state, the output will be pulled to less than 0.8V.
- These are the differential receiver output. They are internally AC-coupled 100 Ω differential lines which should be terminated with 100 Ω (differential) at the user SERDES.
- These are the differential transmitter inputs. They are AC-coupled, differential lines with 100 Ω differential termination inside the module.

Mechanical Design Diagram

The mechanical design diagram is shown in Figure 5

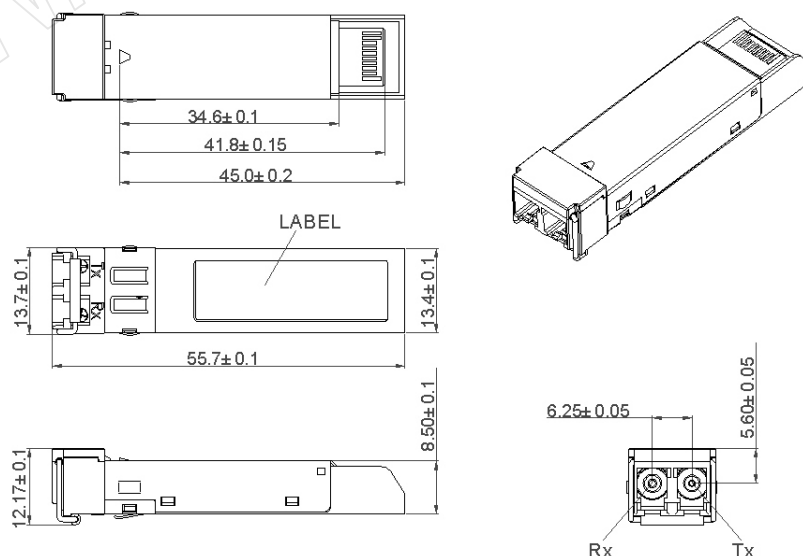
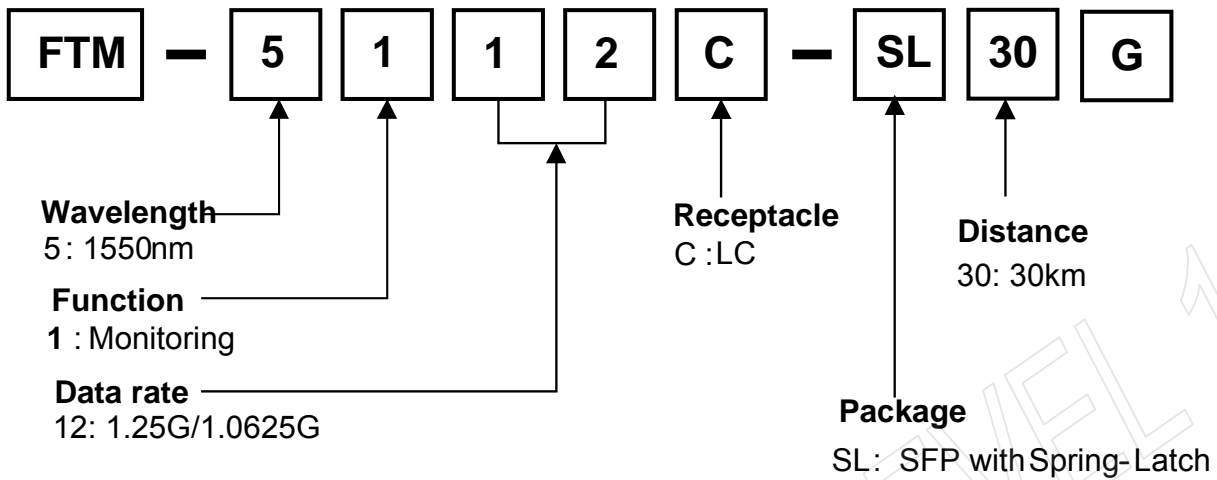


Figure 5, Mechanical Design Diagram of the SFP with Spring-Latch

Ordering information



Part No.	Product Description
FTM-5112C-SL30G	1550nm, 1.25Gbps, 30km, SFP with Spring-Latch, 0°C~+70°C

Related Documents

For further information, please refer to the following documents:

- *Fiberxon Spring-Latch SFP Installation Guide*
- *Fiberxon SFP Application Notes*
- *SFP Multi-Source Agreement (MSA)*

Obtaining Document

You can visit our website:

<http://www.fiberxon.com>

Or contact with Fiberxon, Inc. America Sales Office listed at the end of documentation to get the latest documents.

Revision History

Revision	Initiate	Review	Approve	Subject	Release Date
Rev. 1a	Henry.xiao	Simon.Jiang	Walker.We	Initial datasheet	Jan. 10, 2007

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Contact

U.S.A. Headquarter:

5201 Great America Parkway, Suite 340

Santa Clara, CA 95054

U. S. A.

Tel: 408-562-6288

Fax: 408-562-6289

Or visit our website: <http://www.fiberxon.com>