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FUJITSU

PRODUCT PROFILE

ET2600VH
ECL Gate Array with Mixed ECL/TTL I/O

DESCRIPTION

Fujitsu's ET2600VH array is manufactured using ultra-high speed LSI circuit design and mass-production techniques developed for use in Fujitsu's ultra-large and supercomputers.

The ET2600VH has the internal gate configuration of an ECL circuit and I/O buffers that offer mixed ECL/TTL capability. It can therefore facilitate large scale integration and increase speed in systems in which TTL, CMOS, and ECL devices are used together, without the need for a level conversion device.

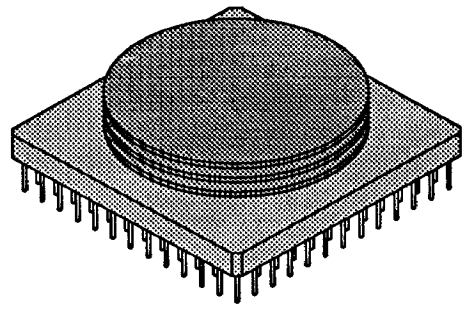
Two types of internal cells are used in the ET2600VH: (1) the normal type with 90 ps typical no-load propagation delay, and (2) the drive type, with only 75 ps typical no-load propagation delay, allowing designers to optimize speed/power trade-offs. The ET2600VH is especially well suited for such high-end applications as communication and transmission systems and high-performance measurement and test instrumentation.

FEATURES

- Ultra High Speed Performance
  - Normal Type cell:
    90 ps/gate (I_{CS} = 0.25 mA, I_{EF} = 0.5 mA, no load)
    220 ps/gate (I_{CS} = 0.25 mA, I_{EF} = 1.0 mA, typical load, L = 1.5 mm, F/I = F/O = 3)
  - Driver type cell:
    75 ps/gates (I_{CS} = 0.8 mA, I_{EF} = 0.8 mA, no load)
    160 ps/gate (I_{CS} = 0.8 mA, I_{EF} = 1.6 mA, typical load, L = 1.5 mm, F/I = F/O = 3)
  - TTL input buffer
    1.6 ns/gate (TTL type)
    1.3 ns/gate (mixed ECL/TTL type)
  - TTL output buffer (C_L = 15 pF)
    3.2 ns/gate (TTL type)
    2.9 ns/gate (mixed ECL/TTL type)
  - ECL output buffer
    0.6 ns/gate
    Internal toggle frequency 2.0 GHz (maximum)
- Low Clock Skew
  - max. 150 ps (typ.) per internal macro with clock based on fixed wiring
- High Operation Frequency
  - ECL Input Buffer: 1 GHz
    ECL Output Buffer: 650 MHz (50 Ω termination)
    ECL Output Buffer: 300 MHz (100 Ω termination)
  - TTL Input Buffer: 150 MHz
    TTL Output Buffer: 80 MHz (CL = 15 pF, I_{OL} = 8 mA)
    TTL Output Buffer: 40 MHz (CL = 50 pF, I_{OL} = 8 mA)
- 2544 Internal Gates
- 104 I/O Buffers (72 ECL outputs, max.; 32 TTL outputs, max.)
- Power Dissipation: 5 W
- Available in Ceramic PGA-121 and QFP-124
- I/O options: ECL 10KH, ECL 100K, TTL, and mixed ECL/TTL

ET2600VH Gate Array Summary	
Maximum Internal Gates[1]	2,544
Maximum I/O	104
Maximum Outputs	72

Note: [1]2,016 internal gates + 528 driver gates



121-pin Ceramic Pin Grid Array Package