DPS256X32AV3

HIGH SPEED 256K X 32 CMOS SRAM VERSA-STACK

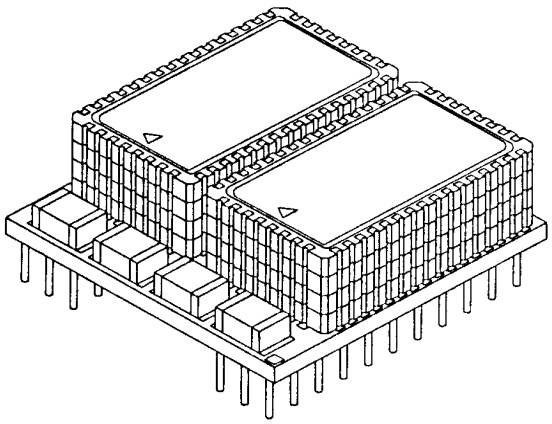
PRELIMINARY

DESCRIPTION:

The DPS256X32AV3 "VERSA-STACK" module is a revolutionary new high speed memory subsystem using Dense-Pac Microsystems' ceramic Stackable Leadless Chip Carriers (SLCC) mounted on a co-fired ceramic substrate. It offers 8 Megabits of SRAM in a package envelope of 1.09 x 1.09 x 0.40 inches.

The DPS256X32AV3 contains eight individual 128K x 8 SRAMs, packaged in their own hermetically sealed SLCCs making the module suitable for commercial, industrial and military applications.

By using SLCCs, the "Versa-Stack" family of modules offers a higher board density of memory than available with conventional through-hole, surface mount, module, or hybrid techniques.

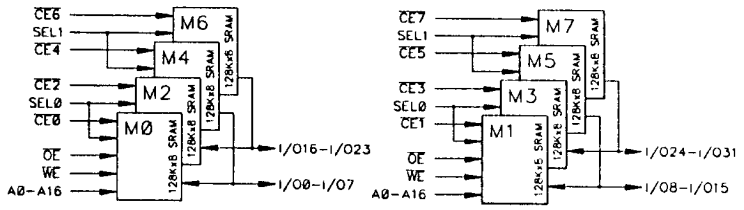


FEATURES:

- Organizations Available:
  256K x 32, 512K x 16, or 1024K x 8
- Access Times:
  35*, 45, 55, 70ns
- Fully Static Operation - No clock or refresh required
- Low Power Dissipation:
  500µW (typ.) Full Standby
  550mW (typ.) Operating (x8)
- Single +5V Power Supply, ±10% Tolerance
- TTL Compatible
- Common Data Inputs and Outputs
- Low Data Retention Current:
  40µA typ. (2.0V)
- 66-Pin PGA "VERSA-STACK" Package

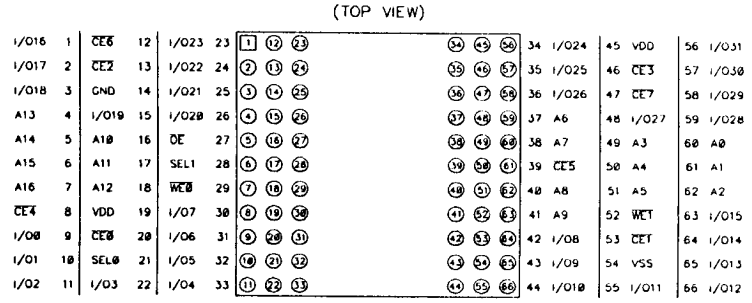
* Commercial only.

FUNCTIONAL BLOCK DIAGRAM



PIN-OUT DIAGRAM

(TOP VIEW)



I/O16	1	CE6	12	I/O23	23	34	I/O24	45	VDD	56	I/O31
I/O17	2	CE2	13	I/O22	24	35	I/O25	46	CE3	57	I/O30
I/O18	3	GND	14	I/O21	25	36	I/O26	47	CE7	58	I/O29
A13	4	I/O19	15	I/O20	26	37	A6	48	I/O27	59	I/O28
A14	5	A10	16	OE	27	38	A7	49	A3	60	A0
A15	6	A11	17	SEL1	28	39	CE5	50	A4	61	A1
A16	7	A12	18	WE0	29	40	A8	51	A5	62	A2
CE4	8	VDD	19	I/O7	30	41	A9	52	WE1	63	I/O15
I/O8	9	CE0	20	I/O6	31	42	I/O8	53	CE1	64	I/O14
I/O1	10	SEL0	21	I/O5	32	43	I/O9	54	VSS	65	I/O13
I/O2	11	I/O3	22	I/O4	33	44	I/O10	55	I/O11	66	I/O12

PIN NAMES	
A0 - A16	Address Inputs
I/O0 - I/O31	Data Input/Output
$\overline{CE0}$ - $\overline{CE7}$	Low Chip Enables
SEL0, SEL1	High Chip Enables
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{DD}	Power (+5V)
V_{SS}	Ground

PRELIMINARY

RECOMMENDED OPERATING RANGE[3]					
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage	2.2		V_{DD}+0.3	V
V_{IL}	Input LOW Voltage	-0.5[2]		0.8	V
T_A	Operating Temp.	-55	+25	+125	°C

DC OUTPUT CHARACTERISTICS					
Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{OH}	HIGH Voltage	I_{OH}= -1.0mA	2.4	-	V
V_{OL}	LOW Voltage	I_{OL}=2.1mA	-	0.4	V

ABSOLUTE MAXIMUM RATINGS[3]			
Symbol	Parameter	Value	Unit
T_{STC}	Storage Temperature	-65 to +150	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
V_{DD}	Supply Voltage [1]	-0.5 to +7.0	V
$V_{I/O}$	Input/Output Voltage [1]	-0.5 to V_{DD} +0.5	V

CAPACITANCE [4]: T_A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C_{ADR}	Address Input	100	pF	V_{IN}[2] = 0V
C_{CE}	Chip Enable	30		
C_{SEL}	Active High Chip Select	40		
C_{WE}	Write Enable	50		
C_{OE}	Output Enable	90		
$C_{I/O}$	Data Input/Output	30		

TRUTH TABLE						
Mode	SEL	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Pin	Supply Current
Not Selected	L	X	X	X	HIGH-Z	Standby
Not Selected	X	H	X	X	HIGH-Z	Standby
D_{OUT} Disable	H	L	H	H	HIGH-Z	Active
Read	H	L	H	L	D_{OUT}	Active
Write	H	L	L	X	D_{IN}	Active

H=HIGH L=LOW X=Don't Care

DC OPERATING CHARACTERISTICS: Over operating ranges											
Symbol	Characteristics	Test Conditions		TYP. (*)	C		I		M		Unit
					Min.	Max.	Min.	Max.	Min.	Max.	
I_{IN}	Input Leakage Current	V_{IN} = 0V to V_{DD}		-	-20	+20	-20	+20	-20	+20	µA
I_{OUT}	Output Leakage Current	$V_{I/O}$ = 0V to V_{DD}, $\overline{CE}$ or $\overline{OE}$ = V_{IH}, or $\overline{WE}$ = V_{IL}		-	-4	+4	-4	+4	-4	+4	µA
I_{CC1}	Active Supply Current	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA	X8	80		140		185		185	mA
			X16	115		200		250		250	
			X32	180		320		380		380	
I_{CC2}	Operating Supply Current	Cycle = min., Duty = 100% I_{OUT} = 0mA	X8	110		180		225		225	mA
			X16	175		280		330		330	
			X32	300		480		540		540	
I_{SB1}	Full Standby Supply Current (CMOS)	V_{IN} ≥ V_{DD} -0.2V or V_{IN} ≤ V_{SS} +0.2V		0.1		8.0		16.0		24.0	mA
I_{SB2}	Standby Current (TTL)	$\overline{CE}$ = V_{IH}		48		80		120		120	mA
I_{DR3}	Data Retention Supply Current (3V)	V_{DR} = 3V, $\overline{CE}$ ≥ V_{DR} -0.2V, or SEL ≤ 0.2V		80		960		1600		5600	µA
I_{DR2}	Data Retention Supply Current (2V)	V_{DR} = 2V, $\overline{CE}$ ≥ V_{DR} -0.2V, SEL ≥ V_{DR} -0.2V or SEL ≤ 0.2V		40		800		1360		4000	µA
V_{OL}	Output Low Voltage	I_{OUT} = 2.1mA		-		0.4		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OUT} = -1.0mA		-	2.4		2.4		2.4		V

* Typical measurements made at +25°C, Cycle = min., V_{DD} = 5.0V.

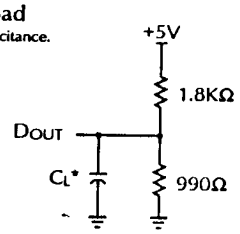
PRELIMINARY

AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V

OUTPUT LOAD		
Load	C_L	Parameters Measured
1	100 pF	except t_{LZ1}, t_{LZ2}, t_{HZ1}, t_{HZ2}, t_{OHZ}, t_{OLZ}, and t_{WHZ}
2	5 pF	t_{LZ1}, t_{LZ2}, t_{HZ1}, t_{HZ2}, t_{OHZ}, t_{OLZ}, and t_{WHZ}

Figure 1. Output Load

* Including Probe and Jig Capacitance.



AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges

No.	Symbol	Parameter	-35†		-45		-55		-70		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	35		45		55		70		ns
2	t_{AA}	Address Access Time		35		45		55		70	ns
3	t_{CO1}	Chip Enable ($\overline{CE}$) to Output Valid		35		45		55		70	ns
4	t_{CO2}	Chip Enable (SEL) to Output Valid		35		45		55		70	ns
5	t_{OE}	Output Enable to Output Valid		20		25		30		40	ns
6	t_{LZ1}	Chip Enable ($\overline{CE}$) to Output in LOW-Z [4, 5]	5		5		5		5		ns
7	t_{LZ2}	Chip Enable (SEL) to Output in LOW-Z [4, 5]	5		5		5		5		ns
8	t_{OLZ}	Output Enable to Output in LOW-Z [4, 5]	0		0		0		0		ns
9	t_{HZ1}	Chip Enable ($\overline{CE}$) to Output in HIGH-Z [4, 5]		15		20		25		30	ns
10	t_{HZ2}	Chip Enable (SEL) to Output in HIGH-Z [4, 5]		15		20		25		30	ns
11	t_{OHZ}	Output Enable to Output in HIGH-Z [4, 5]		15		20		25		30	ns
12	t_{OH}	Output Hold from Address Change	5		5		5		10		ns

AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE [6,7]: Over operating ranges

No.	Symbol	Parameter	-35†		-45		-55		-70		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
13	t_{WC}	Write Cycle Time	35		45		55		70		ns
14	t_{AW}	Address Valid to End of Write	30		40		45		65		ns
15	t_{CW}	Chip Enable to End of Write	30		40		45		65		ns
16	t_{AS}	Address Set-up Time***	0		0		0		0		ns
17	t_{WP}	Write Pulse Width	30		35		40		55		ns
18	t_{WR}	Write Recovery Time	5		5		5		5		ns
19	t_{WHZ}	Write Enable to Output in HIGH-Z [4, 5]		15		20		25		30	ns
20	t_{DW}	Data to Write Time Overlap	18		20		25		35		ns
21	t_{DH}	Data Hold from Write Time	0		0		0		0		ns
22	t_{OW}	Output Active from End of Write	5		5		5		5		ns

*** Valid for both Read and Write Cycles.

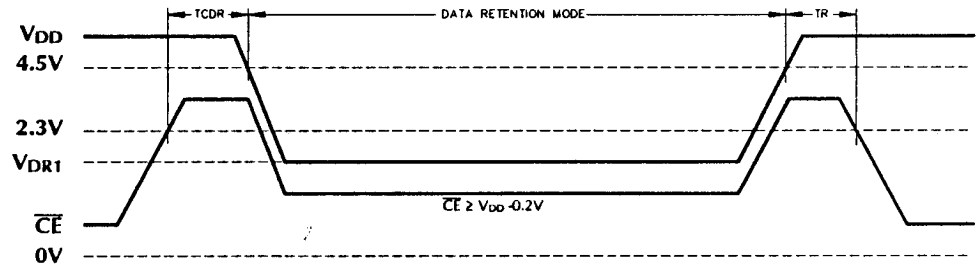
† Commercial only.

Data Retention AC Characteristics

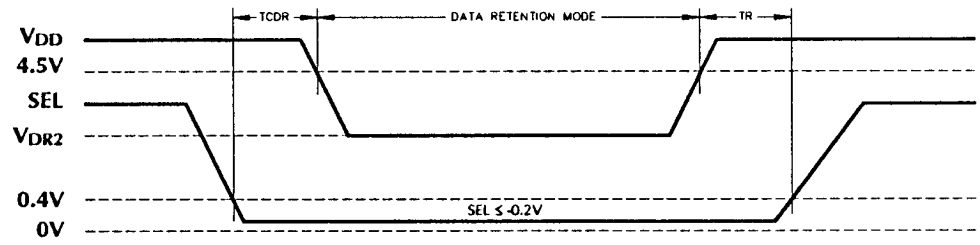
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DR}	V_{DD} for Data Retention	$\overline{CE} \geq V_{DD}$ -0.2V, SEL $\geq V_{DD}$ -0.2V or SEL $\leq V_{DD}$ 0.2V	2.0	-	-	V
t_{CDR}	Chip Disable to Data Retention Time	See Retention Waveform	0	-	-	ns
t_R	Operation Recovery Time	See Retention Waveform	5	-	-	ms

PRELIMINARY

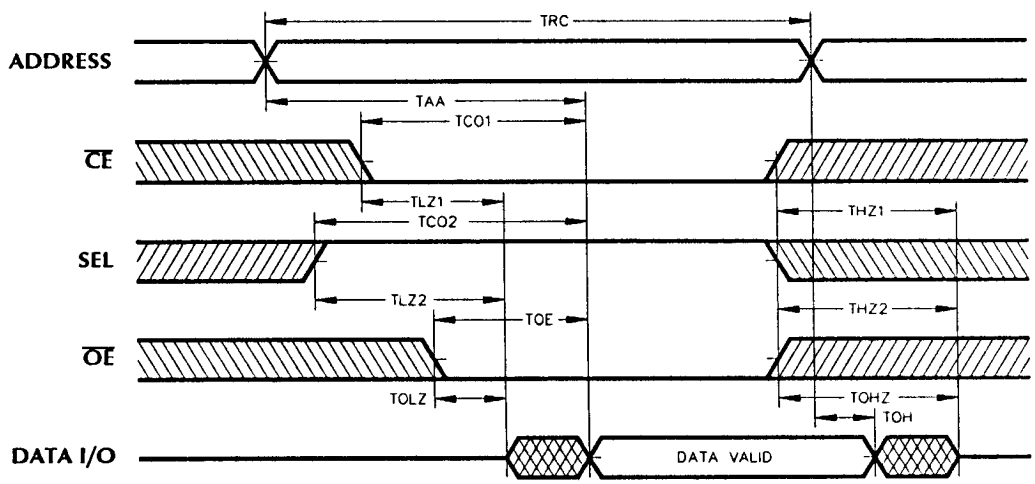
DATA RETENTION WAVEFORM: $\overline{CE}$ Controlled.



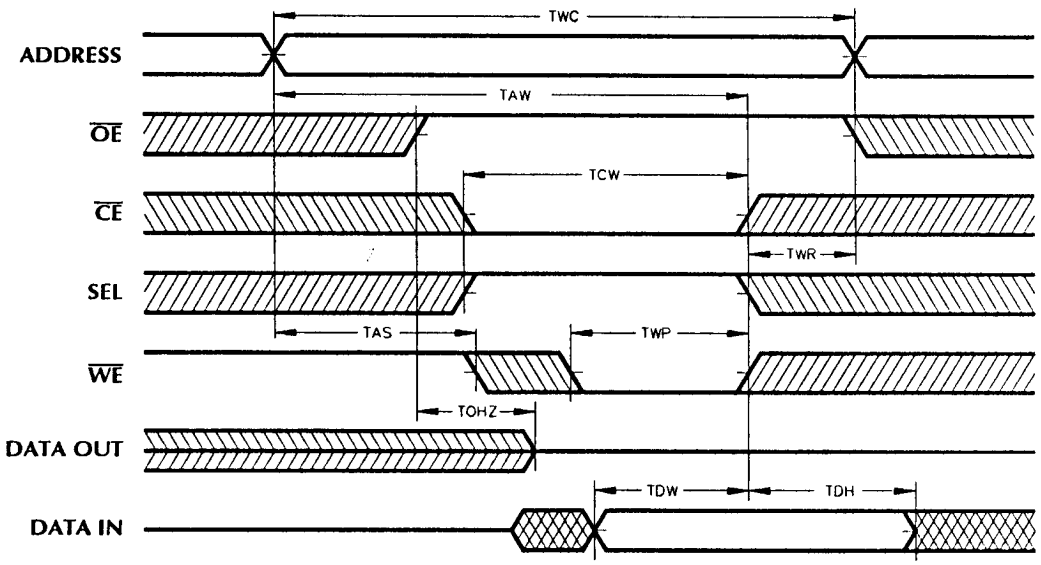
DATA RETENTION WAVEFORM: [8] SEL Controlled.



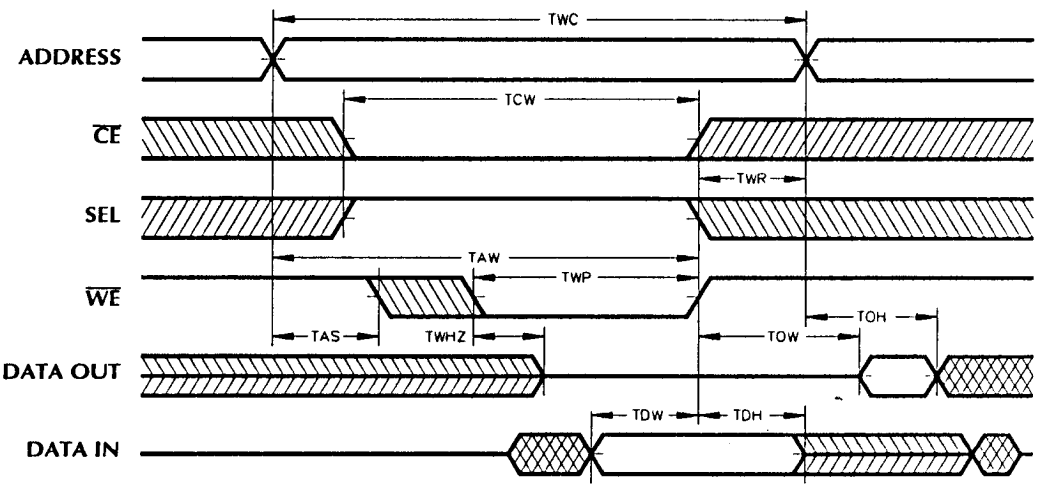
READ CYCLE



WRITE CYCLE 1: $\overline{WE}$ Controlled. $\overline{OE}$ Clocked.



WRITE CYCLE 2: $\overline{CE}$ Controlled. $\overline{OE}$ is LOW.



PRELIMINARY

ORDERING INFORMATION

DP S256X32A V3 – XX X

PREFIX: DP = DENSE-PAC

DEVICE TYPE: S256X32A = HIGH SPEED CMOS SRAM 256Kx32

PACKAGE: V3 = 66 PIN GRID ARRAY (PGA)/(3-D) VERSA-STACK

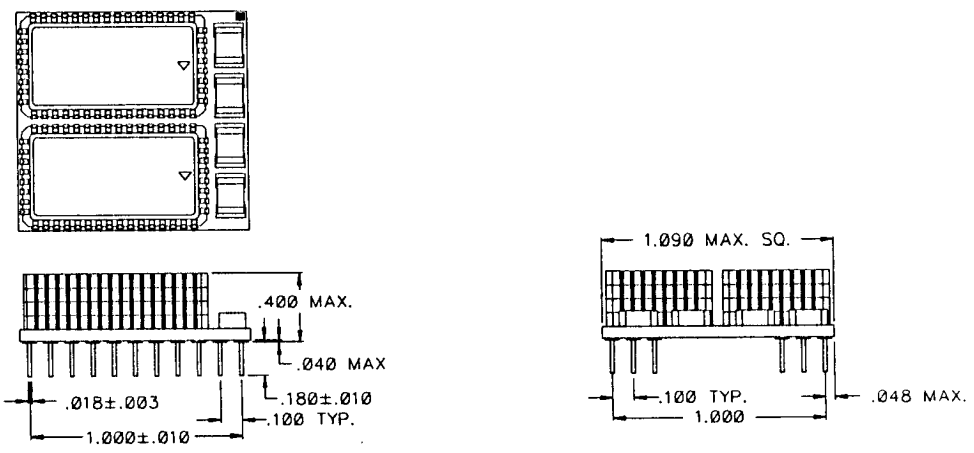
SPEED: 35 = 35ns (COMMERCIAL ONLY); 45 = 45ns; 55 = 55ns; 70 = 70ns

GRADE: C = COMMERCIAL 0°C to +70°C; I = INDUSTRIAL -40°C to +85°C; M = MILITARY -55°C to +125°C; B = MIL-PROCESSED -55°C to +125°C

NOTES:

1. All voltages are with respect to V_{SS}.
2. -2.0V min. for pulse width less than 20ns (V_{IL} min. = -0.5V at DC level).
3. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of ±500mV from steady state voltage.
6. When $\overline{OE}$ and $\overline{CE}$ are LOW and $\overline{WE}$ is HIGH, I/O pins are in the output state,and input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when $\overline{WE}$ is LOW.
8. SEL controls address buffer, $\overline{WE}$ buffer, $\overline{CE}$ buffer and $\overline{OE}$ buffer and D_{IN} buffer. If SEL controls Data Retention Mode, V_{IN} levels (Address, $\overline{WE}$, $\overline{OE}$, $\overline{CE}$, I/O) can be in the high impedance state. If $\overline{CE}$ controls Data Retention Mode, SEL must be SEL ≥ V_{DD} -0.2V or 0V ≤ SEL ≤ 0.2V. The other input levels (Address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the High Impedance State.

MECHANICAL DRAWING



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