AmPAL23S8

20-Pin IMOX™ PAL Device-Based Sequencer

Distinctive Characteristics

- 14 Registers
  - 4 Output Logic Macrocells (OLMs)
  - 4 Output Registers
  - 6 Buried State Registers (BSRs)
- 23 possible array inputs and 8 outputs in a 20-pin package
- 33-MHz external/40-MHz internal cycle time
- Variable product term (PT) distribution for increased design flexibility
- Asynchronous and synchronous outputs supported for both Mealy- and Moore-type state-machine implementations

- Individually user-programmable Output Enable (OE) PTs with polarity control
- PTs for observing the BSRs on 6 of the output pins
- Separate PTs for common Synchronous PRESET and common Asynchronous RESET of all registers
- PRELOAD available on all registers for added test capability
- 99.9% post programming functional yield (PPFY) is due to the testability of this and all other AMD PAL devices.
- Platinum-Silicide fuse technology produces the most reliable bipolar programmable devices available today

General Description

The AmPAL23S8 is the first programmable array logic (PAL)-based sequencer device. It utilizes the familiar sum-of-products (AND-OR) logic structure, allowing users to customize logic functions by programming the device for specific applications. The AmPAL23S8 combines the ease of use of the familiar 20-pin PAL devices with the advanced "macrocell" concept introduced in the AmPAL22V10, as well as six Buried State Registers (BSRs).

The AmPAL23S8 provides up to twenty-three array inputs and eight outputs. Four of the outputs are Output Logic Macrocells (OLMs) capable of being individually programmed as "combinatorial" or "registered," with active-HIGH or active-LOW polarity on each output. The other four are "registered" outputs, also capable of being programmed for active-HIGH or LOW polarity. All the flexibility on the outputs result in the simplification of logic design. The need to perform "DeMorgan's Law" on equations to have them fit into a PAL device is now a thing of the past. Each of the eight output registers can also be used dynamically as an input or output for greater design flexibility.
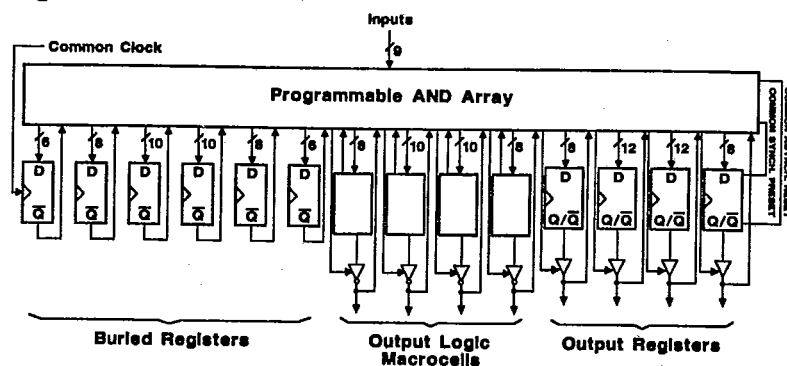
The AmPAL23S8 also offers designers increased flexibility and control over Output Enable (OE) functions. Each output is logically controlled by an OE product term (PT), with programmable OE polarity control. This allows the designer to use more complex control than previously available.

The six BSRs provide designers with enhanced logic power for sequencer applications. These registers are not only available to the system designer for use in sequencer applications (without the expense of a valuable I/O pin), but they may also be observed on the output pins during test. The observability of these registers on a programmable-logic sequencer adds to the list of features which make this device unique, simple to design with, and simple to debug.

System operation has been enhanced by the addition of Synchronous PRESET and Asynchronous RESET PTs. The AmPAL23S8 also incorporates the unique capability of PRELOADing the eight output registers and the BSRs to any desired state during testing. This is essential to permit full logical verification during test.
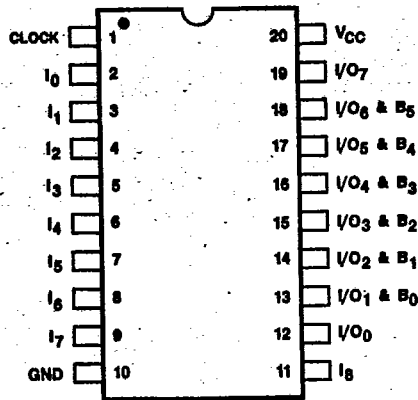
Block Diagram

BD006800

Monolithic MMI Memories

Connection Diagram

Top View

Pin			Pin
CLOCK	1	20	V_{CC}
I_0	2	19	I/O_7
I_1	3	18	I/O_6 & B_5
I_2	4	17	I/O_5 & B_4
I_3	5	16	I/O_4 & B_3
I_4	6	15	I/O_3 & B_2
I_5	7	14	I/O_2 & B_1
I_6	8	13	I/O_1 & B_0
I_7	9	12	I/O_0
GND	10	11	I_8

CD009870

Note: Pin 1 is marked for orientation.

Pin Description

V_{CC} = Supply Voltage

GND = Ground

CLOCK = Clock Pin

$I_0 - I_8$ = Dedicated Input Pins (9)

$I/O_0 - I/O_7$ = Bidirectional I/O Pins (8)
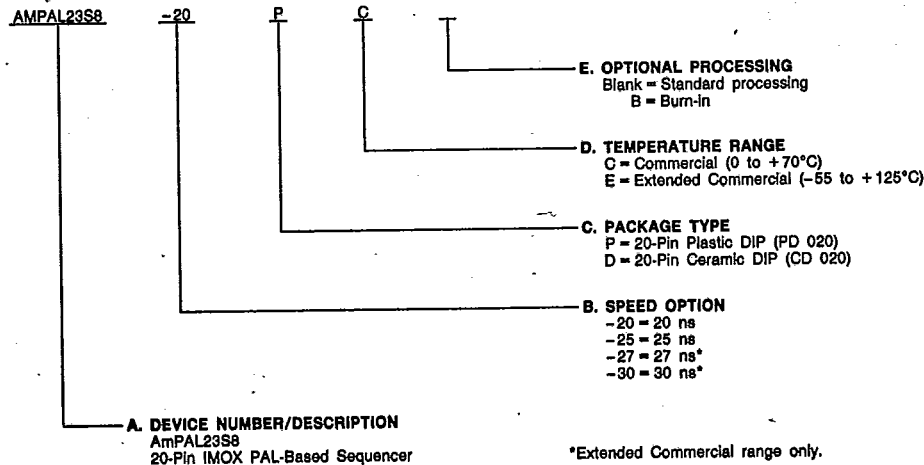
$B_0 - B_5$ = Observability Pins for BSRs (6)

Ordering Information

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: A. Device Number
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing

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AMPAL23S8    -20    P    C    ▢
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E. OPTIONAL PROCESSING
Blank = Standard processing
B = Burn-in

D. TEMPERATURE RANGE
C = Commercial (0 to +70°C)
E = Extended Commercial (−55 to +125°C)

C. PACKAGE TYPE
P = 20-Pin Plastic DIP (PD 020)
D = 20-Pin Ceramic DIP (CD 020)

B. SPEED OPTION
−20 = 20 ns
−25 = 25 ns
−27 = 27 ns*
−30 = 30 ns*

A. DEVICE NUMBER/DESCRIPTION
AmPAL23S8
20-Pin IMOX PAL-Based Sequencer

*Extended Commercial range only.

Valid Combinations

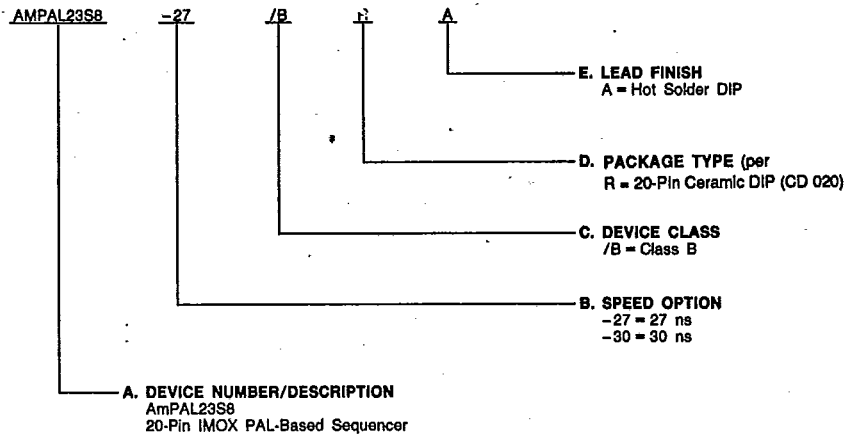| Valid Combinations	
AMPAL23S8-20	PC, DC, DCB
AMPAL23S8-25	PC, DC, DCB, DE, DEB
AMPAL23S8-27	DE, DEB
AMPAL23S8-30	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Ordering Information (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

  A. Device Number
  B. Speed Option (if applicable)
  C. Device Class
  D. Package Type
  E. Lead Finish

AMPAL23S8   –27   /B   R   A

E. LEAD FINISH
A = Hot Solder DIP

D. PACKAGE TYPE (per
R = 20-Pin Ceramic DIP (CD 020)

C. DEVICE CLASS
/B = Class B

B. SPEED OPTION
–27 = 27 ns
–30 = 30 ns

A. DEVICE NUMBER/DESCRIPTION
AmPAL23S8
20-Pin IMOX PAL-Based Sequencer

Valid Combinations	
AMPAL23S8-27	/BRA
AMPAL23S8-30	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A Tests consist of Subgroups: 1, 2, 3, 7, 8, 9, 10, 11

Functional Description

The AmPAL23S8 is an advanced bipolar programmable array logic (PAL)-based sequencer. It contains a programmable array organized in the familiar sum-of-products structure. The structure of this device makes it particularly ideal for state machine applications. Any design which employs the use of complex state functions is a prime candidate for the AmPAL23S8.

The block diagram on the front page shows the basic architecture of this device; a maximum of 23 array inputs and 8 outputs are available. The inputs are connected to a programmable AND array containing 135 product terms (PTs), of which 124 are logical PTs and 11 are control PTs. Before programming, the AND gates are connected to both the true and complement of every input. By selectively programming fuses, the AND gates may be connected to only the true input, the complement input, or to neither type of input, establishing a logical "don't care". When both the true and complement fuses are left intact, a logical FALSE results on the output of the AND gate. An AND gate with all fuses blown will assume the logical TRUE state. The outputs of the AND gates are connected to OR gates.

Variable Product Term (PT) Distribution

The number of AND gates assigned to each OR gate varies in a fixed manner for each output as shown in the logic diagram (Figure 5). The OR- gate outputs feed dedicated registers and macrocells. Each OR gate averages approximately ten PTs for output registers and macrocells. This gives the capability of using from eight to twelve logical PTs on one output in a single clock cycle (no feedback necessary). Buried state registers (BSRs) have an average of eight PTs per OR gate, providing the capability of using from six to ten logical PTs in one BSR in a single clock cycle.

Variable Output Architecture: Output Logic Macrocells (OLMs)

An innovation in logic design is the implementation on the AmPAL23S8 of variable output architecture on four of the outputs. These Output Logic Macrocells (OLMs) are user programmable for a great deal of design flexibility. Each of the four OLMs can be independently programmed for eight distinct configurations. The outputs can be either "registered" or "combinatorial;" they can also be individually programmed for active-HIGH or active-LOW polarity. Finally, the feedback paths which feed through the multiplexer back to the AND array can be programmed so that they originate either from the register or from the I/O pin. From the feedback multiplexer both the true and complement of the output going back to the array are available. All possible configurations of the OLMs are illustrated in Figures 4-1 through 4-8. For maximum flexibility, selection of output polarity and feedback path are kept independent of each other.

Output Registers

In addition to the four OLMs on the AmPAL23S8, there are also four output registers. The data on the output registers may be fed back to the array. When the output is disabled, the pin may be used as an external input. Since each of the eight outputs can obtain feedback from the pins associated with them, all eight of them provide the advantage of being usable dynamically as either inputs or outputs, significantly increasing design flexibility and possibilities.

Buried State Registers (BSRs)

The six observable Buried State Registers are one of the key features of the AmPAL23S8. All BSR outputs are fed back to the AND array, but they do not use up an output pin. The state of each BSR is, however, observable on an associated output pin by activating the user-programmable Observability product term as well as the appropriate Output Enable product term.

The extensive user-programmable flexibility enhances the usefulness of this device for different types of state machine implementations. The possibility exists to create both the Mealy and Moore type of design in the same device.

Programmable Output Polarity

Each output has a user-programmable output polarity fuse which, when blown, indicates that the output will be active HIGH, and when intact, active LOW. The obvious benefit of this enhancement is the increased flexibility of design. With the choice of output polarity, there is no need to DeMorganize equations to fit the device, allowing for more efficient designs both in terms of the amount of time spent in design as well as effective utilization of the device.

For further enhancement of the increased logic power of the AmPAL23S8, each output has a PT to control Output Enable (OE) with programmable polarity.

PRESET/RESET

To improve functionality at the system level, the AmPAL23S8 has additional RESET and PRESET PTs. One PT controls Output Register and BSR PRESET, and one PT controls the RESET for these registers. When the Synchronous PRESET PT is asserted (HIGH), all registers are loaded with a HIGH on the next LOW-to-HIGH clock transition. When the Asynchronous RESET PT is asserted, all registers are immediately loaded with a LOW, independent of the clock. These functions are particularly useful for applications such as system power-up and RESET.

PRELOAD

In order to simplify testing, the AmPAL23S8 is designed with PRELOAD circuitry that provides an easy method for testing logical functionality. PRELOAD allows any arbitrary "present state" values to be loaded into the OLMs, BSRs and Output Registers of this device. OLM Registers and BSRs are PRELOADed in separate cycles, allowing them to be PRELOADed with different values. Logic verification sequences can be significantly shortened, and all possible state sequences tested, reducing test time and development costs, and guaranteeing proper functionality in system.

A typical functional test sequence would be to verify all possible state transitions for the device being tested. To verify these transitions requires the ability to set the state registers to an arbitrary "present state" value and to set the device inputs to any arbitrary "present input" value. Once this is done, the state machine is then clocked into a new state, or "next state," which can be checked to validate the transition from the "present state." In this way, any state transition can be checked.

It is obvious that to attempt the debugging of a design using BSRs without the benefit of PRELOAD capability would be quite difficult. The combination of this feature and the BSRs

being observable is virtually indispensible for efficient and trouble-free state machine design.

Observability

This extra ease of debugging the design comes from the use of the Observability (OBS) PT. When the OBS PT is selected, it disables six of the Output Registers and Macrocell buffers, and enables the BSR buffers onto the output pins associated with them, pins 13 through 18. When the OBS PT is not selected, the Output Registers and Macrocell buffers are enabled and the BSR buffers are disabled. When all the fuses for this PT are intact, (i.e., OBS is not selected), the data from the BSRs will not be visible on the output pins, and the Output Registers and OLMs will be enabled.

Processing and Fuse Technology

The AmPAL23S8 is manufactured using Advanced Micro Devices' IMOX oxide isolation process. This advanced pro-cess permits an increase in density and a decrease in internal capacitance resulting in the fastest possible programmable logic devices.

The AmPAL23S8 is fabricated with AMD's fast programming, highly reliable Platinum-Silicide fuse technology. Utilizing an easily implemented programming algorithm, these products can be rapidly programmed to any customized pattern. Extra test words are preprogrammed during manufacturing to en-sure extremely high field programming yields (> 98%), and provide extra test paths to achieve excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large, noncon-ductive gaps that ensure very stable, long term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers high reliability for fusible link pro-grammable logic.
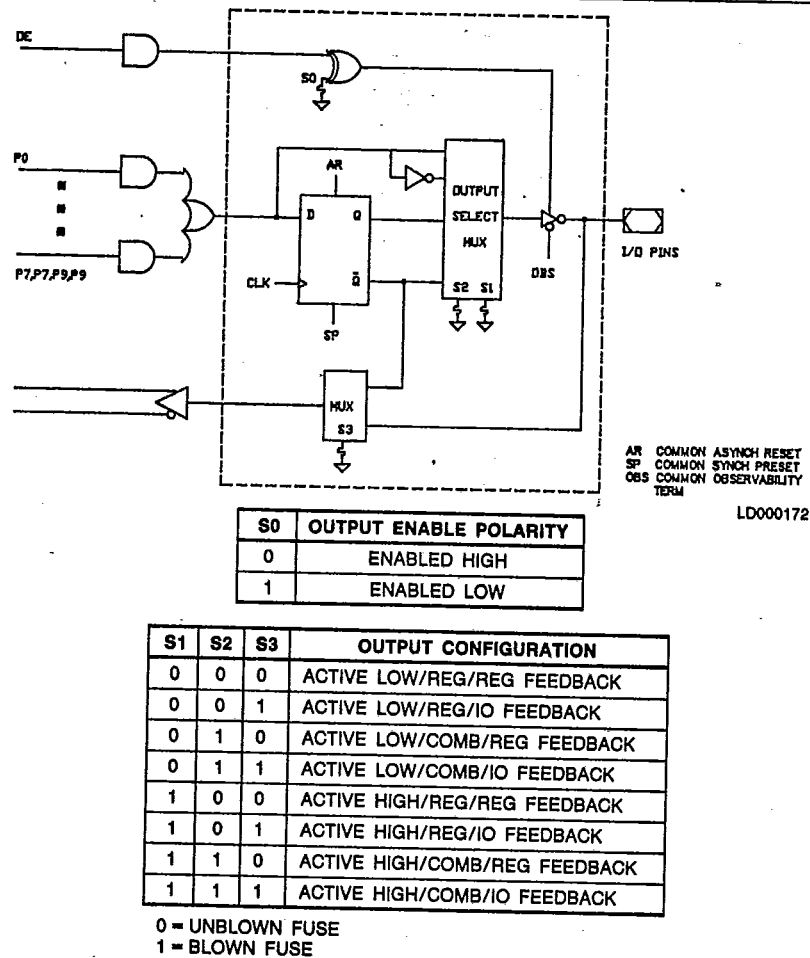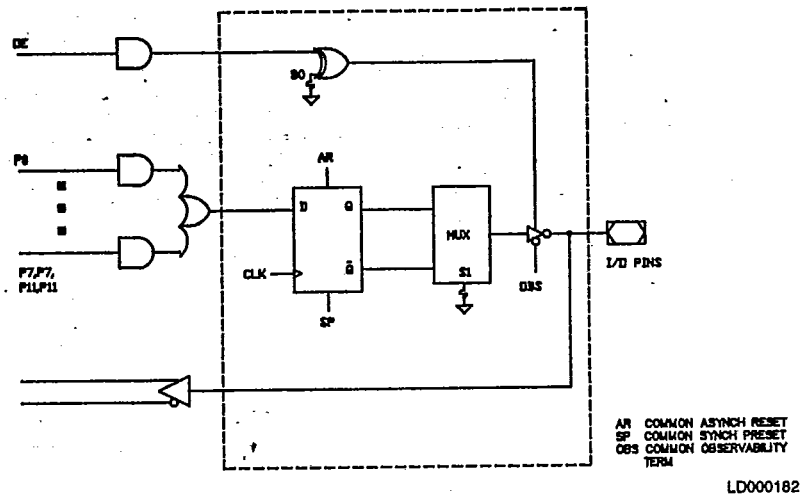

AR   COMMON ASYNCH RESET
SP   COMMON SYNCH PRESET
OBS COMMON OBSERVABILITY
     TERM

LD000172

S0	OUTPUT ENABLE POLARITY
0	ENABLED HIGH
1	ENABLED LOW

S1	S2	S3	OUTPUT CONFIGURATION
0	0	0	ACTIVE LOW/REG/REG FEEDBACK
0	0	1	ACTIVE LOW/REG/IO FEEDBACK
0	1	0	ACTIVE LOW/COMB/REG FEEDBACK
0	1	1	ACTIVE LOW/COMB/IO FEEDBACK
1	0	0	ACTIVE HIGH/REG/REG FEEDBACK
1	0	1	ACTIVE HIGH/REG/IO FEEDBACK
1	1	0	ACTIVE HIGH/COMB/REG FEEDBACK
1	1	1	ACTIVE HIGH/COMB/IO FEEDBACK

0 = UNBLOWN FUSE
1 = BLOWN FUSE

Figure 1. Output Logic Macrocell (OLM)

LD000182

S0	OUTPUT ENABLE POLARITY
0	ENABLED HIGH
1	ENABLED LOW

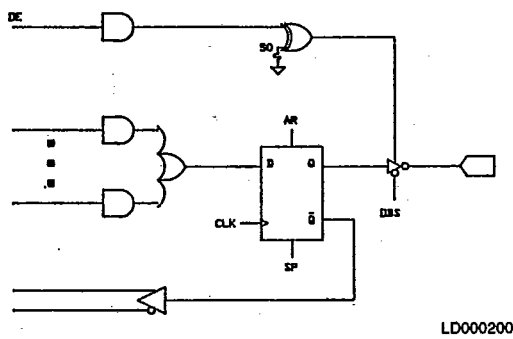| S1	OUTPUT CONFIGURATION
0	ACTIVE LOW
1	ACTIVE HIGH

0 = UNBLOWN FUSE
1 = BLOWN FUSE

Figure 2. Output Register With Polarity
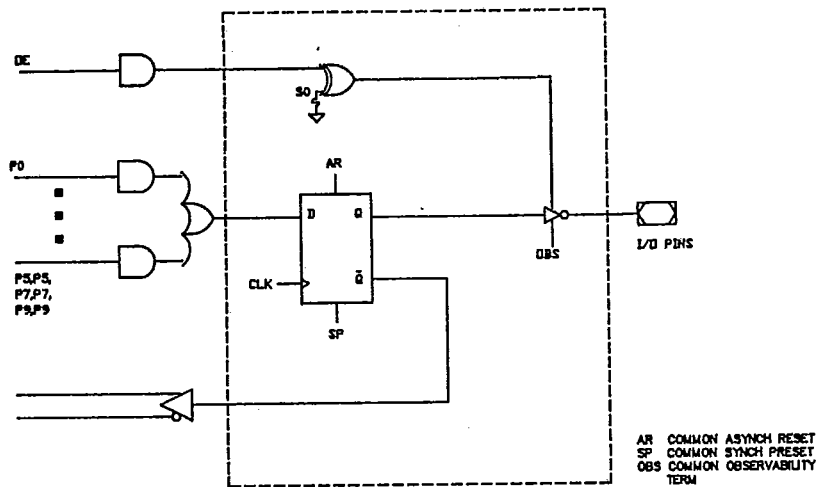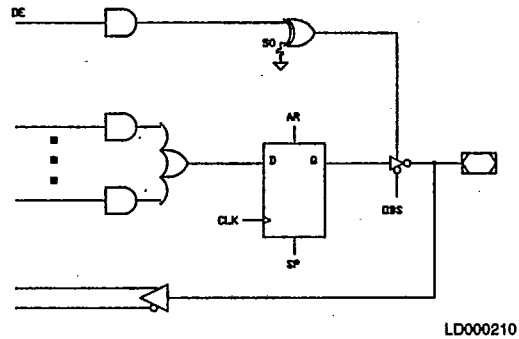

LD000192

Figure 3. Buried State Register (BSR)

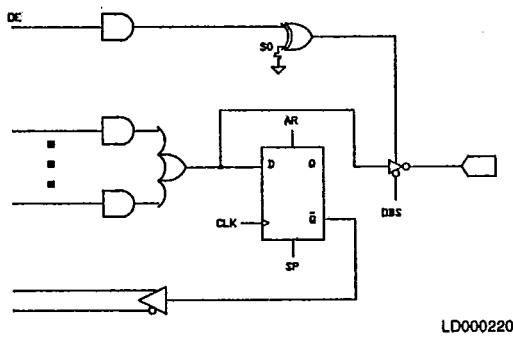## Figure 4. Possible Configurations of the Output Logic Macrocells (OLMs)

LD000200

```
OUTPUT
  ACTIVE LOW      S1 = 0
  REGISTERED      S2 = 0
FEEDBACK
  REGISTERED      S3 = 0
```
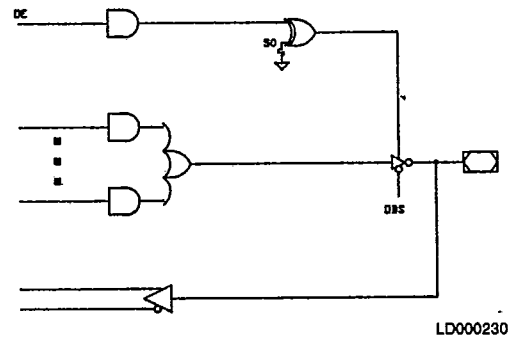
Figure 4-1.

LD000210

```
OUTPUT
  ACTIVE LOW      S1 = 0
  REGISTERED      S2 = 0
FEEDBACK
  I/O PIN         S3 = 1
```

Figure 4-2.

LD000220

```
OUTPUT
  ACTIVE LOW      S1 = 0
  COMBINATORIAL   S2 = 1
FEEDBACK
  REGISTERED      S3 = 0
```

Figure 4-3.

LD000230
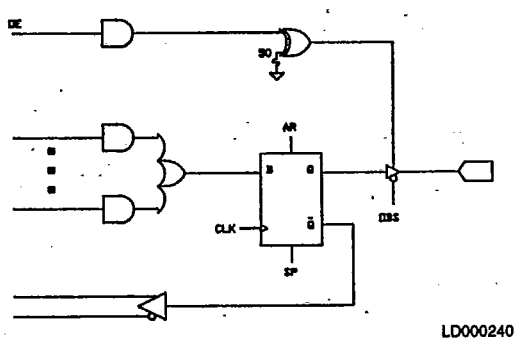
```
OUTPUT
  ACTIVE LOW      S1 = 0
  COMBINATORIAL   S2 = 1
FEEDBACK
  I/O PIN         S3 = 1
```
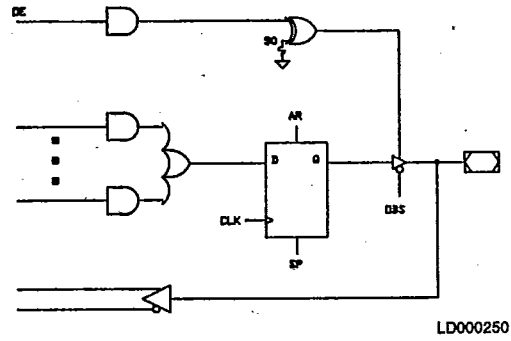
Figure 4-4.

5

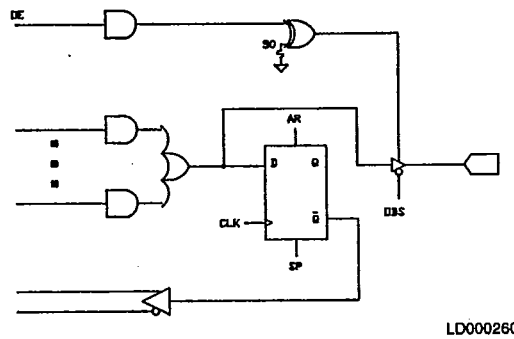**Figure 4. Possible Configurations of the Output Logic Macrocells (OLMs) (Cont'd.)**

LD000240

OUTPUT
  ACTIVE HIGH   S1 = 1
  REGISTERED   S2 = 0
FEEDBACK
  REGISTERED   S3 = 0

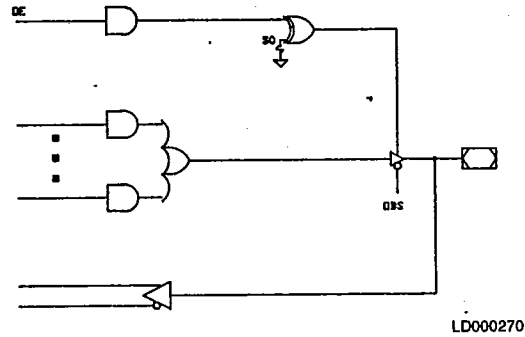**Figure 4-5.**

LD000250

OUTPUT
  ACTIVE HIGH   S1 = 1
  REGISTERED   S2 = 0
FEEDBACK
  I/O PIN   S3 = 1

Figure 4-6.

LD000260

OUTPUT
  ACTIVE HIGH   S1 = 1
  COMBINATORIAL S2 = 1
FEEDBACK
  REGISTERED   S3 = 0

Figure 4-7.

LD000270

OUTPUT
  ACTIVE HIGH   S1 = 1
  COMBINATORIAL S2 = 1
FEEDBACK
  I/O PIN   S3 = 1
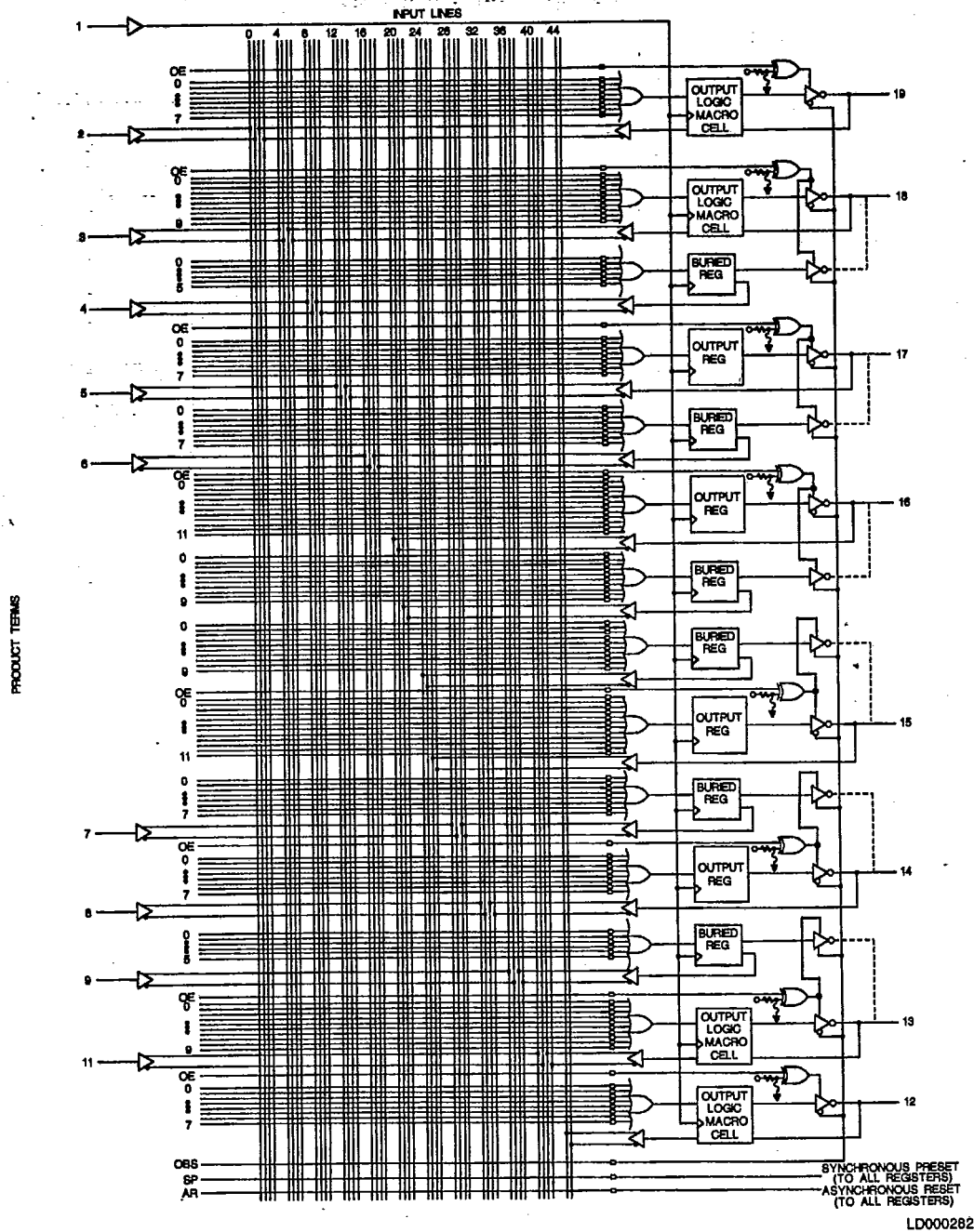
Figure 4-8.

Figure 4. Logic Diagram — AmPAL23S8

Input/Output Diagrams

Input

INPUT

PROGRAM/VERIFY
CIRCUITRY

IC000804

Output

FROM
SENSE
AMP

OUTPUT
DISABLE

OUTPUT

INPUT
TO ARRAY

PRELOAD

PROGRAMMING
CURRENT PATH

IC000805
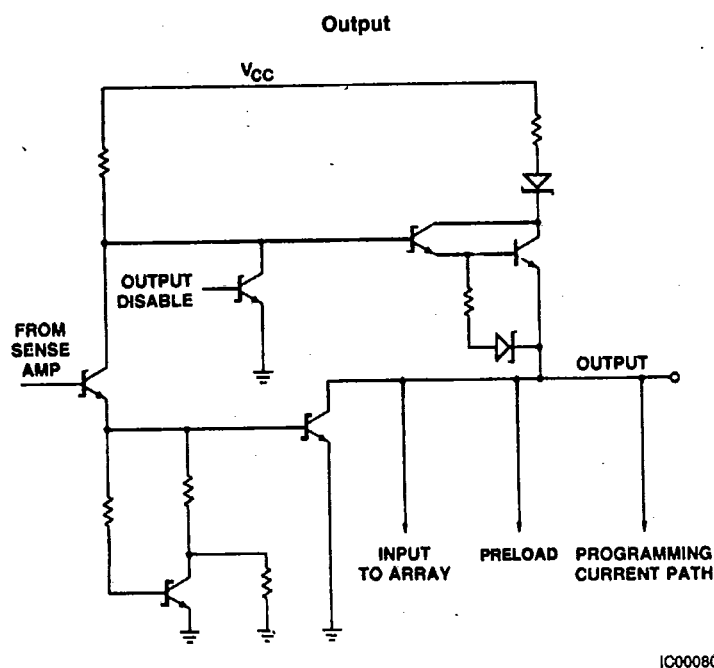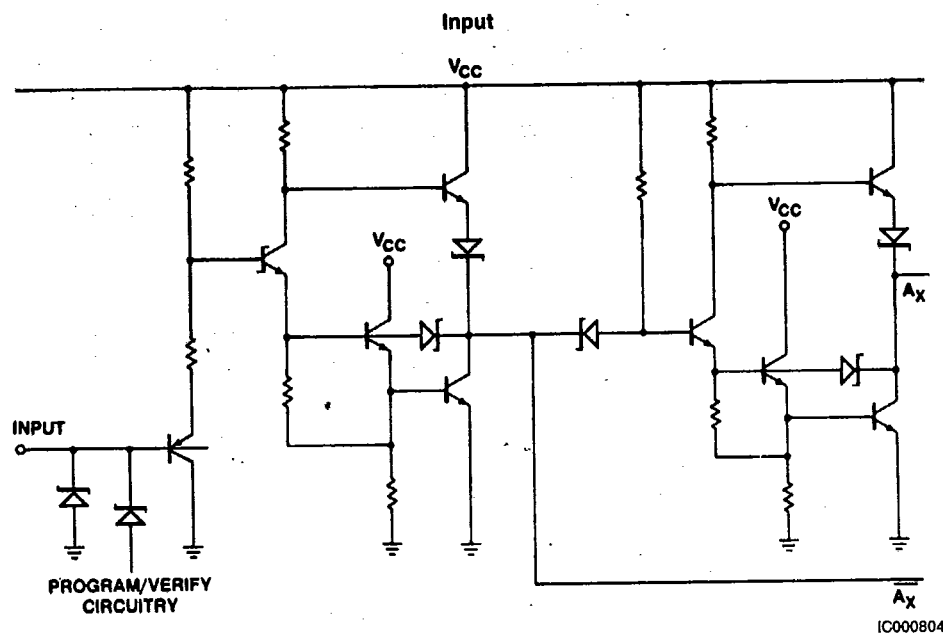
Absolute Maximum Ratings

Storage Temperature .... −65 to +150°C
Ambient Temperature with
  Power Applied .... +125°C
Supply Voltage to Ground Potential
  Continuous (Pin 20 to Pin 10) .... −0.5 to +7.0 V
DC Voltage Applied to Outputs
  (except during programming) .... −0.5 to +V_{CC} Max.
DC Voltage Applied to Outputs
  During Programming .... 16 V
Output Current Into Outputs
  During Programming
  (Maximum duration of 1 second) .... 200 mA
DC Input Voltage .... −0.5 to +5.5 V
DC Input Current .... −30 to +5.0 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Operating Ranges

Commercial (C) Devices
  Temperature (T_A) Operating Free Air .... 0 to +75°C
  Supply Voltage (V_{CC}) .... +4.75 to +5.25 V
Extended Commercial (E) Devices
  Temperature (T_A) .... −55°C Min.
  Temperature (T_C) Operating Case .... +125°C Max.
  Supply Voltage (V_{CC}) .... +4.50 to +5.50 V
Military (M) Devices
  Temperature (T_A) .... −55°C Min.
  Temperature (T_C) .... +125°C Max.
  Supply Voltage (V_{CC}) .... +4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC Characteristics over operating range unless otherwise specified; included in Group A, Subgroup 1, 2, 3 tests unless otherwise noted

Parameter Symbol	Parameter Description	Test Conditions			Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -3.2$ mA	C Devices	2.4	3.5		Volts
			$I_{OH} = -2$ mA	E/M Devices				
V_{OL}	Output LOW Voltage		$I_{OL} = 16$ mA	C Devices			0.50	Volts
			$I_{OL} = 12$ mA	E/M Devices				
V_{IH} (Note 2)	Input HIGH level	Guaranteed Input Logical HIGH Voltage for All Inputs			2.0			Volts
V_{IL} (Note 2)	Input LOW level	Guaranteed Input Logical LOW Voltage for All Inputs					0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.40 V				−10	−250	µA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V					25	µA
I_I	Input HIGH Current	V_{CC} = Max., V_{IN} = 5.5 V					1.0	mA
I_{SC}	Output Short-Circuit Current	V_{CC} = Max., V_{OUT} = 0.5 V (Note 3)			−30	−45	−90	mA
I_{CC}	Power Supply Current	All Inputs = GND, V_{CC} = Max.		COMM MIL			210 / 215	mA / mA
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA				−0.9	−1.2	Volts
I_{OZH} I_{OZL}	Output Leakage Current (Note 4)	V_{CC} = Max., $V_{IN} = V_{IL}$ or V_{IH}	V_0 = 2.7 V				100	µA
			V_0 = 0.4 V				100	

Notes:
1. Typical limits are at V_{CC} = 5.0 V and T_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.
4. I/O pin leakage is the worst case of I_{OZX} or I_{IX} (where X = H or L).

Capacitance

| Parameter Symbol	Parameter Description	Test Conditions		Typ.	Units
C_{IN}	Input Capacitance	V_{IN} = 2.0 V @ f = 1 MHz	Pins 1, 11	10	pF
			Other Pins	6	
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V @ f = 1 MHz		9	

Note: These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
▬▬▬	MUST BE STEADY	WILL BE STEADY
▨▨▨	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
▨▨▨	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
▨▨▨	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
▷◁	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE ▸ "OFF" STATE

KS000010

Switching Test Circuit

AC TEST LOAD

TC001190
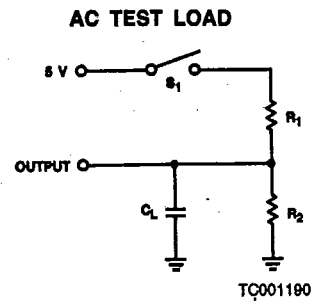
TEST OUTPUT LOADS

| C Devices		E/M Devices	
R_1	R_2	R_1	R_2
300	390	390	750

Switching Characteristics

over operating range unless otherwise specified; included in Group A, Subgroup 7, 8, 9, 10, 11 tests unless otherwise noted

No.	Parameter Symbol	Parameter Description	Test Conditions	Typ (Note 1)	C Devices −20 Min.	C Devices −20 Max.	C Devices −25 Min.	C Devices −25 Max.	E/M Devices −27 Min.	E/M Devices −27 Max.	E/M Devices −30 Min.	E/M Devices −30 Max.	Units
1	t_{PD}	Input or Feedback to Non-Registered Output				20		25		27		30	ns
2	t_{EA}	Input to Output Enable				25		28		30		33	ns
3	t_{ER}	Input to Output Disable				25		28		30		33	ns
4	t_{CO1}	Clock to Output				13		15		18		20	ns
5	t_{CO2}	Reg. Feedback through Array to Combinatorial Output, Relative to External Clock				28		35		40		45	ns
6	t_S	Input or Feedback Setup Time	C Devices $R_1 = 300$ $R_2 = 390$		17		20		22		25		ns
7	t_H	Hold Time			0		0		0		0		ns
8	t_{P1}	Clock Period ($t_S + t_{CO1}$)			30		35		40		45		ns
9	t_{P2}	Minimum Setup Time (Reg. Feedback to Reg. Input Internal Path)			25		30		35		40		ns
10	t_W	Clock Width			12		15		17		20		ns
11	f_{1MAX}	Maximum Frequency ($1/t_{P1}$)				33		28.5		25		22.5	MHz
12	f_{2MAX}	Maximum Frequency ($1/t_{P2}$)	E/M Devices $R_1 = 390$ $R_2 = 750$			40		33		28.5		25	MHz
13	t_{AW}	Asynchronous Reset Width			20		25		27		30		ns
14	t_{AR}	Asynchronous Reset Recovery Time			20		25		27		30		ns
15	t_{AP}	Asynchronous Reset to Registered Output Reset				25		30		32		35	ns

Notes: 1. Typical limits are at $V_{CC} = 5.0$ V and $T_A = 25°C$.
2. t_{PD} is tested with switch S_1 closed and $C_L = 50$ pF.
3. For three-state outputs, output enable times are tested with $C_L = 50$ pF to the 1.5 V level; S_1 is open for high-impedance to HIGH tests and closed for high-impedance to LOW tests. Output disable times are tested with $C_L = 5$ pF. HIGH to high-impedance tests are made to an output voltage of $V_{OH} - 0.5$ V with S_1 open; LOW to high-impedance tests are made to the $V_{OL} + 0.5$ V level with S_1 closed.

Switching Waveform
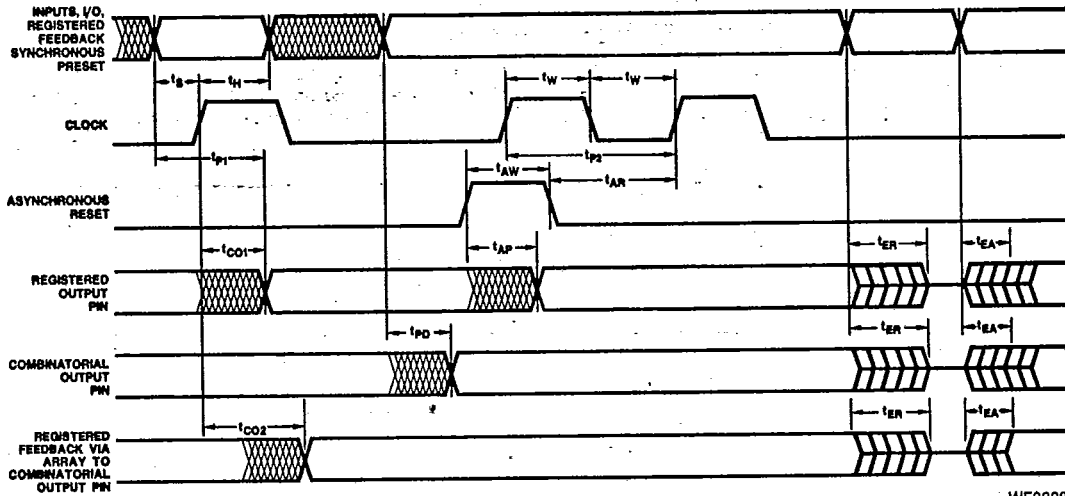
WF022285

PRELOAD of Output/Macrocell Registers or Buried State Registers

All AmPAL23S8 registers are provided with circuitry to allow loading each register synchronously with a HIGH or LOW. Output/macrocell registers and buried state registers are PRELOADed in separate cycles allowing output/macrocell registers and buried state registers to be PRELOADed with different values. PRELOAD will simplify testing since any state can be loaded into the registers to control testing sequences. The pin levels and timing necessary to perform the PRELOAD function are detailed below.
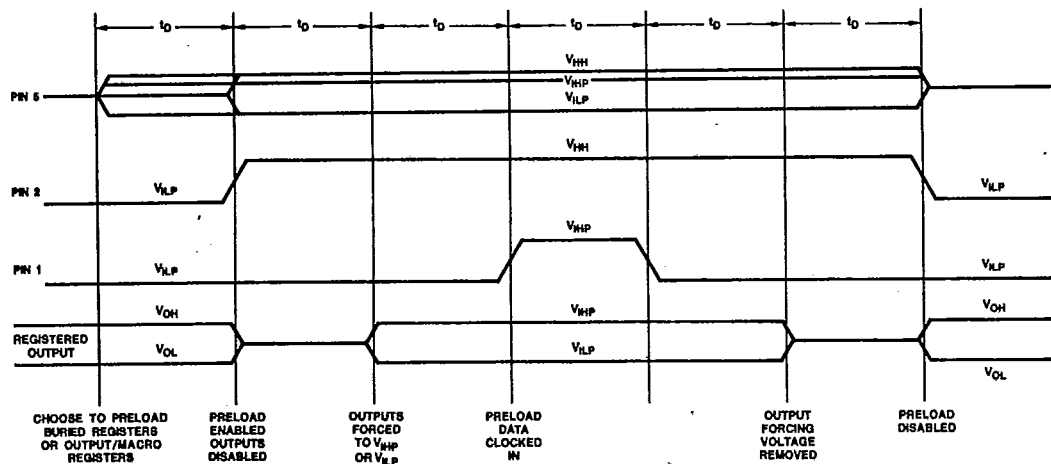
WF022292

Par.	Min.	Max.
V_{HH}	10	12
V_{ILP}	0	0.5
V_{IHP}	2.4	5.5

Register Selection	Pin 5
Buried	V_{HH}
Output/Macro	$\leq V_{IHP}$

Level Forced on Register Output Pin During PRELOAD Cycle	Register State After Cycle
V_{IHP}	HIGH
V_{ILP}	LOW

Power-Up Reset

The registered devices in the AMD PAL Family have been designed with the capability to reset during system power-up. Following power-up, all registers will be reset to LOW. The output state will depend on the polarity of the output buffer. This feature provides an extra flexibility to the designer and is especially valuable in simplifying state-machine initialization. A timing diagram and parameter table follow. Due to the asynchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.
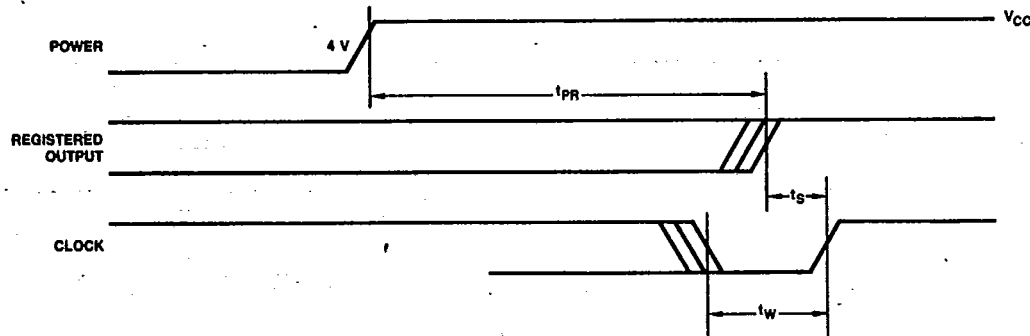
WF022300

Parameter Symbol	Parameter Description	Min.	Typ.	Max.	Units
t_{PR}	Power-Up Reset Time		600	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics			
t_W	Clock Width				

Programmers/Development Systems

(refer to Programmer Reference Guide, page 3-81)

Monolithic Memories