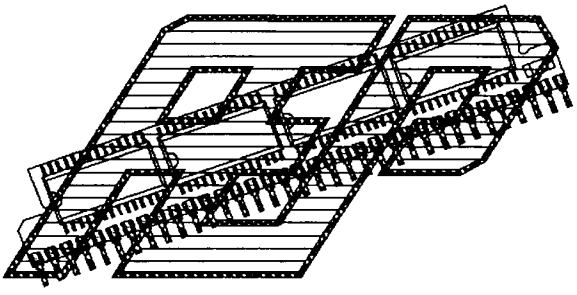


- *>> 262,144 x 8 Organization*
- *>> Double sided to maximize bit density*
- *>> Low 0.66" stand-off height suited to 0.8" card spacing*
- *>> Completely Static operation*
- *>> TTL compatible*
- *>> Low power, battery back-up operation capability*
- *>> Uses single +5V power supply*
- *>> Super Low Power version available*

256 KILOBYTE STATIC RAM MODULE

DESCRIPTION:

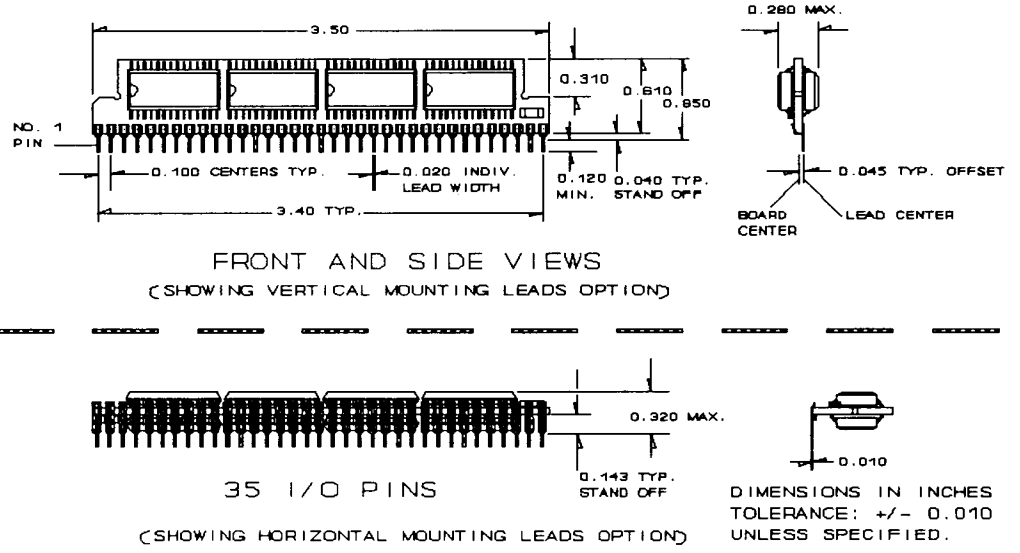
The AEPSX256K8 is a high density 256 Kilo-word by 8 bit static random access memory module in a 35 pin single-inline-package format. Physically it consists of an FR4 PC material substrate mounted with eight 32K x 8 SOP (small outline package) ICs, two 0.1 microfarad decoupling capacitors, and 35 edge-clip I/O pins.

The module can use any of the 32K x 8 SRAMs made by any of a large number of manufacturers in both Mix-MOS and CMOS technologies. A wide range of access speeds are available. Performance specifications and electrical characteristics are determined by the IC devices used. These items can vary according to the type and manufacturer of the components. The necessary information is obtained from the IC vendors data sheets, which are included here, or from data books.

Mechanical dimensions are 0.66 in. high by 3.48 in. long by 0.28 in. wide. The module is available with either vertical or 90 degree (horizontal) lead pins. The latter allows the module to be mounted on its side which gives a low 0.320 stand-off height.

Nearly 250 interconnections are accomplished within the substrate. Using AEP high density memory modules saves board space, reduces line lengths, and simplifies the layout design process. This module is also available in 64K x 8 organization.

SPECIFICATION DRAWING
256Kx8 SRAM



256K x 8 STATIC RAM MODULE

SIP PIN-OUT CONFIGURATION

1	A_0
2	A_1
3	A_{14}
4	A_2
5	A_3
6	A_4
7	CE_2*
8	A_5
9	I/O_1
10	I/O_2
11	CE_1*
12	A_6
13	A_7
14	A_8
15	CE_4*
16	A_9
17	GND
18	CE_3*
19	VCC
20	A_{13}
21	OE*
22	CE_6*
23	I/O_3
24	I/O_4
25	I/O_5
26	CE_5*
27	WE*
28	A_{10}
29	A_{11}
30	CE_8*
31	I/O_6
32	I/O_7
33	CE_7*
34	A_{12}
35	I/O_8

* ACTIVE WHEN LOW

64K x 8 version notes:
pin 3 is a no connect
pin 20 is a CHIP SELECT

64K x 9 version notes:
pin 3 is I/O 9
pin 20 is a CHIP SELECT

FUNCTIONAL DIAGRAM