

REGISTRATION PENDING

Currently Available as FRF9150(D, R, H)

March 1996

 Radiation Hardened
 P-Channel Power MOSFETs

Features

- 23A, -100V, $r_{DS(ON)} = 0.140\Omega$
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
 - Meets Pre-RAD Specifications to 100K RAD (SI)
 - Defined End Point Specs at 300K RAD (SI) and 1000K RAD (SI)
 - Performance Permits Limited Use to 3000K RAD (SI)
- Gamma Dot
 - Survives 3E9 RAD (SI)/s at 80% BV_{DSS} Typically
 - Survives 2E12 Typically If Current Limited to IDM
- Photo Current
 - 7.0nA Per-RAD (SI)/s Typically
- Neutron
 - Pre-RAD Specifications for 3E13 Neutrons/cm²
 - Usable to 3E14 Neutrons/cm²
- Single Event
 - Typically Survives 1E5 ions/cm² Having an LET $\leq 35\text{MeV/mg/cm}^2$ and a Range $\geq 30\mu\text{m}$ at 80% BV_{DSS}

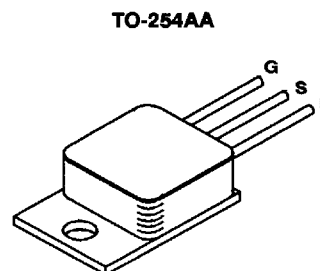
Description

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25m Ω . Total dose hardness is offered at 100K RAD (SI) and 1000K RAD (SI) with neutron hardness ranging from 1E13n/cm² for 500V product to 1E14n/cm² for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

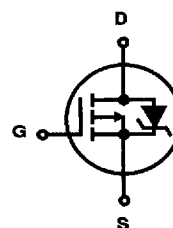
This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n^o) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Package



Symbol



Absolute Maximum Ratings $T_C = +25^\circ\text{C}$, Unless Otherwise Specified

	2N7323D, R, H	UNITS
Drain-Source Voltage..... V_{DS}	-100	V
Drain-Gate Voltage ($R_{GS} = 20k\Omega$)..... V_{DGR}	-100	V
Continuous Drain Current		
$T_C = +25^\circ\text{C}$ I_D	23	A
$T_C = +100^\circ\text{C}$ I_D	15	A
Pulsed Drain Current..... I_{DM}	69	A
Gate-Source Voltage..... V_{GS}	± 20	V
Maximum Power Dissipation		
$T_C = +25^\circ\text{C}$ PT	125	W
$T_C = +100^\circ\text{C}$ PT	50	W
Derated Above $+25^\circ\text{C}$	1.00	W/ $^\circ\text{C}$
Inductive Current, Clamped, $L = 100\mu\text{H}$, (See Test Figure)..... I_{LM}	69	A
Continuous Source Current (Body Diode)..... I_S	23	A
Pulsed Source Current (Body Diode)..... I_{SM}	69	A
Operating And Storage Temperature..... T_{JC}, T_{STG}	-55 to +150	$^\circ\text{C}$
Lead Temperature (During Soldering)		
Distance > 0.063 in. (1.6mm) From Case, 10s Max. T_L	300	$^\circ\text{C}$

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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 File Number **3243.1**

Specifications 2N7323D, 2N7323R, 2N7323H - Registration Pending

Pre-Radiation Electrical Specifications $T_C = +25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Drain-Source Breakdown Volts	BV_{DSS}	$V_{GS} = 0, I_D = 1\text{mA}$	-100	-	V
Gate-Threshold Volts	$V_{GS(TH)}$	$V_{DS} = V_{GS}, I_D = 1\text{mA}$	-2.0	-4.0	V
Gate-Body Leakage Forward	I_{GSSF}	$V_{GS} = -20\text{V}$	-	100	nA
Gate-Body Leakage Reverse	I_{GSSR}	$V_{GS} = +20\text{V}$	-	100	nA
Zero-Gate Voltage Drain Current	I_{DSS1}	$V_{DS} = -100\text{V}, V_{GS} = 0$	-	1	mA
	I_{DSS2}	$V_{DS} = -80\text{V}, V_{GS} = 0$	-	0.025	
	I_{DSS3}	$V_{DS} = -80\text{V}, V_{GS} = 0, T_C = +125^\circ\text{C}$	-	0.25	
Rated Avalanche Current	I_{AR}	Time = 20 μs	-	69	A
Drain-Source On-State Volts	$V_{DS(ON)}$	$V_{GS} = -10\text{V}, I_D = 23\text{A}$	-	-3.38	V
Drain-Source On Resistance	$r_{DS(ON)}$	$V_{GS} = -10\text{V}, I_D = 15\text{A}$	-	0.140	Ω
Turn-On Delay Time	$t_{D(ON)}$	$V_{DD} = -50\text{V}, I_D = 23\text{A}$ Pulse Width = 3 μs Period = 300 μs , $R_G = 25\Omega$ $0 \leq V_{GS} \leq 10$ (See Test Circuit)	-	170	ns
Rise Time	t_R		-	620	
Turn-Off Delay Time	$t_{D(OFF)}$		-	600	
Fall Time	t_F		-	242	
Gate-Charge Threshold	$Q_{G(TH)}$	$V_{DD} = -50\text{V}, I_D = 23\text{A}$ $I_{GS1} = I_{GS2}$ $0 \leq V_{GS} \leq 20$	4	16	nc
Gate-Charge On State	$Q_{G(ON)}$		60	240	
Gate-Charge Total	Q_{GM}		126	504	
Plateau Voltage	V_{GP}		3	14	V
Gate-Charge Source	Q_{GS}		17	68	nc
Gate-Charge Drain	Q_{GD}		21	86	
Diode Forward Voltage	V_{SD}	$I_D = 23\text{A}, V_{GD} = 0$	-0.6	-1.8	V
Reverse Recovery Time	t_T	$I = 23\text{A}; di/dt = 100\text{A}/\mu\text{s}$	-	700	ns
Junction-To-Case	$R_{\theta JC}$		-	1.0	$^\circ\text{C}/\text{W}$
Junction-To-Ambient	$R_{\theta JA}$	Free Air Operation	-	48	

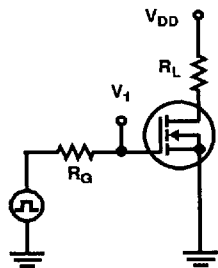


FIGURE 1. SWITCHING TIME TESTING

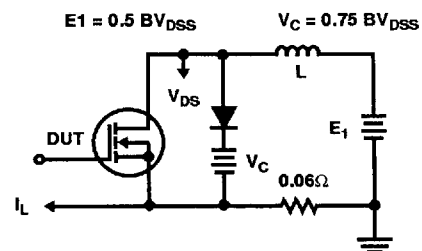


FIGURE 2. CLAMPED INDUCTIVE SWITCHING, ILM

Specifications 2N7323D, 2N7323R, 2N7323H - Registration Pending

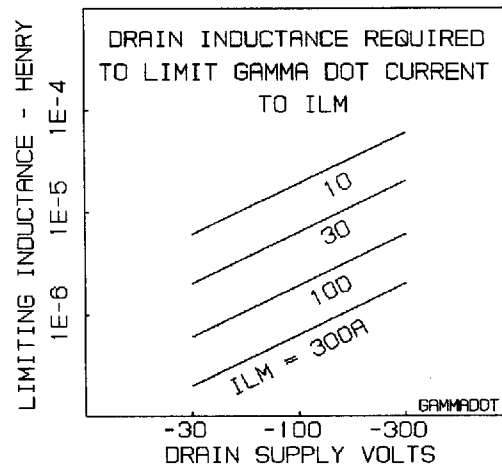
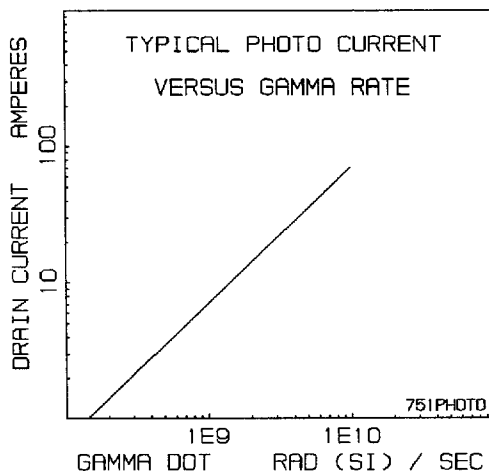
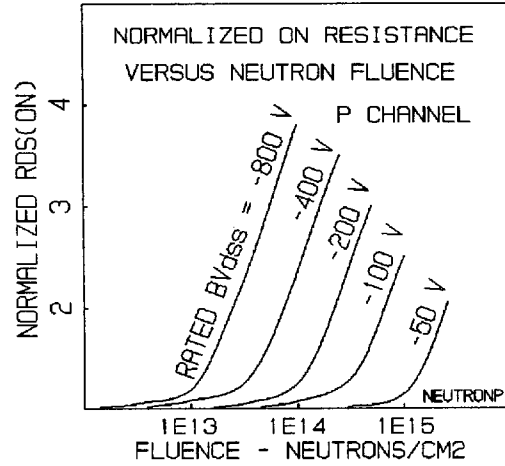
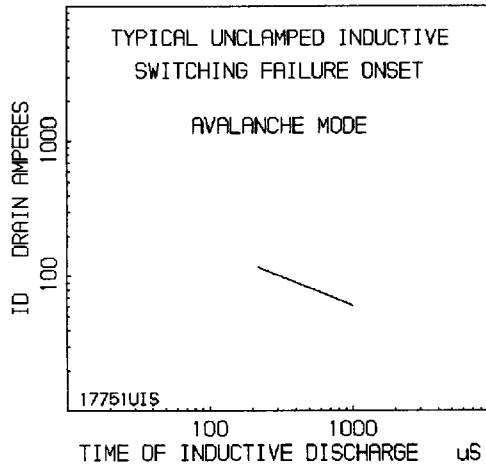
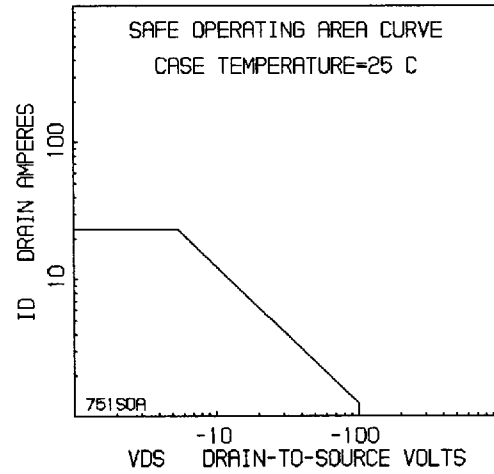
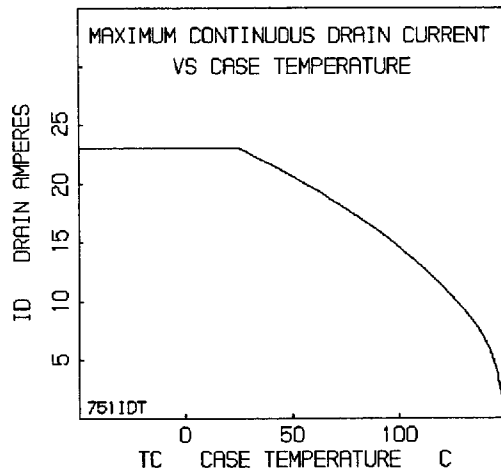
Post-Radiation Electrical Specifications $T_C = +25^\circ\text{C}$, Unless Otherwise Specified

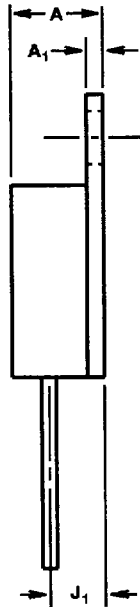
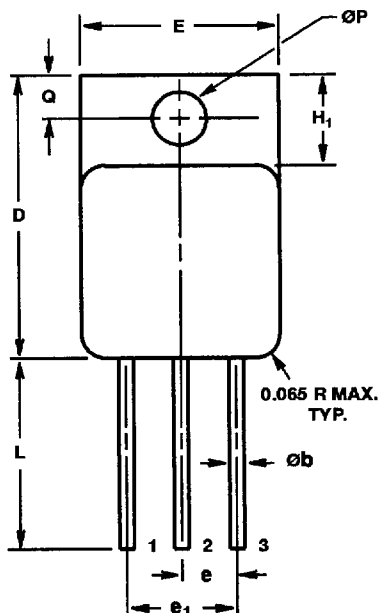
PARAMETER		SYMBOL	TYPE	TEST CONDITIONS	LIMITS		UNITS
					MIN	MAX	
Drain-Source Breakdown Volts	(Notes 4, 6)	BV_{DSS}	2N7323D, R	$V_{GS} = 0, I_D = 1\text{mA}$	-100	-	V
	(Notes 5, 6)	BV_{DSS}	2N7323H	$V_{GS} = 0, I_D = 1\text{mA}$	-95	-	V
Gate-Source Threshold Volts	(Notes 4, 6)	$V_{GS(TH)}$	2N7323D, R	$V_{GS} = V_{DS}, I_D = 1\text{mA}$	-2.0	-4.0	V
	(Notes 3, 5, 6)	$V_{GS(TH)}$	2N7323H	$V_{GS} = V_{DS}, I_D = 1\text{mA}$	-2.0	-6.0	V
Gate-Body Leakage Forward	(Notes 4, 6)	I_{GSSF}	2N7323D, R	$V_{GS} = -20\text{V}, V_{DS} = 0$	-	100	nA
	(Notes 5, 6)	I_{GSSF}	2N7323H	$V_{GS} = -20\text{V}, V_{DS} = 0$	-	200	nA
Gate-Body Leakage Reverse	(Notes 2, 4, 6)	I_{GSSR}	2N7323D, R	$V_{GS} = 20\text{V}, V_{DS} = 0$	-	100	nA
	(Notes 2, 5, 6)	I_{GSSR}	2N7323H	$V_{GS} = 20\text{V}, V_{DS} = 0$	-	200	nA
Zero-Gate Voltage Drain Current	(Notes 4, 6)	I_{DSS}	2N7323D, R	$V_{GS} = 0, V_{DS} = -80\text{V}$	-	25	μA
	(Notes 5, 6)	I_{DSS}	2N7323H	$V_{GS} = 0, V_{DS} = -80\text{V}$	-	100	μA
Drain-Source On-State Volts	(Notes 1, 4, 6)	$V_{DS(ON)}$	2N7323D, R	$V_{GS} = -10\text{V}, I_D = 23\text{A}$	-	-3.38	V
	(Notes 1, 5, 6)	$V_{DS(ON)}$	2N7323H	$V_{GS} = -16\text{V}, I_D = 23\text{A}$	-	-5.07	V
Drain-Source On Resistance	(Notes 1, 4, 6)	$r_{DS(ON)}$	2N7323D, R	$V_{GS} = -10\text{V}, I_D = 15\text{A}$	-	0.140	Ω
	(Notes 1, 5, 6)	$r_{DS(ON)}$	2N7323H	$V_{GS} = -14\text{V}, I_D = 15\text{A}$	-	0.210	Ω

NOTES:

1. Pulse test, 300 μs (Max)
2. Absolute value
3. Gamma = 300K RAD (Si)
4. Gamma = 10K RAD (Si) for "D", 100K RAD (Si) for "R". Neutron = 3E13
5. Gamma = 1000K RAD (Si). Neutron = 3E13
6. In situ Gamma bias must be sampled for both $V_{GS} = -10\text{V}, V_{DS} = 0\text{V}$ and $V_{GS} = 0\text{V}, V_{DS} = 80\% BV_{DSS}$
7. Gamma data taken 1/18/91 on TA 17751 devices by GE ASTRO SPACE; EMC/SURVIVABILITY LABORATORY; KING OF PRUSSIA, PA 19401
8. Single event drain burnout testing by Titus, J.L., et al of NWSC, Crane, IN at Brookhaven Nat. Lab. Dec 11-14, 1989
9. Neutron derivation, HARRIS Application note AN-8831, Oct. 1988

Typical Performance Characteristics



Hermetic Metal Packages**TO-254AA****3 LEAD JEDEC TO-254AA HERMETIC METAL PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.249	0.260	6.33	6.60	-
A ₁	0.040	0.050	1.02	1.27	-
Øb	0.035	0.045	0.89	1.14	2, 3
D	0.790	0.800	20.07	20.32	-
E	0.535	0.545	13.59	13.84	-
e	0.150 TYP		3.81 TYP		4
e ₁	0.300 BSC		7.62 BSC		4
H ₁	0.245	0.265	6.23	6.73	-
J ₁	0.140	0.160	3.56	4.06	4
L	0.520	0.560	13.21	14.22	-
ØP	0.139	0.149	3.54	3.78	-
Q	0.110	0.130	2.80	3.30	-

NOTES:

1. These dimensions are within allowable dimensions of Rev. A of JEDEC outline TO-254AA dated 11-86.
2. Add typically 0.002 inches (0.05mm) for solder coating.
3. Lead dimension (without solder).
4. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
5. Die to base BeO isolated, terminals to case ceramic isolated.
6. Controlling dimension: Inch.
7. Revision 1 dated 1-93.

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