27LV256

256K (32K x 8) Low-Voltage CMOS EPROM

FEATURES

- Wide voltage range 3.0V to 5.5V
- High speed performance
  - 200 ns access time available at 3.0V
- CMOS Technology for low power consumption
  - 8 mA Active current at 3.0V
  - 20 mA Active current at 5.5V
  - 100 µA Standby current
- Factory programming available
- Auto-insertion-compatible plastic packages
- Auto ID aids automated programming
- Separate chip enable and output enable controls
- High speed “Express” programming algorithm
- Organized 32K x 8: JEDEC standard pinouts
  - 28-pin Dual-in-line package
  - 32-pin PLCC package
  - 28-pin SOIC package
  - Tape and reel
- Data Retention > 200 years
- Available for the following temperature ranges:
  - Commercial: 0˚C to +70˚C
  - Industrial: -40˚C to +85˚C

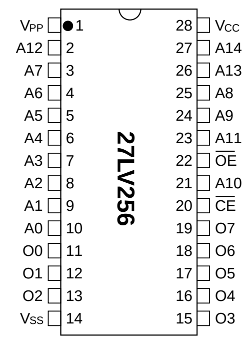
DESCRIPTION

The Microchip Technology Inc. 27LV256 is a low voltage (3.0 volt) CMOS EPROM designed for battery powered applications. The device is organized as a 32K x 8 (32K-Byte) non-volatile memory product. The 27LV256 consumes only 8 mA maximum of active current during a 3.0 volt read operation therefore improving battery performance. This device is designed for very low voltage applications where conventional 5.0 volt only EPROMS can not be used. Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 200 ns at 3.0V. This device allows systems designers the ability to use low voltage non-volatile memory with today’s' low voltage microprocessors and peripherals in battery powered applications.

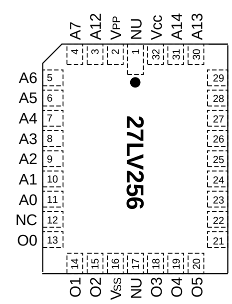
A complete family of packages is offered to provide the most flexibility in applications. For surface mount applications, PLCC or SOIC packaging is available. Tape and reel packaging is also available for PLCC or SOIC packages.

PACKAGE TYPES

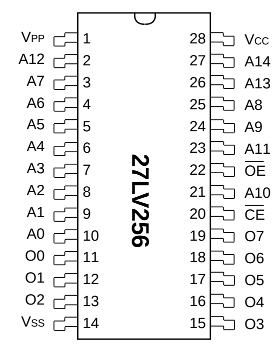
PDIP



PLCC



SOIC



1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC and input voltages w.r.t. VSS .... -0.6V to +7.25V

VPP voltage w.r.t. VSS during programming .... -0.6V to +14V

Voltage on A9 w.r.t. VSS .... -0.6V to +13.5V

Output voltage w.r.t. VSS .... -0.6V to VCC +1.0V

Storage temperature .... -65˚C to +150˚C

Ambient temp. with power applied...... -65˚C to +125˚C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0-A14	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
VPP	Programming Voltage
O0 - O7	Data Output
VCC	+5V or +3V Power Supply
VSS	Ground
NC	No Connection; No Internal Connection
NU	Not Used; No External Connection Is Allowed

TABLE 1-2: READ OPERATION DC CHARACTERISTICS

VCC = +5V ±10% or 3.0V where indicated
Commercial: Tamb = 0˚C to +70˚C
Industrial: Tamb = -40˚C to +85˚C

Parameter	Part*	Status	Symbol	Min.	Max.	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.5	VCC+1 0.8	V V	
Input Leakage	all		ILI	-10	10	µA	VIN = 0 to VCC
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -400 µA IOL = 2.1 mA
Output Leakage	all	—	ILO	-10	10	µA	VOUT = 0V to VCC
Input Capacitance	all	—	CIN	—	6	pF	VIN = 0V; Tamb = 25°C; f = 1 MHz
Output Capacitance	all	—	COUT	—	12	pF	VOUT = 0V; Tamb = 25°C; f = 1 MHz
Power Supply Current, Active	C I	TTL input TTL input	ICC1 ICC2	— —	20 @ 5.0V 8 @ 3.0V 25 @ 5.0V 10 @ 3.0V	mA mA mA mA	VCC = 5.5V; VPP = VCC f = 1 MHz; $\overline{OE}$ = $\overline{CE}$ = VIL; IOUT = 0 mA; VIL = -0.1 to 0.8V; VIH = 2.0 to VCC; Note 1
Power Supply Current, Standby	C I all	TTL input TTL input CMOS input	ICC(s)	—	1 @ 3.0V 2 @ 3.0V 100 @ 3.0V	mA mA µA	 $\overline{CE}$=VCC ± 0.2V

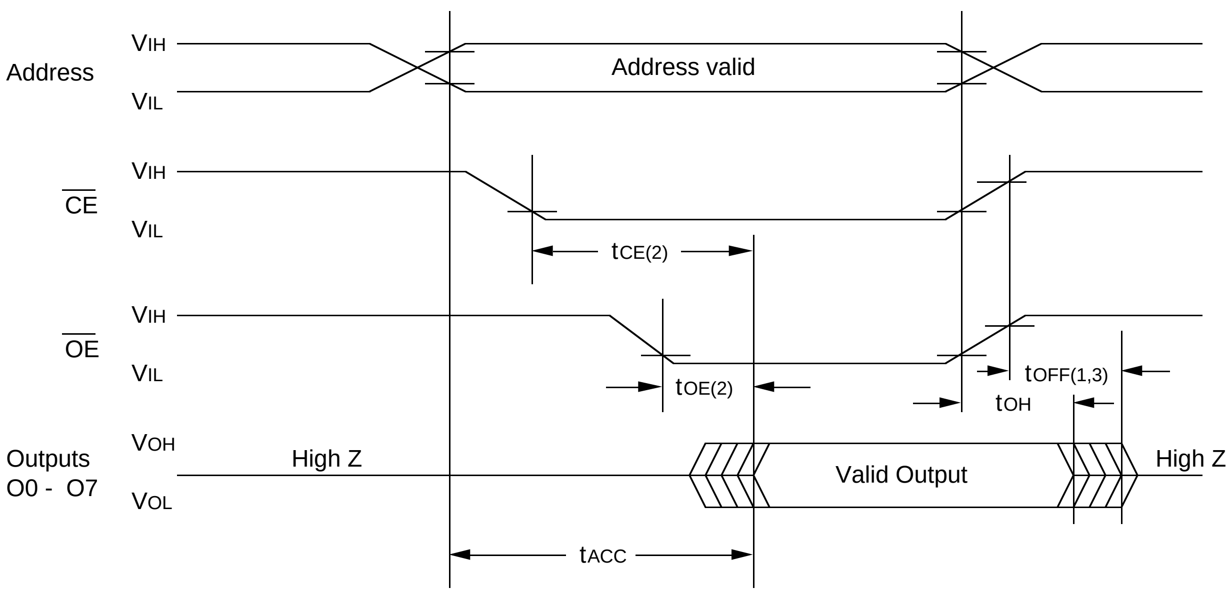
* Parts: C=Commercial Temperature Range
I =Industrial Temperature Ranges

Note 1: Typical active current increases .75 mA per MHz up to operating frequency for all temperature ranges.

TABLE 1-3: READ OPERATION AC CHARACTERISTICS

AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V V_{OL} = 0.8V Output Load: 1 TTL Load + 100 pF Input Rise and Fall Times: 10 ns Ambient Temperature: Commercial: Tamb = 0°C to +70°C Industrial: Tamb = -40°C to +85°C									
Parameter	**Sym**	**27HC256-20**		**27HC256-25**		**27HC256-30**		**Units**	**Conditions**
		Min	**Max**	**Min**	**Max**	**Min**	**Max**		
Address to Output Delay	t_{ACC}	—	200	—	250	—	300	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}	—	200	—	250	—	300	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}	—	100	—	125	—	125	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ to O/P High Impedance	t_{OFF}	0	50	0	50	0	50	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever goes first	t_{OH}	0	—	0	—	0	—	ns	

FIGURE 1-1: READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first

(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}

(3) This parameter is sampled and is not 100% tested.

I

TABLE 1-4: PROGRAMMING DC CHARACTERISTICS

Ambient Temperature: Tamb = 25°C ± 5°C
VCC = 6.5V ± 0.25V, VPP = 13.0V ± 0.25V

Parameter	Status	Symbol	Min	Max.	Units	Conditions
Input Voltages	Logic"1" Logic"0"	VIH VIL	2.0 -0.1	VCC+1 0.8	V V	
Input Leakage	—	ILI	-10	10	μA	VIN = 0V to VCC
Output Voltages	Logic"1" Logic"0"	VOH VOL	2.4	 0.45	V V	IOH = -400 μA IOL = 2.1 mA
VCC Current, program & verify	—	ICC2	—	20	mA	Note 1
VPP Current, program	—	IPP2	—	25	mA	Note 1
A9 Product Identification	—	VH	11.5	12.5	V	

Note 1: VCC must be applied simultaneously or before VPP and removed simultaneously or after VPP.

TABLE 1-5: PROGRAMMING AC CHARACTERISTICS

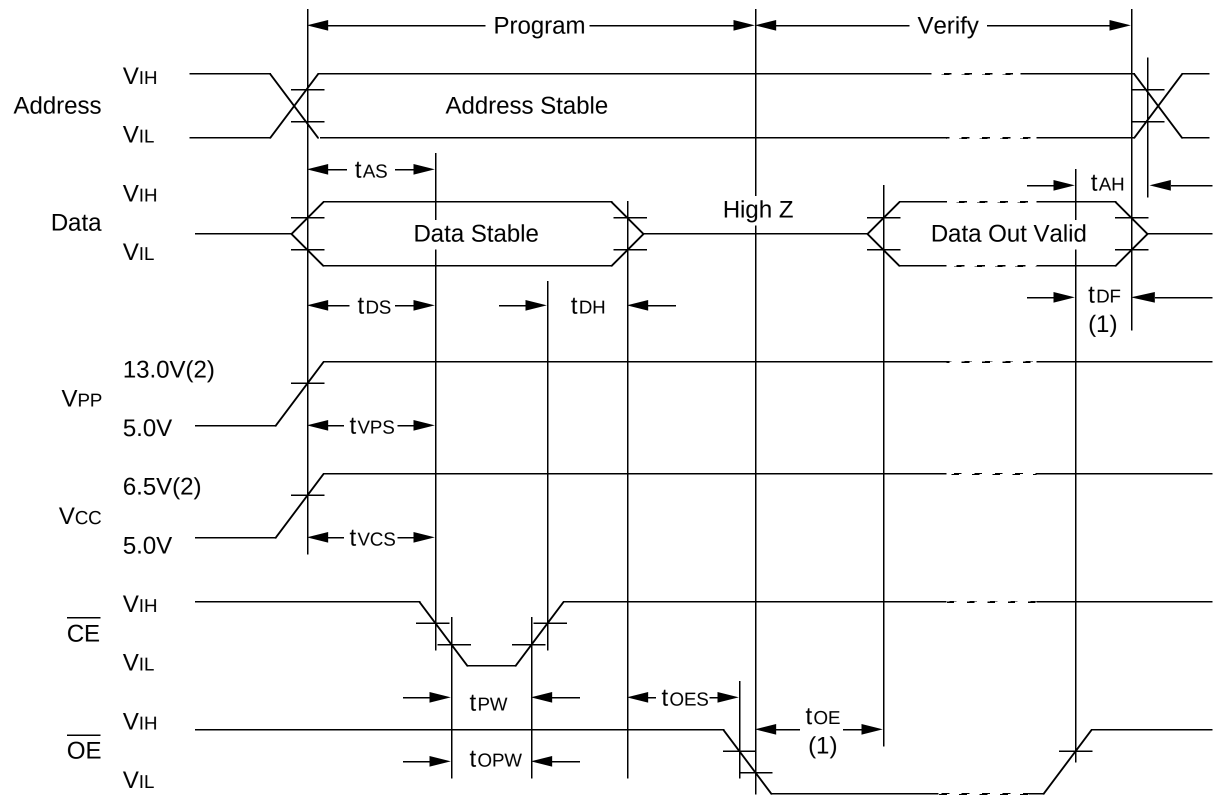
for Program, Program Verify and Program Inhibit Modes

AC Testing Waveform: VIH=2.4V and VIL=0.45V; VOH=2.0V; VOL=0.8V
Output Load: 1 TLL Load + 100pF
Ambient Temperature: Tamb=25°C±5°C
VCC= 6.5V ± 0.25V, VPP =13.0V ± 0.25V

Parameter	Symbol	Min.	Max.	Units	Remarks
Address Set-Up Time	tAS	2	—	μs	
Data Set-Up Time	tDS	2	—	μs	
Data Hold Time	tDH	2	—	μs	
Address Hold Time	tAH	0	—	μs	
Float Delay (2)	tDF	0	130	ns	
VCC Set-Up Time	tVCS	2	—	μs	
Program Pulse Width (1)	tPW	95	105	μs	100 μs typical
$\overline{\text{CE}}$ Set-Up Time	tCES	2	—	μs	
$\overline{\text{OE}}$ Set-Up Time	tOES	2	—	μs	
VPP Set-Up Time	tVPS	2	—	μs	
Data Valid from $\overline{\text{OE}}$	tOE	—	100	ns	

Note 1: For express algorithm, initial programming width tolerance is 100 μs ±5%.
2: This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

FIGURE 1-2: PROGRAMMING WAVEFORMS



Notes: (1) t_{DF} and t_{OE} are characteristics of the device but must be accommodated by the programmer
(2) V_{CC} = 6.5V ±0.25V, V_{PP} = V_H = 13.0V ±0.25V for express algorithm

TABLE 1-6: MODES

Operation Mode	$\overline{CE}$	$\overline{OE}$	V_{PP}	A9	O0 - O7
Read	V_{IL}	V_{IL}	V_{CC}	X	D_{OUT}
Program	V_{IL}	V_{IH}	V_H	X	D_{IN}
Program Verify	V_{IH}	V_{IL}	V_H	X	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	V_H	X	High Z
Standby	V_{IH}	X	V_{CC}	X	High Z
Output Disable	V_{IL}	V_{IH}	V_{CC}	X	High Z
Identity	V_{IL}	V_{IL}	V_{CC}	V_H	Identity Code

X = Don't Care

1.2 Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when:

a) the $\overline{CE}$ pin is low to power up (enable) the chip

b) the $\overline{OE}$ pin is low to gate the data to the output pins

For Read operations, if the addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is transferred to the output after a delay from the falling edge of $\overline{OE}$ (t_{OE}).

1.3 Standby Mode

The standby mode is defined when the $\overline{CE}$ pin is high (V_{IH}) and a program mode is not defined. Output Disable

1.4 Output Enable

This feature eliminates bus contention in multiple bus microprocessor systems and the outputs go to a high impedance when the following condition is true:

- The $\overline{OE}$ pin is high and program mode is not defined.

1.5 Programming Mode

The Express algorithm has been developed to improve on the programming throughput times in a production environment. Up to 10 100-microsecond pulses are applied until the byte is verified. No over-programming is required. A flowchart of the express algorithm is shown in Figure 1.

Programming takes place when:

a) V_{CC} is brought to the proper voltage
b) V_{PP} is brought to the proper V_H level
c) the $\overline{OE}$ pin is high
d) the $\overline{CE}$ pin is low

Since the erased state is “1” in the array, programming of “0” is required. The address to be programmed is set via pins A0-A14 and the data to be programmed is presented to pins O0-O7. When data and address are stable, a low-going pulse on the $\overline{CE}$ line programs that location.

1.6 Verify

After the array has been programmed it must be verified to ensure that all the bits have been correctly programmed. This mode is entered when all of the following conditions are met:

a) V_{CC} is at the proper level
b) V_{PP} is at the proper V_H level
c) the $\overline{CE}$ pin is high
d) the $\overline{OE}$ line is low

1.7 Inhibit

When Programming multiple devices in parallel with different data, only $\overline{CE}$ needs to be under separate control to each device. By pulsing the $\overline{CE}$ line low on a particular device, that device will be programmed, and all other devices with $\overline{CE}$ held high will not be programmed with the data although address and data are available on their input pins.

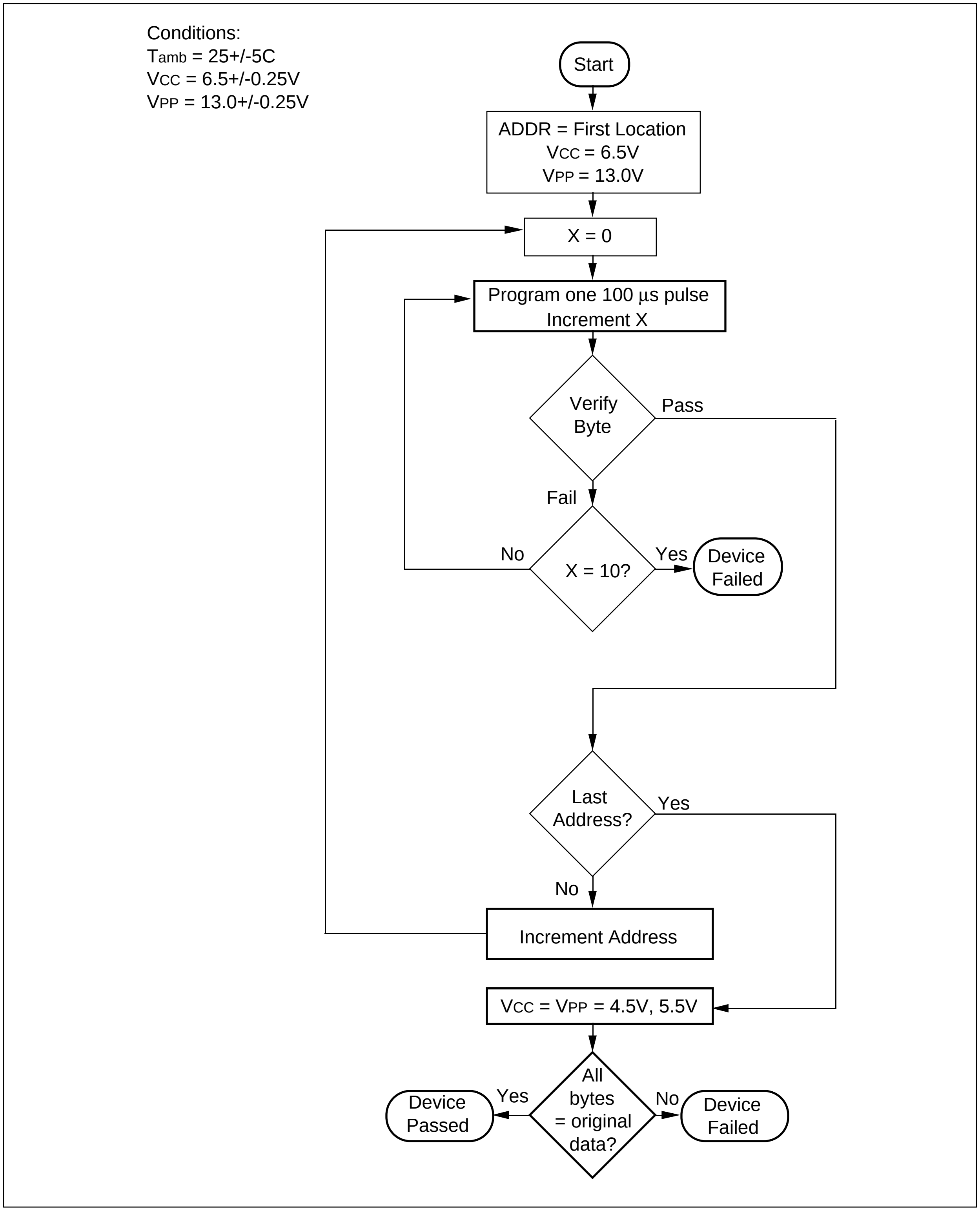
1.8 Identity Mode

In this mode specific data is outputted which identifies the manufacturer as Microchip Technology Inc. and device type. This mode is entered when Pin A9 is taken to V_H (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$ lines must be at V_{IL}. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin	**Input**	**Output**								
Identity	A0	07	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	V_{IL}	0	0	1	0	1	0	0	1	29
Device Type*	V_{IH}	1	0	0	0	1	1	0	0	8C

* Code subject to change.

FIGURE 1-3: PROGRAMMING EXPRESS ALGORITHM



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27LV256 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

27LV256 – 25 I /P

Package:	L	=	Plastic Leaded Chip Carrier
	P	=	Plastic DIP (600 Mil)
	SO	=	Plastic SOIC (300 Mil)
Temperature Range:	Blank	=	0˚C to +70˚C
	I	=	-40˚C to +85˚C
Access Time:	20	=	200 ns
	25	=	250 ns
	30	=	300 ns (SOIC only)
Device:	27LV256		256K (32K x 8) Low-Voltage CMOS EPROM

Note the following details of the code protection feature on PICmicro® MCUs.

- The PICmicro family meets the specifications contained in the Microchip Data Sheet.
- Microchip believes that its family of PICmicro microcontrollers is one of the most secure products of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the PICmicro microcontroller in a manner outside the operating specifications contained in the data sheet. The person doing so may be engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable”.
- Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our product.

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