NEC

MOS INTEGRATED CIRCUIT
μPD780031Y, 780032Y, 780033Y, 780034Y

8-BIT SINGLE-CHIP MICROCONTROLLERS

DESCRIPTION

The μPD780031Y, 780032Y, 780033Y, and 780034Y are products based on the μPD780031, 780032, 780033, and 780034, with an I²C bus interface supporting multimaster added to make them suitable for application in AV equipment.

A flash memory version, the μPD78F0034Y which can operate in the same power supply voltage range as the mask ROM version, and various development tools, are also under development.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD780024, 780034, 780024Y, 780034Y Subseries User's Manual : U12022E
78K/0 Series User's Manual – Instructions : U12326E

FEATURES

- Internal ROM and RAM

Item / Part Number	Program Memory (Internal ROM)	Data Memory (Internal High-Speed RAM)	Package
μPD780031Y	8 Kbytes	512 bytes	• 64-pin plastic shrink DIP (750 mils) • 64-pin plastic QFP (14 × 14 mm) • 64-pin plastic LQFP (12 × 12 mm)
μPD780032Y	16 Kbytes		
μPD780033Y	24 Kbytes	1024 bytes	
μPD780034Y	32 Kbytes		

- External memory expansion space: 64 Kbytes
- Minimum instruction execution time: 0.24 μs (at fx = 8.38-MHz operation)
★ • I/O ports: 51 (N-ch open-drain 5-V withstand voltage: 4)
- 10-bit resolution A/D converter: 8 channels (AV$_{DD}$ = 2.7 to 5.5 V)
- Serial interface: 3 channels
- Timer: 5 channels
- Power supply voltage: V$_{DD}$ = 1.8 to 5.5 V

APPLICATIONS

Telephones, home electric appliances, pagers, AV equipment, car audios, office automation equipment, etc.

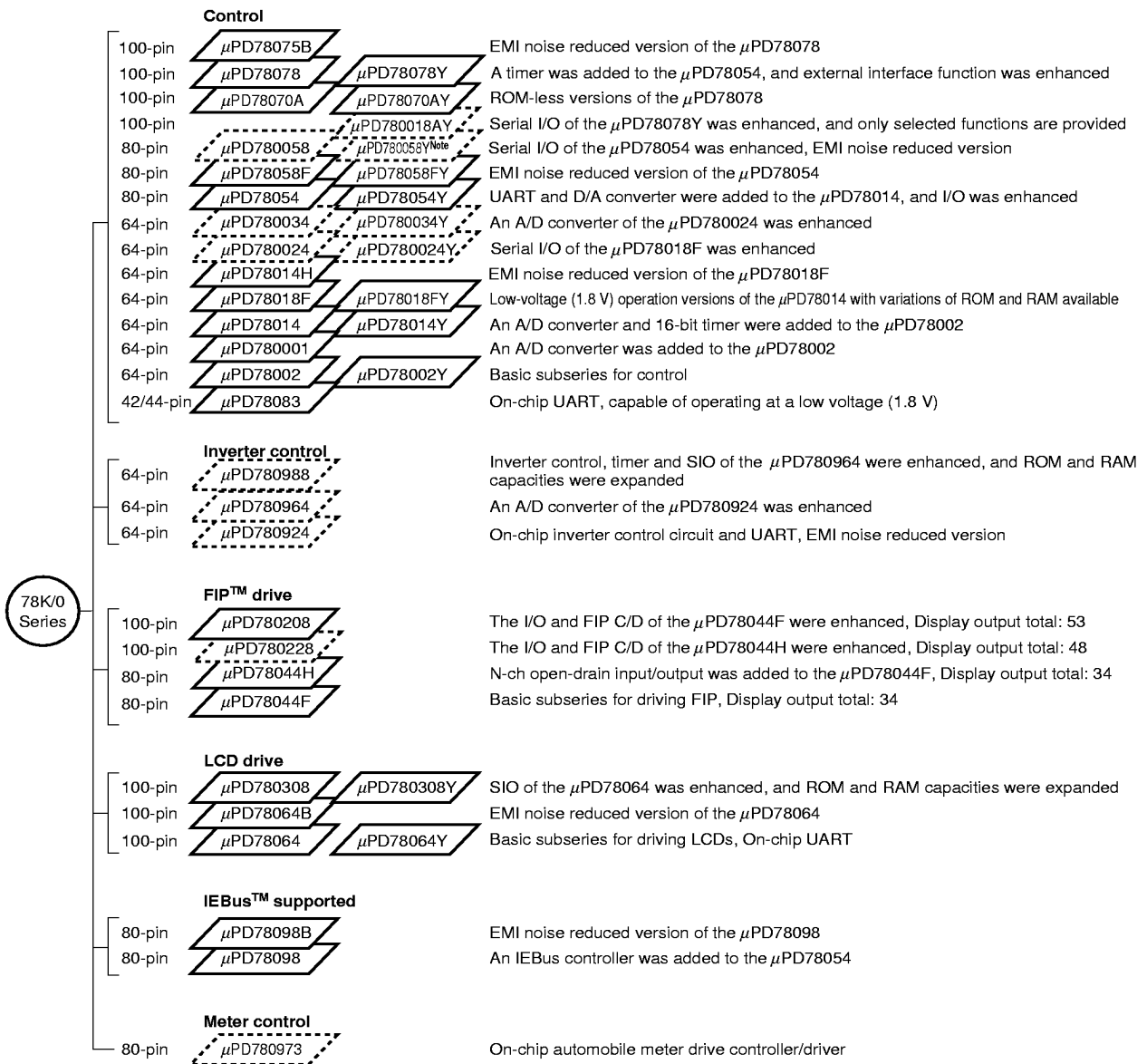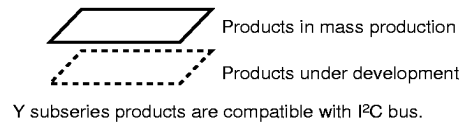**The information in this document is subject to change without notice.**

The mark ★ shows major revised points.

ORDERING INFORMATION

Part Number	Package
μPD780031YCW-×××	64-pin plastic shrink DIP (750 mils)
μPD780031YGC-×××-AB8	64-pin plastic QFP (14 × 14 mm)
μPD780031YGK-×××-8A8	64-pin plastic LQFP (12 × 12 mm)
μPD780032YCW-×××	64-pin plastic shrink DIP (750 mils)
μPD780032YGC-×××-AB8	64-pin plastic QFP (14 × 14 mm)
μPD780032YGK-×××-8A8	64-pin plastic LQFP (12 × 12 mm)
μPD780033YCW-×××	64-pin plastic shrink DIP (750 mils)
μPD780033YGC-×××-AB8	64-pin plastic QFP (14 × 14 mm)
μPD780033YGK-×××-8A8	64-pin plastic LQFP (12 × 12 mm)
μPD780034YCW-×××	64-pin plastic shrink DIP (750 mils)
μPD780034YGC-×××-AB8	64-pin plastic QFP (14 × 14 mm)
μPD780034YGK-×××-8A8	64-pin plastic LQFP (12 × 12 mm)

Remark ××× indicates the ROM code suffix.

★   **78K/0 SERIES PRODUCT DEVELOPMENT**

These products are a further development in the 78K/0 Series. The designations appearing inside the boxes are subseries names.

Products in mass production

Products under development

Y subseries products are compatible with I²C bus.

Control

100-pin	μPD78075B	EMI noise reduced version of the μPD78078
100-pin	μPD78078 / μPD78078Y	A timer was added to the μPD78054, and external interface function was enhanced
100-pin	μPD78070A / μPD78070AY	ROM-less versions of the μPD78078
100-pin	μPD780018AY	Serial I/O of the μPD78078Y was enhanced, and only selected functions are provided
80-pin	μPD780058 / μPD780058Y Note	Serial I/O of the μPD78054 was enhanced, EMI noise reduced version
80-pin	μPD78058F / μPD78058FY	EMI noise reduced version of the μPD78054
80-pin	μPD78054 / μPD78054Y	UART and D/A converter were added to the μPD78014, and I/O was enhanced
64-pin	μPD780034 / μPD780034Y	An A/D converter of the μPD780024 was enhanced
64-pin	μPD780024 / μPD780024Y	Serial I/O of the μPD78018F was enhanced
64-pin	μPD78014H	EMI noise reduced version of the μPD78018F
64-pin	μPD78018F / μPD78018FY	Low-voltage (1.8 V) operation versions of the μPD78014 with variations of ROM and RAM available
64-pin	μPD78014 / μPD78014Y	An A/D converter and 16-bit timer were added to the μPD78002
64-pin	μPD780001	An A/D converter was added to the μPD78002
64-pin	μPD78002 / μPD78002Y	Basic subseries for control
42/44-pin	μPD78083	On-chip UART, capable of operating at a low voltage (1.8 V)

Inverter control

64-pin	μPD780988	Inverter control, timer and SIO of the μPD780964 were enhanced, and ROM and RAM capacities were expanded
64-pin	μPD780964	An A/D converter of the μPD780924 was enhanced
64-pin	μPD780924	On-chip inverter control circuit and UART, EMI noise reduced version

FIP™ drive

100-pin	μPD780208	The I/O and FIP C/D of the μPD78044F were enhanced, Display output total: 53
100-pin	μPD780228	The I/O and FIP C/D of the μPD78044H were enhanced, Display output total: 48
80-pin	μPD78044H	N-ch open-drain input/output was added to the μPD78044F, Display output total: 34
80-pin	μPD78044F	Basic subseries for driving FIP, Display output total: 34

LCD drive

100-pin	μPD780308 / μPD780308Y	SIO of the μPD78064 was enhanced, and ROM and RAM capacities were expanded
100-pin	μPD78064B	EMI noise reduced version of the μPD78064
100-pin	μPD78064 / μPD78064Y	Basic subseries for driving LCDs, On-chip UART

IEBus™ supported

80-pin	μPD78098B	EMI noise reduced version of the μPD78098
80-pin	μPD78098	An IEBus controller was added to the μPD78054

Meter control

80-pin	μPD780973	On-chip automobile meter drive controller/driver

78K/0 Series

Note   Under planning

The major functional differences among the Y subseries are shown below.

Function / Subseries Name		ROM Capacity	Configuration of Serial Interface		I/O	V_{DD} MIN. Value
Control	μPD78078Y	48 K to 60 K	3-wire/2-wire/I²C	: 1 ch	88	1.8 V
	μPD78070A	–	3-wire with automatic transmit/receive function	: 1 ch	61	2.7 V
			3-wire/UART	: 1 ch		
	μPD780018AY	48 K to 60 K	3-wire with automatic transmit/receive function	: 1 ch	88	
			Time-division 3-wire	: 1 ch		
			I²C bus (multimaster supported)	: 1 ch		
	μPD780058Y	24 K to 60 K	3-wire/2-wire/I²C	: 1 ch	68	1.8 V
			3-wire with automatic transmit/receive function	: 1 ch		
			3-wire/time-division UART	: 1 ch		
	μPD78058FY	48 K to 60 K	3-wire/2-wire/I²C	: 1 ch	69	2.7 V
	μPD78054Y	16 K to 60 K	3-wire with automatic transmit/receive function	: 1 ch		2.0 V
			3-wire/UART	: 1 ch		
	μPD780034Y	8 K to 32 K	UART	: 1 ch	51	1.8 V
	μPD780024Y		3-wire	: 1 ch		
			I²C bus (multimaster supported)	: 1 ch		
	μPD78018FY	8 K to 60 K	3-wire/2-wire/I²C	: 1 ch	53	
			3-wire with automatic transmit/receive function	: 1 ch		
	μPD78014Y	8 K to 32 K	3-wire/2-wire/SBI/I²C	: 1 ch		2.7 V
			3-wire with automatic transmit/receive function	: 1 ch		
	μPD78002Y	8 K to 16 K	3-wire/2-wire/SBI/I²C	: 1 ch		
LCD drive	μPD780308Y	48 K to 60 K	3-wire/2-wire/I²C	: 1 ch	57	2.0 V
			3-wire/time-division UART	: 1 ch		
			3-wire	: 1 ch		
	μPD78064Y	16 K to 32 K	3-wire/2-wire/I²C	: 1 ch	57	
			3-wire/UART	: 1 ch		

Remark   The functions other than the serial interface are common to the Subseries without Y.

FUNCTION OVERVIEW

Item	Part Number	μPD780031Y	μPD780032Y	μPD780033Y	μPD780034Y
Internal memory	ROM	8 Kbytes	16 Kbytes	24 Kbytes	32 Kbytes
	High-speed RAM	512 bytes		1024 bytes	
Memory space		64 Kbytes			
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)			
Minimum instruction execution time		On-chip variable function of minimum instruction execution time			
	When main system clock selected	0.24 μs/0.48 μs/0.95 μs/1.91 μs/3.81 μs (at 8.38-MHz operation)			
	When subsystem clock selected	122 μs (at 32.768-kHz operation)			
Instruction set		• 16-bit operation • Multiply/divide (8 bits × 8 bits,16 bits ÷ 8 bits) • Bit manipulate (set, reset, test, Boolean operation) • BCD adjust, etc.			
I/O ports		Total : 51 • CMOS input : 8 • CMOS I/O : 39 • N-ch open-drain I/O (5-V withstand voltage) : 4			
A/D converter		• 10-bit resolution × 8 channels • Low-voltage operation available: AV_{DD} = 2.7 to 5.5 V			
Serial interface		• 3-wire serial I/O mode : 1 channel • UART mode : 1 channel • I²C bus mode (multimaster supported) : 1 channel			
Timer		• 16-bit timer/event counter : 1 channel • 8-bit timer/event counter : 2 channels • Watch timer : 1 channel • Watchdog timer : 1 channel			
Timer output		3 (8-bit PWM output capable: 2)			
Clock output		• 65.5 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.10 MHz, 4.19 MHz, 8.38 MHz (at 8.38-MHz operation with main system clock) • 32.768 kHz (at 32.768-kHz operation with subsystem clock)			
Buzzer output		1.02 kHz, 2.05 kHz, 4.10 kHz, 8.19 kHz (at 8.38-MHz operation with main system clock)			
Vectored interrupt source	Maskable	Internal : 13, external : 5			
	Non-maskable	Internal : 1			
	Software	1			
Power supply voltage		V_{DD} = 1.8 to 5.5 V			
Operating ambient temperature		T_A = −40 to +85°C			
Package		• 64-pin plastic shrink DIP (750 mils) • 64-pin plastic QFP (14 × 14 mm) • 64-pin plastic LQFP (12 × 12 mm)			

★

Preliminary Data Sheet

5

CONTENTS

1. PIN CONFIGURATION (Top View)

- **64-pin plastic shrink DIP (750 mils)**
  μPD780031YCW-xxx, 780032YCW-xxx, 780033YCW-xxx, 780034YCW-xxx
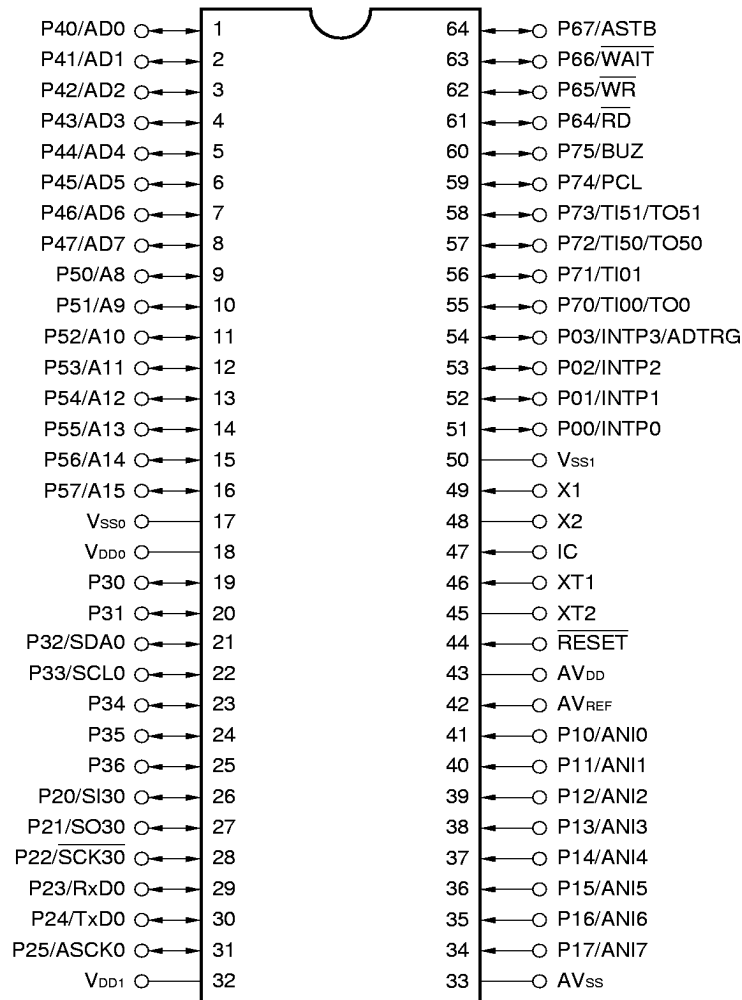
P40/AD0	1	64	P67/ASTB
P41/AD1	2	63	P66/$\overline{\text{WAIT}}$
P42/AD2	3	62	P65/$\overline{\text{WR}}$
P43/AD3	4	61	P64/$\overline{\text{RD}}$
P44/AD4	5	60	P75/BUZ
P45/AD5	6	59	P74/PCL
P46/AD6	7	58	P73/TI51/TO51
P47/AD7	8	57	P72/TI50/TO50
P50/A8	9	56	P71/TI01
P51/A9	10	55	P70/TI00/TO0
P52/A10	11	54	P03/INTP3/ADTRG
P53/A11	12	53	P02/INTP2
P54/A12	13	52	P01/INTP1
P55/A13	14	51	P00/INTP0
P56/A14	15	50	V$_{SS1}$
P57/A15	16	49	X1
V$_{SS0}$	17	48	X2
V$_{DD0}$	18	47	IC
P30	19	46	XT1
P31	20	45	XT2
P32/SDA0	21	44	$\overline{\text{RESET}}$
P33/SCL0	22	43	AV$_{DD}$
P34	23	42	AV$_{REF}$
P35	24	41	P10/ANI0
P36	25	40	P11/ANI1
P20/SI30	26	39	P12/ANI2
P21/SO30	27	38	P13/ANI3
P22/$\overline{\text{SCK30}}$	28	37	P14/ANI4
P23/RxD0	29	36	P15/ANI5
P24/TxD0	30	35	P16/ANI6
P25/ASCK0	31	34	P17/ANI7
V$_{DD1}$	32	33	AV$_{SS}$

★ **Cautions 1. Connect the IC (Internally Connected) pin directly to V$_{SS0}$ or V$_{SS1}$.**
　　　　　　2. Connect the AV$_{SS}$ pin to V$_{SS0}$.

Remark When the μPD780031Y, 780032Y, 780033Y, and 780034Y are used in applications where the noise generated inside the microcontroller needs to be reduced, the implementation of noise reduction measures, such as supplying voltage to V$_{DD0}$ and V$_{DD1}$ individually and connecting V$_{SS0}$ and V$_{SS1}$ to different ground lines, is recommended.

- **64-pin plastic QFP (14 × 14 mm)**
  μPD780031YGC-xxx-AB8, 780032YGC-xxx-AB8, 780033YGC-xxx-AB8, 780034YGC-xxx-AB8
- **64-pin plastic LQFP (12 × 12 mm)**
  μPD780031YGK-xxx-8A8, 780032YGK-xxx-8A8, 780033YGK-xxx-8A8, 780034YGK-xxx-8A8

Top pins (64→49): P47/AD7, P46/AD6, P45/AD5, P44/AD4, P43/AD3, P42/AD2, P41/AD1, P40/AD0, P67/ASTB, P66/$\overline{WAIT}$, P65/$\overline{WR}$, P64/$\overline{RD}$, P75/BUZ, P74/PCL, P73/TI51/TO51, P72/TI50/TO50

Left pins:
Pin	Signal
1	P50/A8
2	P51/A9
3	P52/A10
4	P53/A11
5	P54/A12
6	P55/A13
7	P56/A14
8	P57/A15
9	V_{SS0}
10	V_{DD0}
11	P30
12	P31
13	P32/SDA0
14	P33/SCL0
15	P34
16	P35

Right pins:
Pin	Signal
48	P71/TI01
47	P70/TI00/TO0
46	P03/INTP3/ADTRG
45	P02/INTP2
44	P01/INTP1
43	P00/INTP0
42	V_{SS1}
41	X1
40	X2
39	IC
38	XT1
37	XT2
36	$\overline{RESET}$
35	AV_{DD}
34	AV_{REF}
33	P10/ANI0

Bottom pins (17→32): P36, P20/SI30, P21/SO30, P22/$\overline{SCK30}$, P23/RxD0, P24/TxD0, P25/ASCK0, V_{DD1}, AV_{SS}, P17/ANI7, P16/ANI6, P15/ANI5, P14/ANI4, P13/ANI3, P12/ANI2, P11/ANI1

★ **Cautions 1. Connect the IC (Internally Connected) pin directly to V_{SS0} or V_{SS1}.**
       2. Connect the AV_{SS} pin to V_{SS0}.

Remark When the μPD780031Y, 780032Y, 780033Y, and 780034Y are used in applications where the noise generated inside the microcontroller needs to be reduced, the implementation of noise reduction measures, such as supplying voltage to V_{DD0} and V_{DD1} individually and connecting V_{SS0} and V_{SS1} to different ground lines, is recommended.

A8 to A15	: Address Bus	P70 to P75	: Port 7
AD0 to AD7	: Address/Data Bus	PCL	: Programmable Clock
ADTRG	: AD Trigger Input	$\overline{RD}$	: Read Strobe
ANI0 to ANI7	: Analog Input	$\overline{RESET}$	: Reset
ASCK0	: Asynchronous Serial Clock	RxD0	: Receive Data
ASTB	: Address Strobe	$\overline{SCK30}$	: Serial Clock
AV_{DD}	: Analog Power Supply	SCL0	: Serial Clock
AV_{REF}	: Analog Reference Voltage	SDA0	: Serial Data
AV_{SS}	: Analog Ground	SI30	: Serial Input
BUZ	: Buzzer Clock	SO30	: Serial Output
IC	: Internally Connected	TI00, TI01, TI50, TI51	: Timer Input
INTP0 to INTP3	: Interrupt from Peripherals	TO0, TO50, TO51	: Timer Output
P00 to P03	: Port 0	TxD0	: Transmit Data
P10 to P17	: Port 1	V_{DD0}, V_{DD1}	: Power Supply
P20 to P25	: Port 2	V_{SS0}, V_{SS1}	: Ground
P30 to P36	: Port 3	$\overline{WAIT}$	: Wait
P40 to P47	: Port 4	$\overline{WR}$	: Write Strobe
P50 to P57	: Port 5	X1, X2	: Crystal (Main System Clock)
P64 to P67	: Port 6	XT1, XT2	: Crystal (Subsystem Clock)

2. BLOCK DIAGRAM
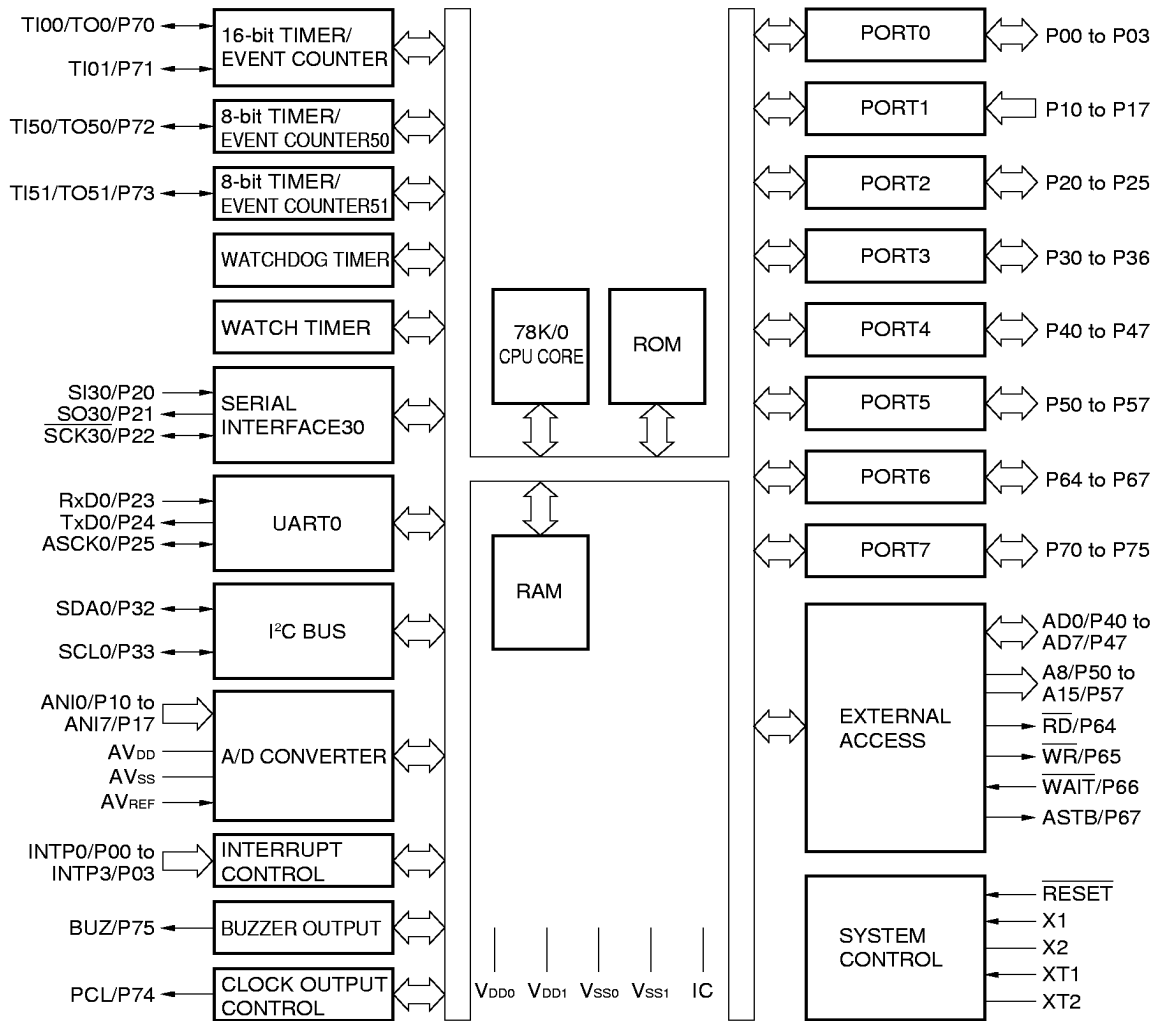
Remark   The internal ROM and RAM capacities depend on the product.

3. PIN FUNCTIONS

3.1 Port Pins (1/2)

Pin Name	I/O	Function		After Reset	Alternate Function
P00	I/O	Port 0 4-bit input/output port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be connected by software.		Input	INTP0
P01					INTP1
P02					INTP2
P03					INTP3/ADTRG
P10 to P17	Input	Port 1 8-bit input only port.		Input	ANI0 to ANI7
P20	I/O	Port 2 6-bit input/output port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be connected by software.		Input	SI30
P21					SO30
P22					$\overline{\text{SCK30}}$
P23					RxD0
P24					TxD0
P25					ASCK0
P30	I/O	Port 3 7-bit input/output port. Input/output can be specified bit-wise.	N-ch open-drain input/output port. P30 and P31 on-chip pull-up resistors can be specified by mask option. LEDs can be driven directly.	Input	—
P31					
P32					SDA0
P33					SCL0
P34			When used as an input port, an on-chip pull-up resistor can be connected by software.		—
P35					
P36					
P40 to P47	I/O	Port 4 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be connected by software. Interrupt request flag (KRIF) is set to 1 by the falling edge detection.		Input	AD0 to AD7
P50 to P57	I/O	Port 5 8-bit input/output port. LEDs can be driven directly. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be connected by software.		Input	A8 to A15
P64	I/O	Port 6 4-bit input/output port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be connected by software.		Input	$\overline{\text{RD}}$
P65					$\overline{\text{WR}}$
P66					$\overline{\text{WAIT}}$
P67					ASTB

3.1 Port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
P70	I/O	Port 7 6-bit input/output port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be connected by software.	Input	TI00/TO0
P71				TI01
P72				TI50/TO50
P73				TI51/TO51
P74				PCL
P75				BUZ

3.2 Non-port Pins (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising edge and falling edge) can be specified.	Input	P00
INTP1				P01
INTP2				P02
INTP3				P03/ADTRG
SI30	Input	Serial interface serial data input.	Input	P20
SO30	Output	Serial interface serial data output.	Input	P21
SDA0	I/O	Serial interface serial data input/output.	Input	P32
$\overline{\text{SCK30}}$	I/O	Serial interface serial clock input/output.	Input	P22
SCL0				P33
RxD0	Input	Serial data input for asynchronous serial interface.	Input	P23
TxD0	Output	Serial data output for asynchronous serial interface.	Input	P24
ASCK0	Input	Serial clock input for asynchronous serial interface.	Input	P25
TI00	Input	External count clock input to 16-bit timer (TM0). Capture trigger input to capture register (CR01) of 16-bit timer (TM0).	Input	P70/TO0
TI01		Capture trigger input to capture register (CR00) of 16-bit timer (TM0).		P71
TI50		External count clock input to 8-bit timer (TM50).		P72/TO50
TI51		External count clock input to 8-bit timer (TM51).		P73/TO51
TO0	Output	16-bit timer (TM0) output.	Input	P70/TI00
TO50		8-bit timer (TM50) output (shared with 8-bit PWM output).	Input	P72/TI50
TO51		8-bit timer (TM51) output (shared with 8-bit PWM output).		P73/TI51
PCL	Output	Clock output (for trimming of main system clock and subsystem clock).	Input	P74
BUZ	Output	Buzzer output.	Input	P75
AD0 to AD7	I/O	Lower address/data bus for extending memory externally.	Input	P40 to P47
A8 to A15	Output	Higher address bus for extending memory externally.	Input	P50 to P57
$\overline{\text{RD}}$	Output	Strobe signal output for read operation of external memory.	Input	P64
$\overline{\text{WR}}$		Strobe signal output for write operation of external memory.		P65
$\overline{\text{WAIT}}$	Input	Inserting wait for accessing external memory.	Input	P66
ASTB	Output	Strobe output which externally latches address information output to port 4 and port 5 to access external memory.	Input	P67

3.2 Non-port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
ANI0 to ANI7	Input	A/D converter analog input.	Input	P10 to P17
ADTRG	Input	A/D converter trigger signal input.	Input	P03/INTP3
AV$_{REF}$	Input	A/D converter reference voltage input.	—	—
AV$_{DD}$	—	A/D converter analog power supply. Set the same potential as that of V$_{DD0}$ or V$_{DD1}$.	—	—
AV$_{SS}$	—	A/D converter ground potential. Set the same potential as that of V$_{SS0}$ or V$_{SS1}$.	—	—
$\overline{\text{RESET}}$	Input	System reset input.	—	—
X1	Input	Connecting crystal resonator for main system clock oscillation.	—	—
X2	—		—	X2
XT1	Input	Connecting crystal resonator for subsystem clock oscillation.	—	—
XT2	—		—	—
V$_{DD0}$	—	Positive power supply for ports.	—	—
V$_{SS0}$	—	Ground potential of ports.	—	—
V$_{DD1}$	—	Positive power supply (except ports).	—	—
V$_{SS1}$	—	Ground potential (except ports).	—	—
IC	—	Internally connected. Connect directly to V$_{SS0}$ or V$_{SS1}$.	—	—

★

3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 3-1. For the input/output circuit configuration of each type, see Figure 3-1.

Table 3-1. Input/Output Circuit Type of Each Pin

Pin Name	Input/output Circuit Type	I/O	Recommended Connection when not Used
P00/INTP0	8-C	Input	Independently connect to V_{SS0} via a resistor .
P01/INTP1			
P02/INTP2			
P03/INTP3			
P10/ANI0 to P17/ANI7	25	Input	Independently connect to V_{DD0} or V_{SS0} via a resistor.
P20/SI30	8-C	Input/output	
P21/SO30	5-H		
P22/$\overline{SCK30}$	8-C		
P23/RxD0			
P24/TxD0	5-H		
P25/ASCK0	8-C		
★ P30, P31	13-Q	Input/output	Independently connect to V_{DD0} via a resistor .
★ P32/SDA0	13-R		
P33/SCL0			
P34	8-C		Independently connect to V_{DD0} or V_{SS0} via a resistor .
P35	5-H		
P36	8-C		
P40/AD0 to P47/AD7	5-H	Input/output	Independently connect to V_{DD0} via a resistor.
P50/A8 to P57/A15		Input/output	Independently connect to V_{DD0} or V_{SS0} via a resistor.
P64/$\overline{RD}$		Input/output	
P65/$\overline{WR}$			
P66/$\overline{WAIT}$			
P67/ASTB			
P70/TI00/TO0	8-C		
P71/TI01			
P72/TI50/TO50			
P73/TI51/TO51			
P74/PCL	5-H		
P75/BUZ			
$\overline{RESET}$	2	Input	—
XT1	16		Connect to V_{DD0}.
XT2		—	Leave open.
AV_{DD}	—		Connect to V_{DD0}.
★ AV_{REF}			Connect to V_{SS0}.
★ AV_{SS}			
★ IC			Connect directly to V_{SS0} or V_{SS1}.

Figure 3-1. Pin Input/Output Circuits

TYPE 2

IN ○————▷ (Schmitt-Triggered symbol) ○————▶

Schmitt-Triggered Input with Hysteresis Characteristics

TYPE 13-R ★

data
output disable ———▷ (NOR) ○——| N-ch ————○ IN/OUT

V_{SS0}

◀——————○ (Schmitt)

TYPE 5-H

V_{DD0}

pullup enable ———▷○——| P-ch

V_{DD0}

data ———| (NAND) ○——| P-ch

output disable ———| (NOR) ○——| N-ch ————○ IN/OUT

V_{SS0}

input enable ◀——— (NAND)

TYPE 16

feedback cut-off

P-ch

———◁◁◁———| |———●————▷○——▶

———▷○———

XT1   XT2

TYPE 8-C

V_{DD0}

pullup enable ———▷○——| P-ch

V_{DD0}

data ———| (NAND) ○——| P-ch

output disable ———| (NOR) ○——| N-ch ————○ IN/OUT

V_{SS0}

◀——— (Schmitt)

TYPE 25

P-ch

Comparator ▷—+ |——

— === N-ch

V_{SS0}

V_{REF} (threshold voltage)   ○ IN

input enable ◀——— (NAND)

TYPE 13-Q

V_{DD0}

(Mask Option) ⌇

data
output disable ———▷○ (NOR)——| N-ch ————○ IN/OUT

V_{SS0}

input enable ◀——— (NAND)

4. MEMORY SPACE

Figure 4-1 shows the memory map of the μPD780031Y, 780032Y, 780033Y, and 780034Y.

Figure 4-1. Memory Map
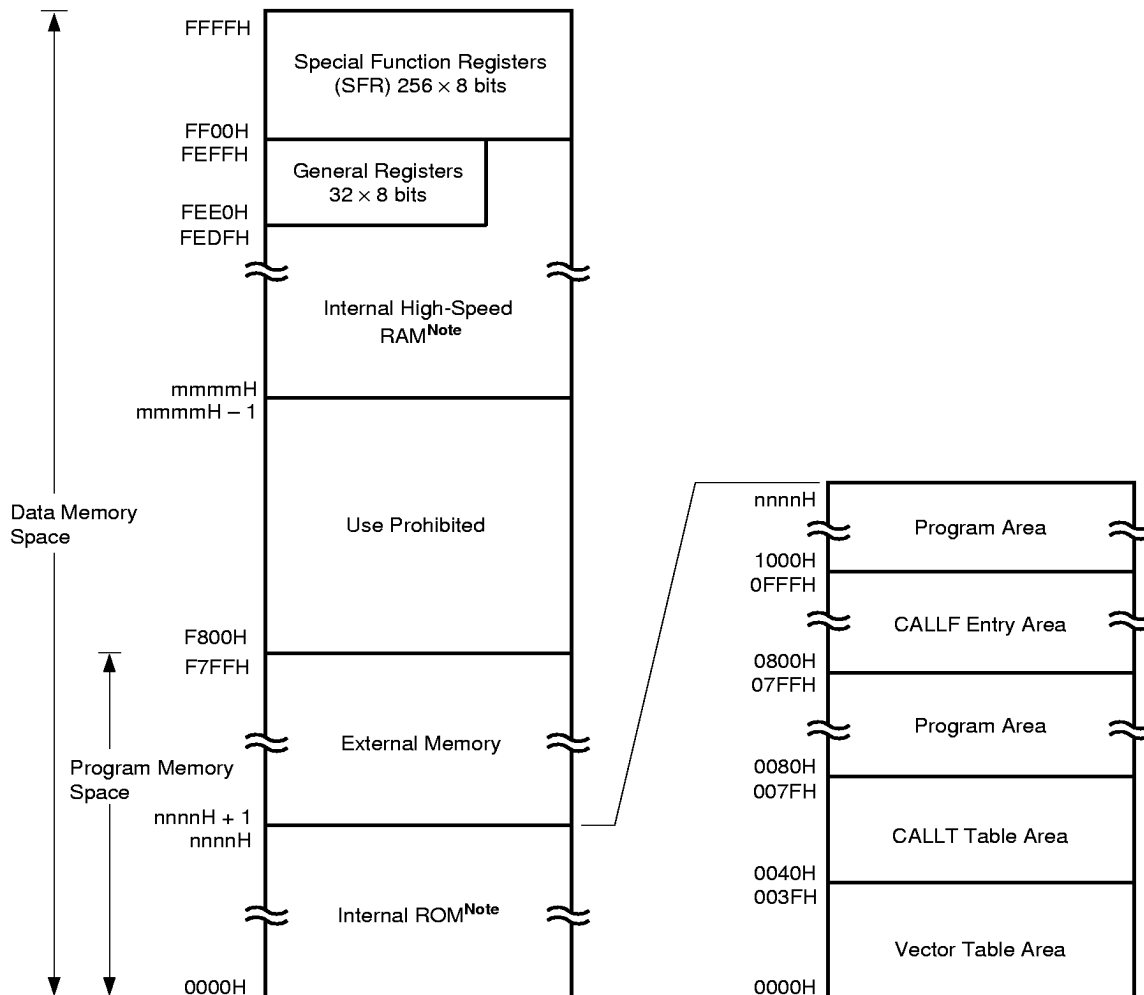
Note   The internal ROM capacity and internal high-speed RAM capacity depend on the products (see the following table).

Part Number	Internal ROM Last Address nnnnH	Internal High-Speed RAM Start Address mmmmH
μPD780031Y	1FFFH	FD00H
μPD780032Y	3FFFH	
μPD780033Y	5FFFH	FB00H
μPD780034Y	7FFFH	

5. PERIPHERAL HARDWARE FUNCTION FEATURES

5.1 Ports

The following 3 types of I/O ports are available.

- CMOS input (Port 1)   : 8
- CMOS input/output (Port 0, Port 2 to Port 7)   : 39
- N-channel open-drain input/output (P30 to P33)   : 4

    Total   : 51

Table 5-1. Port Functions

Name	Pin Name	Function
Port 0	P00 to P03	Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be connected by software.
Port 1	P10 to P17	Input-only port pins.
Port 2	P20 to P25	Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be connected by software.
Port 3	P30 to P33	N-ch open-drain input/output port pins. Input/output specifiable bit-wise. On-chip pull-up resistor can be connected by mask option. LEDs can be driven directly.
	P34 to P36	Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be connected by software.
Port 4	P40 to P47	Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be connected by software. Test input flag (KRIF) is set to 1 by falling edge detection.
Port 5	P50 to P57	Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be connected by software. LEDs can be driven directly.
Port 6	P64 to P67	Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be connected by software.
Port 7	P70 to P75	Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be connected by software.

5.2 Clock Generator

A system clock generator is incorporated.

Also, the variation of the minimum instruction execution time is available.

* 0.24 μs/0.48 μs/0.95 μs/1.91 μs/3.81 μs (at 8.38-MHz operation with main system clock)

* 122 μs (at 32.768-kHz operation with subsystem clock)

Figure 5-1. Block Diagram of Clock Generator
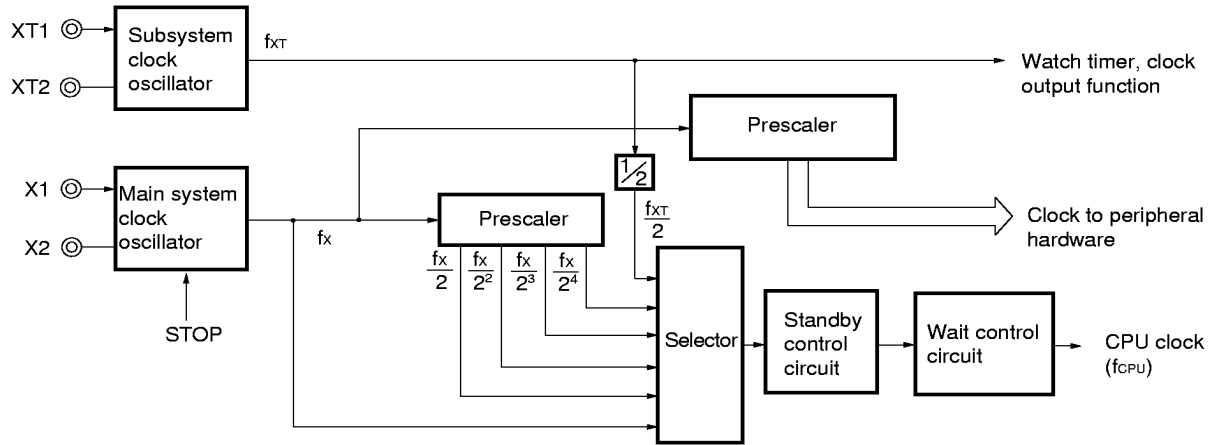
5.3 Timer/Counter

Five timer/counter channels are incorporated.

- 16-bit timer/event counter : 1 channel
- 8-bit timer/event counter : 2 channels
- Watch timer   : 1 channel
- Watchdog timer   : 1 channel

Table 5-2. Operations of Timer/Event Counter

		16-Bit Timer/ Event Counter TM0	8-Bit Timer/ Event Counter TM50, TM51	Watch Timer	Watchdog Timer
Operation mode					
	Interval timer	2 channels[Note 1]	2 channels	1 channel[Note 2]	1 channel[Note 3]
	External event counter	1 channel	2 channels	—	—
Function					
	Timer output	1 output	2 outputs	—	—
	PWM output	—	2 outputs	—	—
	Pulse width measurement	2 inputs	—	—	—
	Square wave output	1 output	2 outputs	—	—
	One-shot pulse output	1 output	—	—	—
	Interrupt source	2	2	2	1

Notes 1. When capture/compare registers 00, 01 (CR00, CR01) are both specified as compare registers
   2. The watch timer can perform both watch timer and interval timer functions at the same time.
   3. The watchdog timer has the watchdog timer and interval timer functions. However, use the watchdog timer by selecting either the watchdog timer function or the interval timer function.

Figure 5-2. Block Diagram of 16-bit Timer/Event Counter TM0
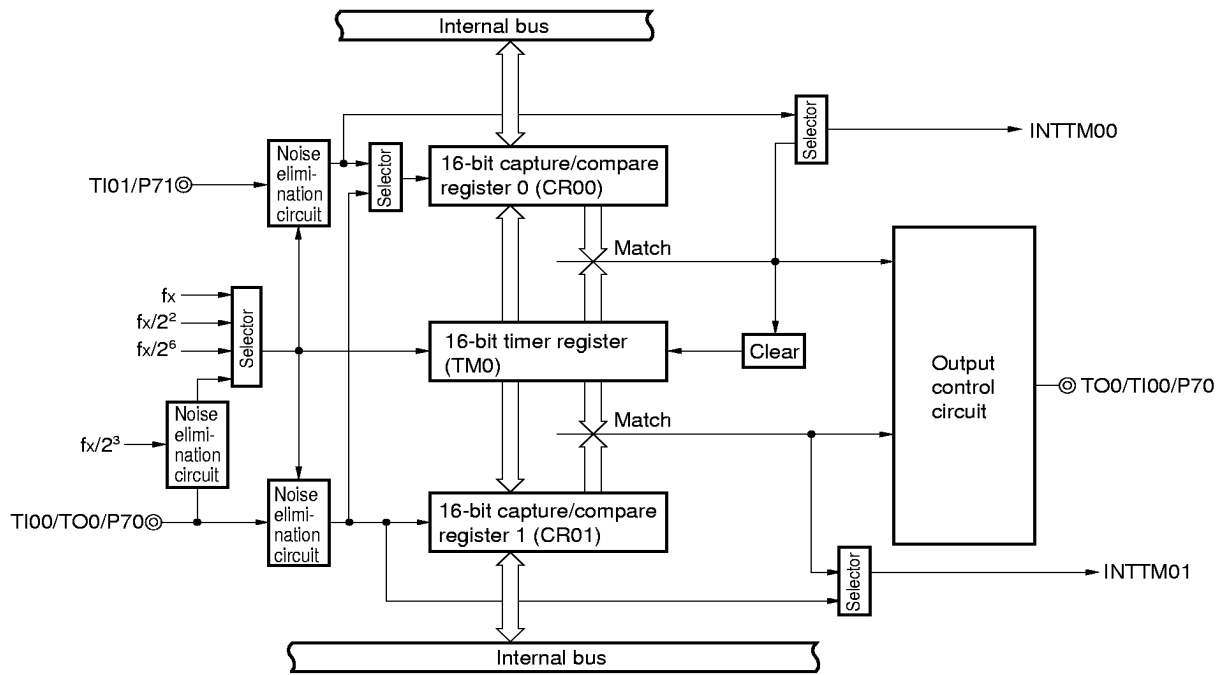
Figure 5-3. Block Diagram of 8-bit Timer/Event Counter TM50
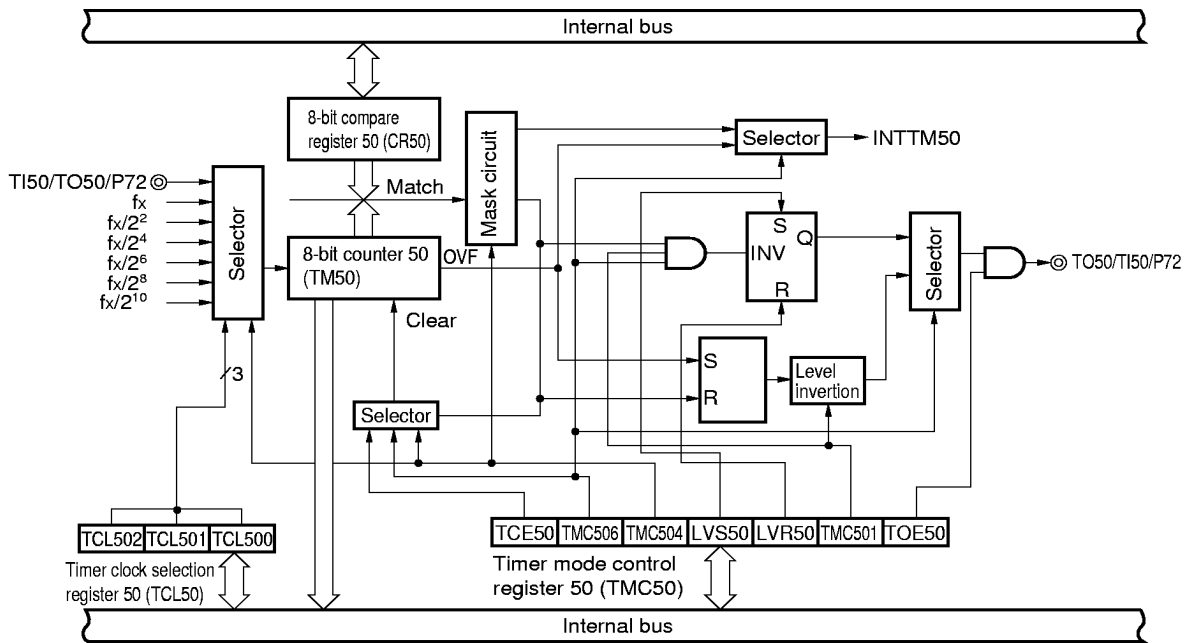
Figure 5-4. Block Diagram of 8-bit Timer/Event Counter TM51
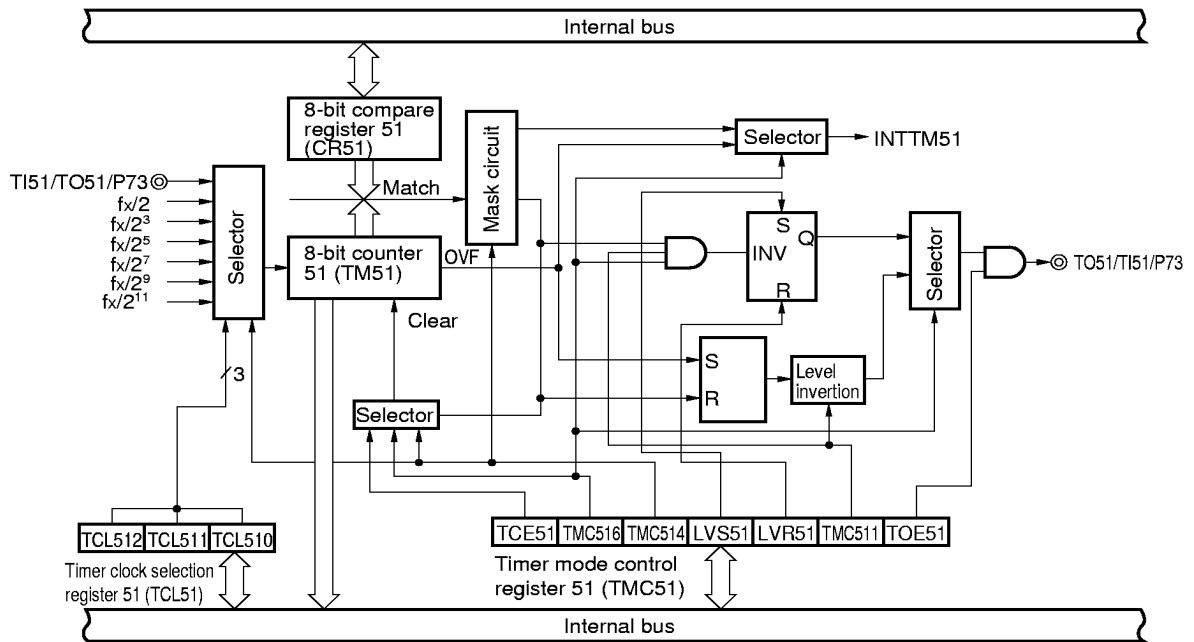
Figure 5-5. Block Diagram of Watch Timer
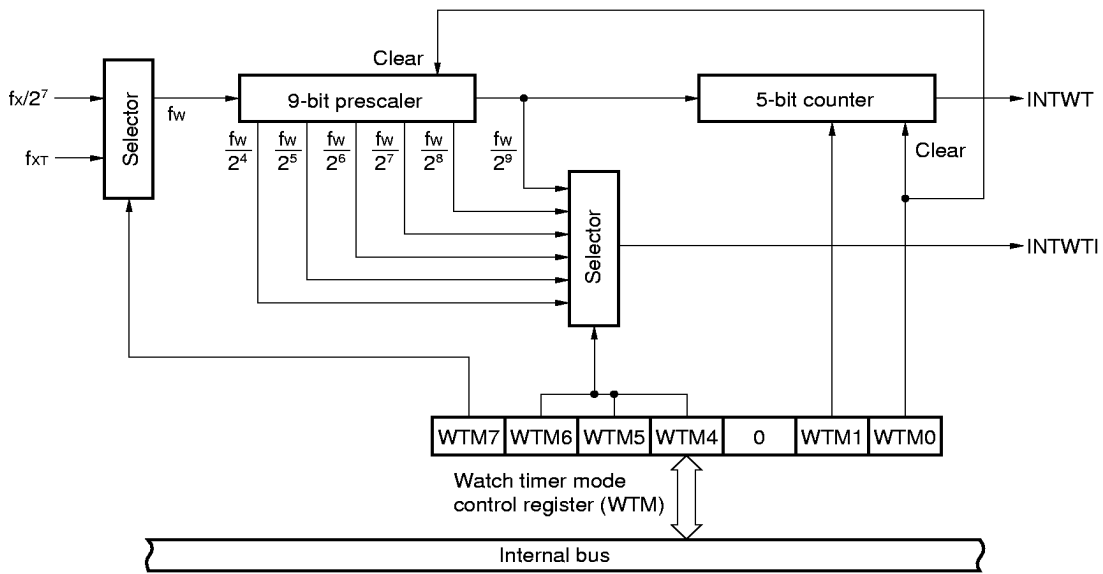
★ **Figure 5-6. Block Diagram of Watchdog Timer**
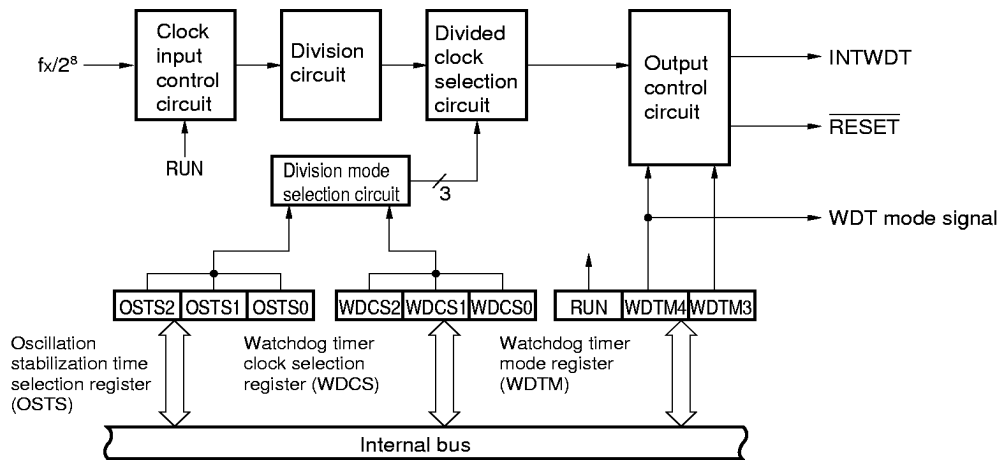
5.4 Clock Output/Buzzer Output Control Circuit

A clock output/buzzer output control circuit (CKU) is incorporated.

Clocks with the following variation of frequency can be output as a clock output.

- 65.5 kHz/131 kHz/262 kHz/524 kHz/1.05 MHz/2.10 MHz/4.19 MHz/8.38 MHz (at 8.38-MHz operation with main system clock)
- 32.768 kHz (at 32.768-kHz operation with subsystem clock)

Clocks with the following variation of frequency can be output as a buzzer output.

- 1.02 kHz/2.05 kHz/4.10 kHz/8.19 kHz (at 8.38-MHz operation with main system clock)

★

Figure 5-7. Block Diagram of Clock Output/Buzzer Output Control Circuit CKU
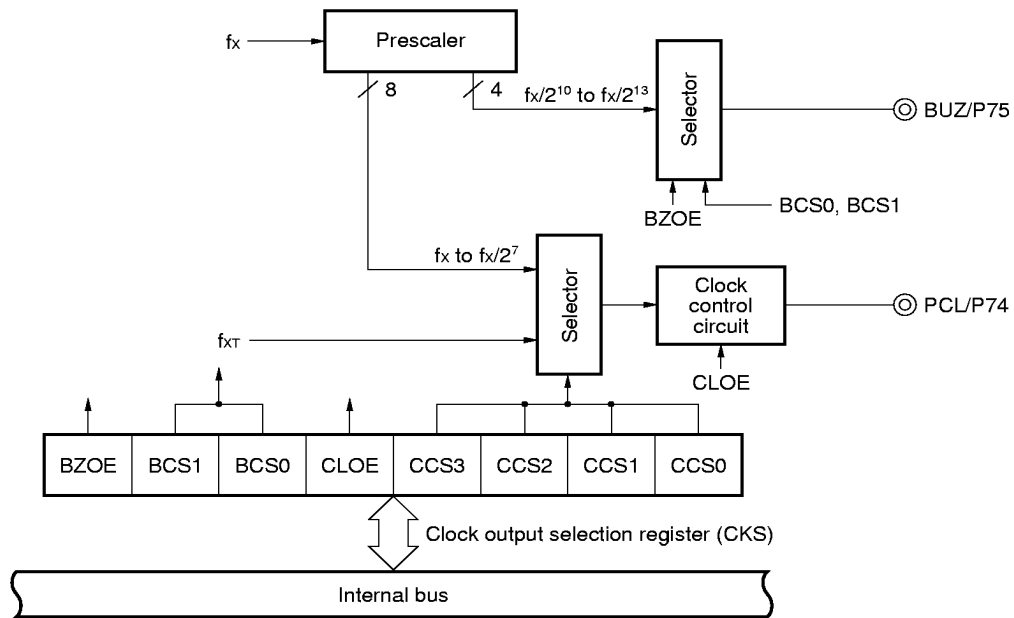
5.5 A/D Converter

An A/D converter of 10-bit resolution × 8 channels is incorporated.

The following two types of the A/D conversion operation start-up methods are available.

• Hardware start

• Software start

Figure 5-8. Block Diagram of A/D Converter
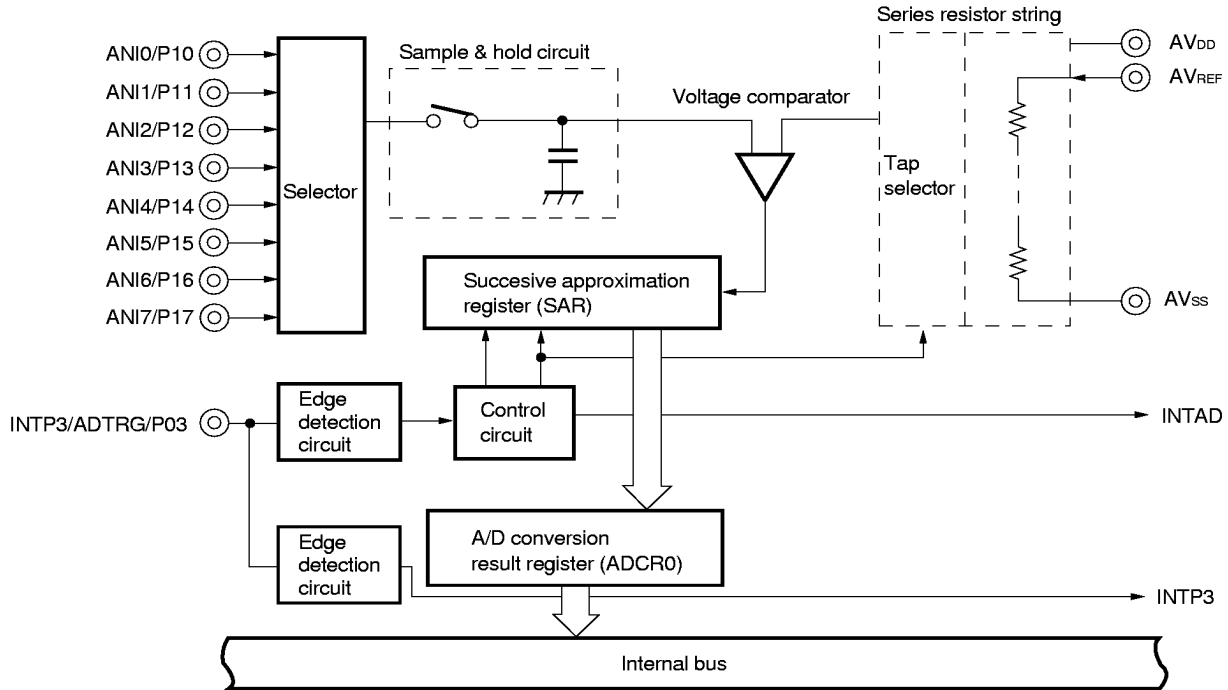
5.6 Serial Interface

Three channels of the serial interface are incorporated.

- Serial interface UART0
- Serial interface SIO30
- Serial interface IIC0

(1) Serial interface UART0

The serial interface UART0 has two modes, asynchronous serial interface (UART) mode and infrared data transfer mode.

- **Asynchronous serial interface (UART) mode**

  This mode enables full-duplex operation wherein one byte of data is transmitted and received after the start bit.

  The on-chip dedicated UART baud rate generator enables communication using a wide range of selectable baud rates. In addition, a baud rate can be also defined by dividing the clock input to the ASCK0 pin.

  The dedicated UART baud rate generator can also be used to generate a MIDI-standard baud rate (31.25 kbps).

★
- **Infrared data transfer mode**

  This mode enables pulse output and pulse reception in data format.

  This mode can be used for office equipment applications such as personal computers.

Figure 5-9. Block Diagram of Serial Interface UART0
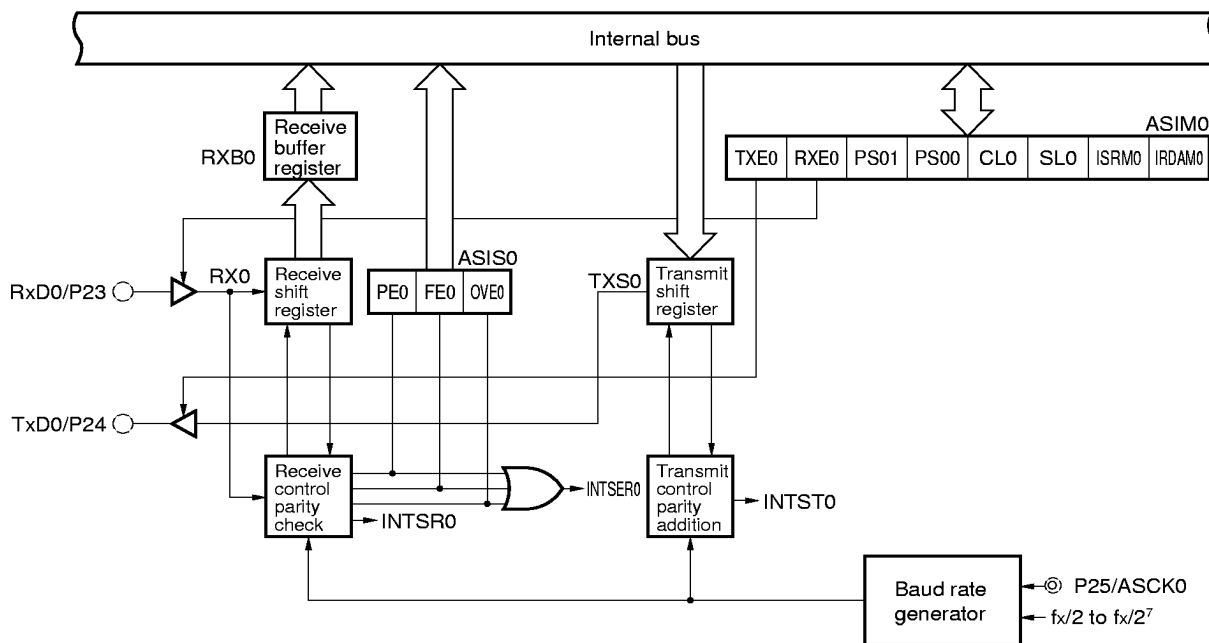
(2) Serial interface SIO30

The serial interface SIO30 has the 3-wire serial I/O mode.

* **3-wire serial I/O mode (fixed as MSB first)**

This is an 8-bit data transfer mode using three lines: serial clock line ($\overline{\text{SCK30}}$), serial output line (SO30), and serial input line (SI30).

Since simultaneous transmit and receive operations are available in the 3-wire serial I/O mode, the processing time for data transfer is reduced.

The first bit in 8-bit data in the serial transfer is fixed as MSB.

The 3-wire serial I/O mode is useful for connection to a peripheral I/O device that includes a clocked serial interface, a display controller, etc.

Figure 5-10. Block Diagram of Serial Interface SIO30
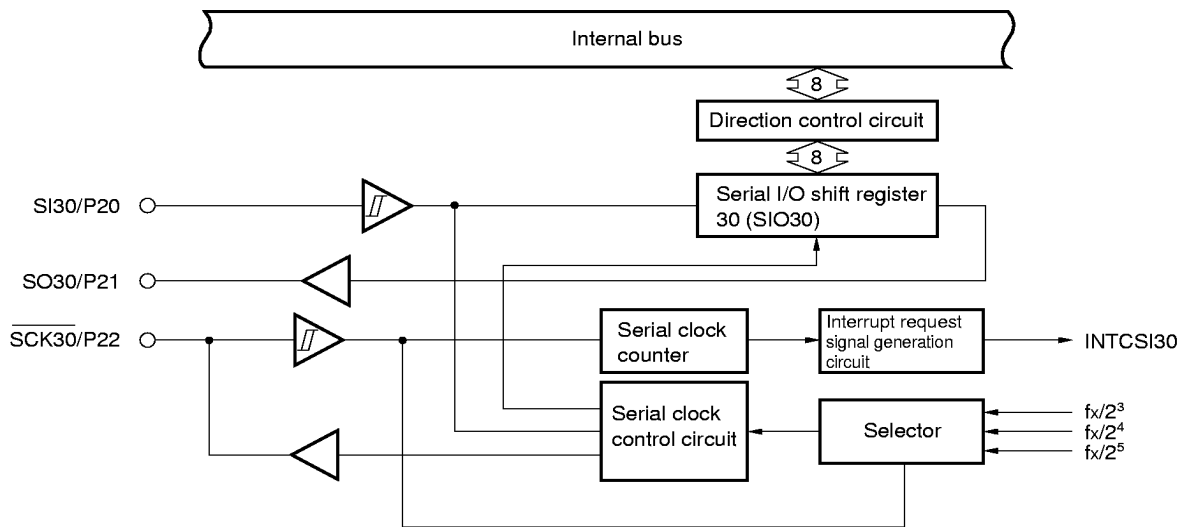
(3) Serial interface IIC0

The serial interface IIC0 has the I²C (Inter IC) bus mode (multimaster supported).

• I²C bus mode (multimaster supported)

This is an 8-bit data transfer mode using two lines: serial clock line (SCL0) and serial data bus line (SDA0). This mode complies with the I²C bus format, and can output "start condition", "data", and "stop condition" during transmission via the serial data bus. These data are automatically detected by hardware during reception.

Since the SCL0 and SDA0 are open-drain outputs in IIC0, pull-up resistors for the serial clock line and the serial data bus line are required.

★

Figure 5-11. Block Diagram of Serial Interface IIC0
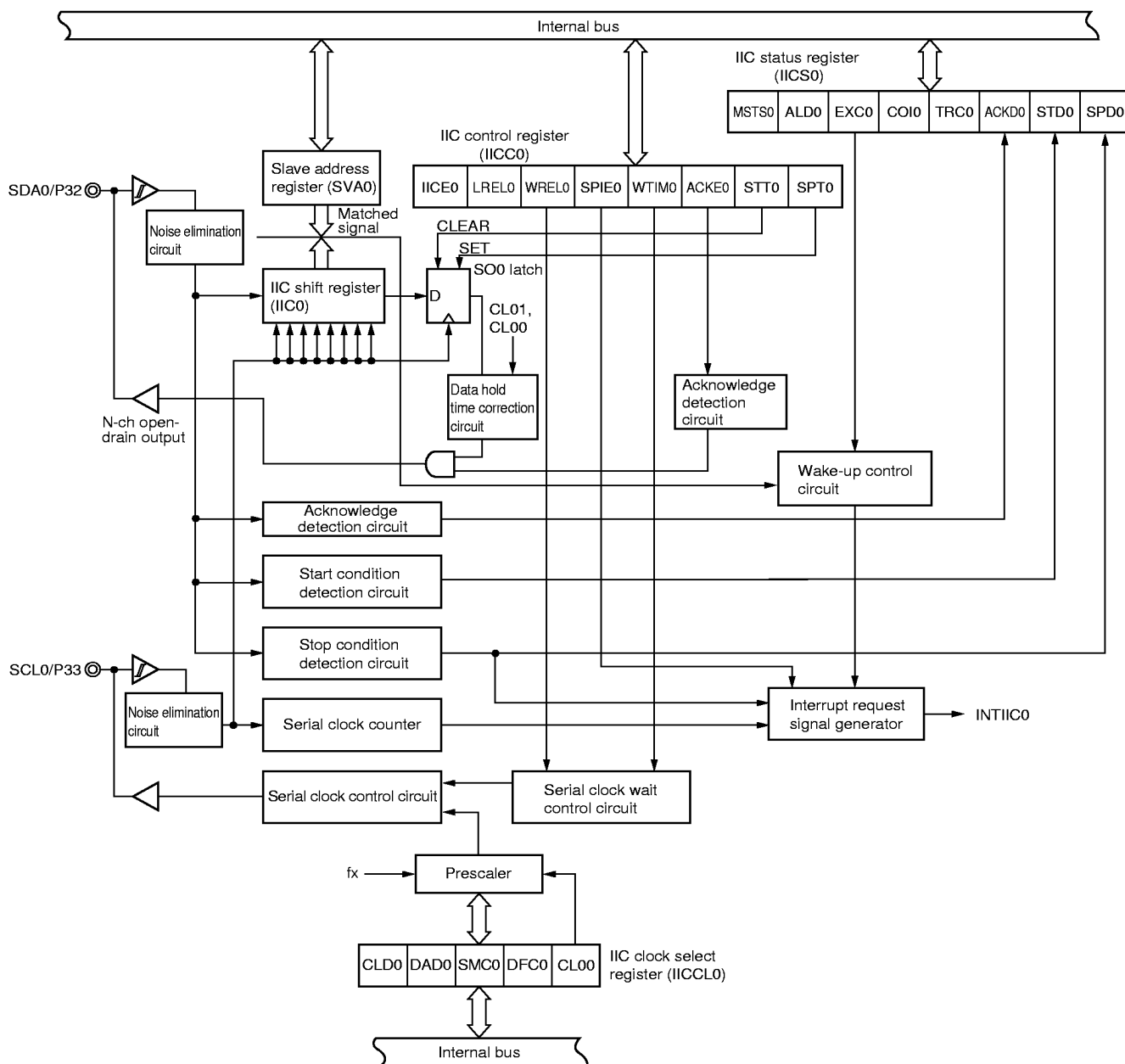
6. INTERRUPT FUNCTIONS

There are 20 interrupt functions of three different types, as shown below.
- Non-maskable: 1
- Maskable   : 18
- Software   : 1

★ **Table 6-1. Interrupt Source List**

Type of Interrupt	Default PriorityNote 1	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration TypeNote 2
		Name	Trigger			
Non-maskable	—	INTWDT	Watchdog timer overflow (watchdog timer mode 1 selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (interval timer mode selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	
	3	INTP2			000AH	
	4	INTP3			000CH	
	5	INTSER0	Generation of serial interface UART0 reception error	Internal	000EH	(B)
	6	INTSR0	End of serial interface UART0 reception		0010H	
	7	INTST0	End of serial interface UART0 transmission		0012H	
	8	INTCSI30	End of serial interface SIO3 (SIO30) transfer		0014H	
	9	INTIIC0	End of serial interface IIC0 transfer		0018H	
	10	INTWTI	Reference time interval signal from watch timer		001AH	
	11	INTTM00	Generation of coincidence signal of 16-bit timer register and capture/compare register 00 (CR00) (when CR00 is specified as compare register)		001CH	
	12	INTTM01	Generation of coincidence signal of 16-bit timer register and capture/compare register 01 (CR01) (when CR01 is specified as compare register)		001EH	
	13	INTTM50	Generation of coincidence signal of 8-bit timer/event counter 50		0020H	
	14	INTTM51	Generation of coincidence signal of 8-bit timer/event counter 51		0022H	
	15	INTAD0	End of conversion by A/D converter		0024H	
	16	INTWT	Watch timer overflow		0026H	
	17	INTKR	Falling edge detection of port 4	External	0028H	(D)
Software	—	BRK	BRK instruction execution	—	003EH	(E)

Notes 1. The default priority is a priority order when two or more maskable interrupt requests are generated simultaneously. 0 is the highest order and 17, the lowest.
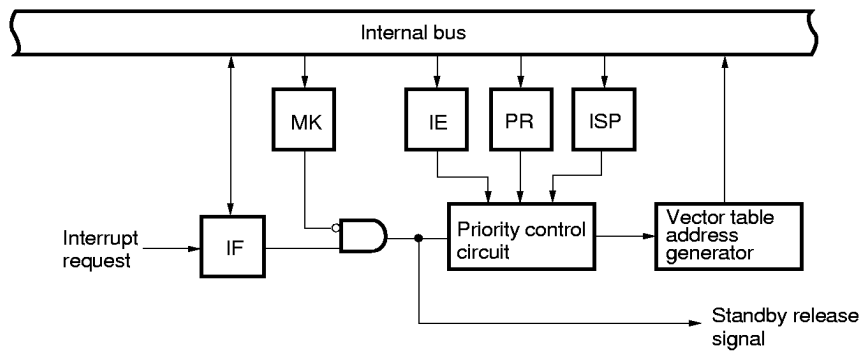**2.** Basic configuration types (A) to (E) correspond to (A) to (E) in Figure 6-1, respectively.

Figure 6-1. Basic Configuration of Interrupt Function (1/2)

(A) Internal non-maskable interrupt
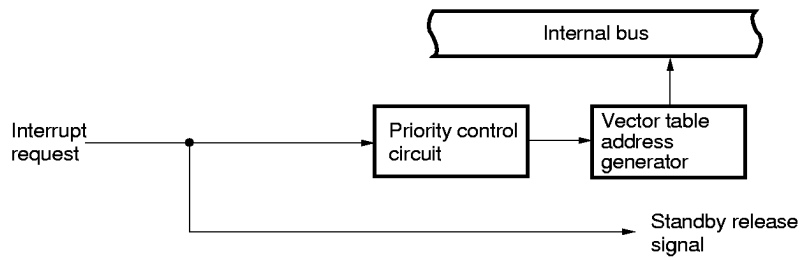
(B) Internal maskable interrupt

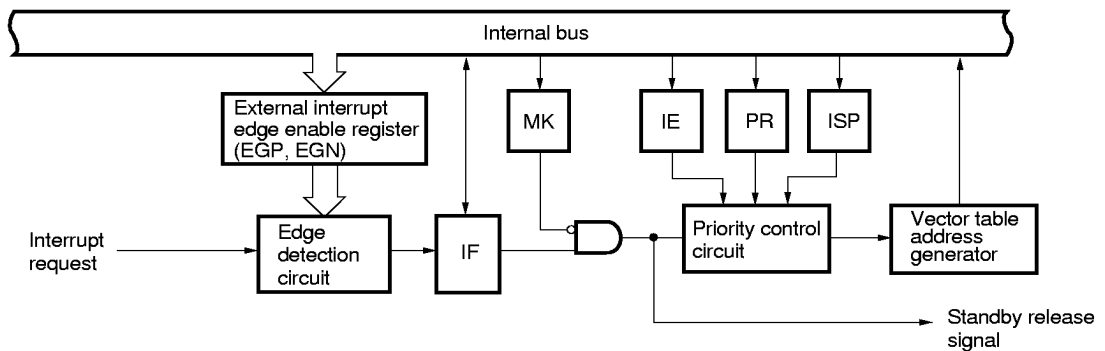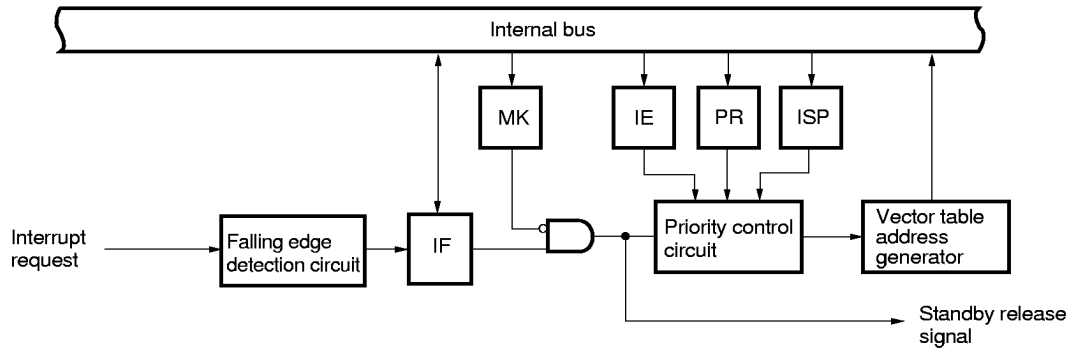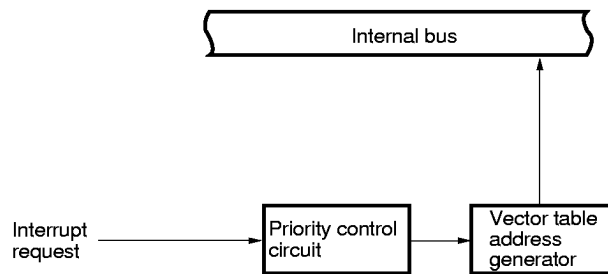**(C) External maskable interrupt (INTP0 to INTP3)**

Figure 6-1. Basic Configuration of Interrupt Function (2/2)

(D) External maskable interrupt (INTKR)

```
┌──────────────────────── Internal bus ────────────────────────┐
                          │      │    │    │                 │
                        ┌───┐  ┌───┐┌───┐┌───┐               │
                        │MK │  │IE ││PR ││ISP│               │
                        └───┘  └───┘└───┘└───┘               │
                          │      └──┼────┘                   │
            ┌───────────┐ │       ┌────────────┐  ┌─────────────┐
Interrupt ──│Falling edge│─┤IF├──▷─┤Priority     │──│Vector table │
request     │detection   │          │control      │  │address      │
            │circuit     │          │circuit      │  │generator    │
            └───────────┘          └────────────┘  └─────────────┘
                                         │
                                         └──────────► Standby release
                                                      signal
```

(E) Software interrupt

```
┌──────────────────── Internal bus ────────────────────┐
                                    │
                        ┌────────────┐  ┌─────────────┐
Interrupt ──────────────│Priority     │──│Vector table │
request                 │control      │  │address      │
                        │circuit      │  │generator    │
                        └────────────┘  └─────────────┘
```

IF   : Interrupt request flag
IE   : Interrupt enable flag
ISP : In-service priority flag
MK   : Interrupt mask flag
PR   : Priority specification flag

7. EXTERNAL DEVICE EXPANSION FUNCTIONS

The external device expansion functions connect external devices to areas other than the internal ROM, RAM and SFR. Ports 4 to 6 are used for external device connection.

8. STANDBY FUNCTIONS

There are the following two standby functions to reduce the consumption current.

• HALT mode: The CPU operating clock is stopped. The average consumption current can be reduced by intermittent operation in combination with the normal operating mode.
• STOP mode: The system clock oscillation is stopped. The whole operation by the system clock is stopped, so that the system operates with ultra-low power consumption.

Figure 8-1. Standby Function
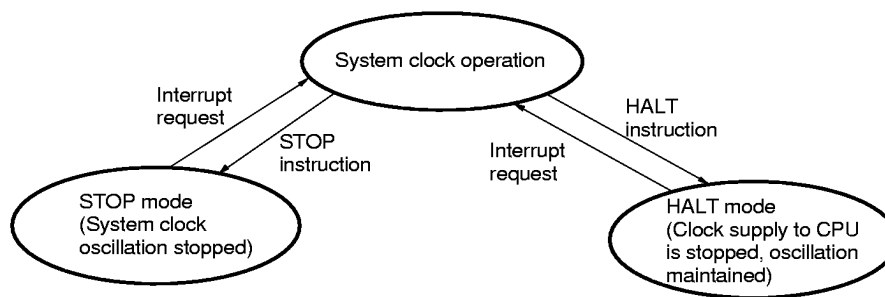
9. RESET FUNCTIONS

There are the following two reset methods.

• External reset by $\overline{\text{RESET}}$ pin
• Internal reset by watchdog timer runaway time detection

10. INSTRUCTION SET

(1) 8-bit instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

Second operand / First operand	#byte	A	r^Note	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL + byte] [HL + B] [HL + C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
B, C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL + byte] [HL + B] [HL + C]		MOV											
X													MULU
C													DIVUW

Note Except r = A

Preliminary Data Sheet

(2) 16-bit instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

Second operand / First operand	#word	AX	rp^Note	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW^Note						INCW, DECW PUSH, POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp = BC, DE or HL

(3) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

Second operand / First operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call instructions/branch instructions

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

Second operand / First operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic instruction	BR	CALL BR	CALLF	CALLT	BR, BC, BNC BZ, BNZ
Compound instruction					BT, BF BTCLR DBNZ

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

Preliminary Data Sheet　　　　　　　　　　　　　　　　　　　　**33**

★ ## 11. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T$_A$ = 25°C)

Parameter	Symbol	Test Conditions		Ratings	Unit
Supply voltage	V$_{DD}$			−0.3 to +6.5	V
	AV$_{DD}$			−0.3 to V$_{DD}$ + 0.3	V
	AV$_{REF}$			−0.3 to V$_{DD}$ + 0.3	V
	AV$_{SS}$			−0.3 to +0.3	V
Input voltage	V$_{I1}$	P00 to P03, P10 to P17, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75, X1, X2, XT1, XT2, $\overline{RESET}$		−0.3 to V$_{DD}$ + 0.3	V
	V$_{I2}$	P30 to P33	N-ch open-drain	−0.3 to V$_{DD}$ + 0.3	V
Output voltage	V$_O$			−0.3 to V$_{DD}$ + 0.3	V
Analog input voltage	V$_{AN}$	P10 to P17	Analog input pin	AV$_{SS}$ − 0.3 to AV$_{REF}$ + 0.3 and −0.3 to V$_{DD}$ + 0.3	V
High-level output current	I$_{OH}$	Per pin		−10	mA
		Total for P00 to P03, P40 to P47, P50 to P57, P64 to P67, P70 to P75		−15	mA
		Total for P20 to P25, P30 to P36		−15	mA
Low-level output current	I$_{OL}$ **Note**	Per pin for P00 to P03, P20 to P25, P34 to P36, P40 to P47, P64 to P67, P70 to P75	Peak value	20	mA
			Effective value	10	mA
		Per pin for P30 to P33, P50 to P57	Peak value	30	mA
			Effective value	15	mA
		Total for P00 to P03, P40 to P47, P64 to P67, P70 to P75	Peak value	50	mA
			Effective value	20	mA
		Total for P20 to P25	Peak value	20	mA
			Effective value	10	mA
		Total for P30 to P36	Peak value	100	mA
			Effective value	70	mA
		Total for P50 to P57	Peak value	100	mA
			Effective value	70	mA
Operating ambient temparature	T$_A$		Peak value	−40 to +85	°C
Storage temperature	T$_{stg}$		Effective value	−65 to +150	°C

Note The effective value should be calculated as follows: [Effective value] = [Peak value] × $\sqrt{duty}$
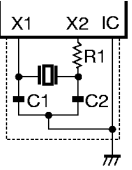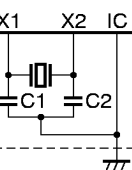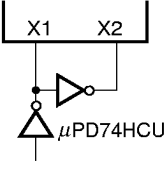
Caution **Product quality may suffer if the absolute maximum rating is exceeded for even single parameter or even momentarily. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions ensuring that the absolute maximum ratings are not exceeded.**

Capacitance (T$_A$ = 25°C, V$_{DD}$ = V$_{SS}$ = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C$_{IN}$	f = 1 MHz Unmeasured pins returned to 0 V.				15	pF
I/O capacitance	C$_{IO}$	f = 1 MHz Unmeasured pins returned to 0 V.	P00 to P03, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75			15	pF
			P30 to P33			20	pF

Remark Unless specified otherwise, alternate-function pin characteristics are the same as port pin characteristics.

Main System Clock Oscillation Circuit Characteristics (T$_A$ = –40 to 85°C, V$_{DD}$ = 1.8 to 5.5 V)
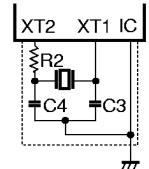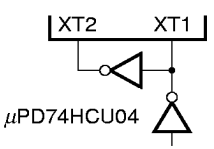
Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator	X1 X2 IC R1 C1 C2	Oscillation frequency (f$_x$)[Note 1]	V$_{DD}$ = 4.5 to 5.5 V	1.0		8.38	MHz
				1.0		5.0	
		Oscillation stabilization time[Note 2]	After V$_{DD}$ reaches oscillation voltage range MIN.			4	ms
Crystal resonator	X1 X2 IC C1 C2	Oscillation frequency (f$_x$)[Note 1]	V$_{DD}$ = 4.5 to 5.5 V	1.0		8.38	MHz
				1.0		5.0	
		Oscillation stabilization time[Note 2]	V$_{DD}$ = 4.5 to 5.5 V			10	ms
						30	
External clock	X1 X2 µPD74HCU04	X1 input frequency (f$_x$)[Note 1]	V$_{DD}$ = 4.5 to 5.5 V	1.0		8.38	MHz
						5.0	
		X1 input high-/low-level width (t$_{XH}$, t$_{XL}$)	V$_{DD}$ = 4.5 to 5.5 V	50		500	ns
				85		500	

Notes 1. Indicates only oscillation circuit characteristics. Refer to **AC Characteristics** for instruction execution time.
2. Time required to stabilize oscillation after reset or STOP mode release.

Cautions 1. When using the main system clock oscillator, wiring in the area enclosed with the broken line in the above figures should be carried out as follows to avoid an adverse effect from wiring capacitance.

• **Keep the wiring length as short as possible.**
• **Do not cross the wiring with the other signal lines.**
• **Do not route the wiring near a line through which a high fluctuating current flows.**
• **Always keep the ground point of the oscillator to the same potential as V$_{SS1}$.**
• **Do not ground the capacitor to a ground pattern in which a high current flows.**
• **Do not fetch signals from the oscillator.**

2. When the main system clock is stopped and the system is operated by the subsystem clock, the subsystem clock should be switched again to the main system clock after the oscillation stabilization time is secured by the program.

Subsystem Clock Oscillation Circuit Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator	XT2 XT1 IC R2 C4 C3	Oscillation frequency (f_{XT})[Note 1]		32	32.768	35	kHz
		Oscillation stabilization time[Note 2]	V_{DD} = 4.5 to 5.5 V		1.2	2	s
						10	
External clock	XT2 XT1 μPD74HCU04	XT1 input frequency (f_{XT})[Note 1]		32		100	kHz
		XT1 input high-/low-level width (t_{XTH}, t_{XTL})		5		15	μs

Notes 1. Indicates only oscillation circuit characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after V_{DD} reaches oscillation voltage MIN.

Cautions 1. **When using the subsystem clock oscillator, wiring in the area enclosed with the broken line in the above figures should be carried out as follows to avoid an adverse effect from wiring capacitance.**

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a line through which a high fluctuating current flows.**
- **Always keep the ground point of the oscillator to the same potential as V_{SS1}.**
- **Do not ground the capacitor to a ground pattern in which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. **The subsystem clock oscillator is a low-amplitude circuit in order to achieve a low consumption current, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.**

DC Characteristics (T$_A$ = −40 to +85°C, V$_{DD}$ = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V$_{IH1}$	P10 to P17, P21, P24, P35, P40 to P47, P50 to P57, P64 to P67, P74, P75	V$_{DD}$ = 2.7 to 5.5 V	0.7 V$_{DD}$		V$_{DD}$	V
				0.8 V$_{DD}$		V$_{DD}$	V
	V$_{IH2}$	P00 to P03, P20, P22, P23, P25, P34, P36, P70 to P73, $\overline{RESET}$	V$_{DD}$ = 2.7 to 5.5 V	0.8 V$_{DD}$		V$_{DD}$	V
				0.85 V$_{DD}$		V$_{DD}$	V
	V$_{IH3}$	P30 to P33 (N-ch open-drain)	V$_{DD}$ = 2.7 to 5.5 V	0.7 V$_{DD}$		5.5	V
				0.8 V$_{DD}$		5.5	V
	V$_{IH4}$	X1, X2	V$_{DD}$ = 2.7 to 5.5 V	V$_{DD}$ − 0.5		V$_{DD}$	V
				V$_{DD}$ − 0.2		V$_{DD}$	V
	V$_{IH5}$	XT1, XT2	V$_{DD}$ = 4.5 to 5.5 V	0.8 V$_{DD}$		V$_{DD}$	V
				0.9 V$_{DD}$		V$_{DD}$	V
Input voltage, low	V$_{IL1}$	P10 to P17, P21, P24, P35, P40 to P47, P50 to P57, P64 to P67, P74, P75	V$_{DD}$ = 2.7 to 5.5 V	0		0.3 V$_{DD}$	V
				0		0.2 V$_{DD}$	V
	V$_{IL2}$	P00 to P03, P20, P22, P23, P25, P34, P36, P70 to P73, $\overline{RESET}$	V$_{DD}$ = 2.7 to 5.5 V	0		0.2 V$_{DD}$	V
				0		0.15 V$_{DD}$	V
	V$_{IL3}$	P30 to P33	4.5 V ≤ V$_{DD}$ ≤ 5.5 V	0		0.3 V$_{DD}$	V
			2.7 V ≤ V$_{DD}$ < 4.5 V	0		0.2 V$_{DD}$	V
			1.8 V ≤ V$_{DD}$ < 2.7 V	0		0.1 V$_{DD}$	V
	V$_{IL4}$	X1, X2	V$_{DD}$ = 2.7 to 5.5 V	0		0.4	V
				0		0.2	V
	V$_{IL5}$	XT1, XT2	V$_{DD}$ = 4.5 to 5.5 V	0		0.2 V$_{DD}$	V
				0		0.1 V$_{DD}$	V
Output voltage, high	V$_{OH}$	V$_{DD}$ = 4.5 to 5.5 V, I$_{OH}$ = −1mA		V$_{DD}$ − 1.0		V$_{DD}$	V
		I$_{OH}$ = −100 μA		V$_{DD}$ − 0.5		V$_{DD}$	V
Output voltage, low	V$_{OL1}$	P30 to P33, P50 to P57	V$_{DD}$ = 4.5 to 5.5 V, I$_{OL}$ = 15 mA		0.4	2.0	V
		P00 to P03, P20 to P25, P34 to P36, P40 to P47, P64 to P67, P70 to P75	V$_{DD}$ = 4.5 to 5.5 V, I$_{OL}$ = 1.6 mA			0.4	V
	V$_{OL2}$	I$_{OL}$ = 400 μA				0.5	V

Remark Unless specified otherwise, alternate-function pin characteristics are the same as port pin characteristics.

DC Characteristics (T$_A$ = −40 to +85°C, V$_{DD}$ = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I$_{LIH1}$	V$_{IN}$ = V$_{DD}$	P00 to P03, P10 to P17, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P60 to P67, P70 to P75, $\overline{\text{RESET}}$			3	μA
	I$_{LIH2}$		X1, X2, XT1, XT2			20	μA
	I$_{LIH3}$	V$_{IN}$ = 5.5 V	P30 to P33			80	μA
Input leakage current, low	I$_{LIL1}$	V$_{IN}$ = 0 V	P00 to P03, P10 to P17, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75, $\overline{\text{RESET}}$			−3	μA
	I$_{LIL2}$		X1, X2, XT1, XT2			−20	μA
	I$_{LIL3}$		P30 to P33			−3[Note]	μA
Output leakage current, high	I$_{LOH}$	V$_{OUT}$ = V$_{DD}$				3	μA
Output leakage current, low	I$_{LOL}$	V$_{OUT}$ = 0 V				−3	μA
Mask option pull-up resistor	R$_1$	V$_{IN}$ = 0 V, P60 to P63 P30, P31		15	30	90	kΩ
Software pull-up resistor	R$_2$	V$_{IN}$ = 0 V, P00 to P03, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75		15	30	90	kΩ

Note When the pull-up resistor is not included in P30 and P31 (specified by a mask option), a −200 μA (MAX.) low-level input leakage current flows only at the 3-clock interval (no wait) when the read instruction to port 3 (P3) and port mode register 3 (PM3) is executed. At times other than this 3-clock interval, a −3 μA (MAX.) current flows.

Remark Unless specified otherwise, alternate-function pin characteristics are the same as port pin characteristics.

DC Characteristics (T_A = −40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Power supply current[Note 1]	I_{DD1}	8.38-MHz crystal oscillation operating mode	V_{DD} = 5.0 V ±10%		8	16	mA
	I_{DD2}	8.38-MHz crystal oscillation HALT mode	V_{DD} = 5.0 V ±10%		1.6	3.2	mA
	I_{DD3}	32.768-kHz crystal oscillation operating mode[Note 2]	V_{DD} = 5.0 V ±10%		60	120	μA
			V_{DD} = 3.0 V ±10%		32	64	μA
			V_{DD} = 2.0 V ±10%		24	48	μA
	I_{DD4}	32.768-kHz crystal oscillation HALT mode[Note 2]	V_{DD} = 5.0 V ±10%		25	55	μA
			V_{DD} = 3.0 V ±10%		5	15	μA
			V_{DD} = 2.0 V ±10%		2.5	12.5	μA
	I_{DD5}	XT1 = V_{DD} STOP mode. When feedback resistor is used	V_{DD} = 5.0 V ±10%		1	30	μA
			V_{DD} = 3.0 V ±10%		0.5	10	μA
			V_{DD} = 2.0 V ±10%		0.3	10	μA
	I_{DD6}	XT1 = V_{DD} STOP mode. When feedback resistor is not used	V_{DD} = 5.0 V ±10%		0.1	30	μA
			V_{DD} = 3.0 V ±10%		0.05	10	μA
			V_{DD} = 2.0 V ±10%		0.05	10	μA

Notes 1. Does not include the on-chip pull-up resistor, AV_{REF} current, and port current.
      2. When the main system clock is stopped.

AC Characteristics

(1) Basic Operation (T$_A$ = −40 to +85°C, V$_{DD}$ = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions			MIN.	TYP.	MAX.	Unit
Cycle time (Min. instruction execution time)	T$_{CY}$	Operating with main system clock	4.5 V ≤ V$_{DD}$ ≤ 5.5 V		0.24		32	μs
			2.7 V ≤ V$_{DD}$ < 4.5 V		0.8		32	μs
					1.6		32	μs
		Operating with subsystem clock			40[Note 1]	122	125	μs
TI00, TI01 input high-/low-level width	t$_{TIH0}$, t$_{TIL0}$	3.5 V ≤ V$_{DD}$ ≤ 5.5 V			2/f$_{sam}$ + 0.1[Note 2]			μs
		2.7 V ≤ V$_{DD}$ < 3.5 V			2/f$_{sam}$ + 0.2[Note 2]			μs
		1.8 V ≤ V$_{DD}$ < 2.7 V			2/f$_{sam}$ + 0.5[Note 2]			μs
TI50, TI51 input frequency	f$_{TI5}$	V$_{DD}$ = 2.7 to 5.5 V			0		4	MHz
					0		275	kHz
TI50, TI51 input high-/low-level width	t$_{TIH5}$, t$_{TIL5}$	V$_{DD}$ = 2.7 to 5.5 V			100			ns
					1.8			ns
Interrupt request input high-/low -level width	t$_{INTH}$, t$_{INTL}$	INTP0 to INTP3, P40 to P47		V$_{DD}$ = 2.7 to 5.5 V	1			μs
					2			μs
RESET low-level width	t$_{RSL}$	V$_{DD}$ = 2.7 to 5.5 V			10			μs
					20			μs

Notes 1. Value when using the external clock. When using a crystal resonator, the value becomes 114 μs (MIN.).

2. Selection of f$_{sam}$ = f$_X$, f$_X$/4, f$_X$/64 is available with bits 0 and 1 (PRM00, PRM01) of prescaler mode register 0 (PRM0). However, if the TI00 valid edge is selected as the count clock, the value becomes f$_{sam}$ = f$_X$/8.

T$_{CY}$ vs V$_{DD}$ (at main system clock operation)
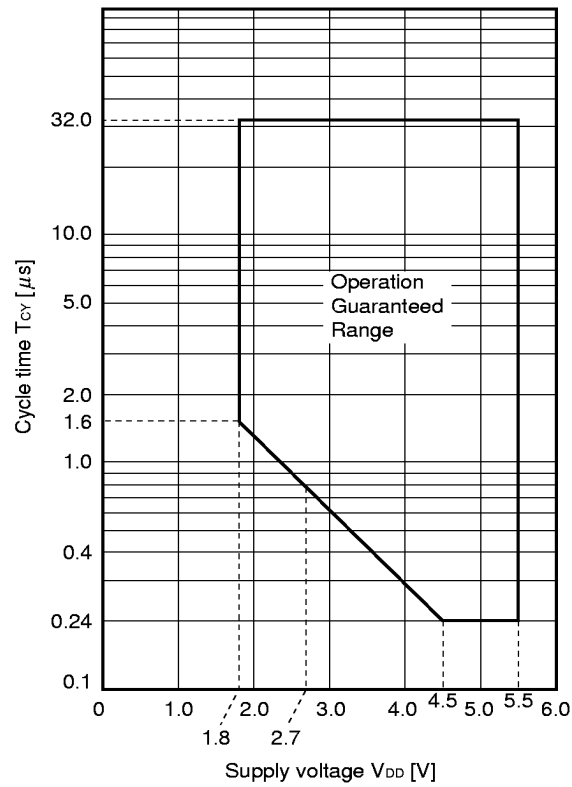
(2) **Read/Write Operation** (T$_A$ = −40 to + 85°C, V$_{DD}$ = 4.5 to 5.5 V) (1/3)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t$_{ASTH}$		0.5t$_{CY}$		ns
Address setup time	t$_{ADS}$		t$_{CY}$ − 40		ns
Address hold time	t$_{ADH}$		6		ns
Data input time from address	t$_{ADD1}$			(2 + 2n)t$_{CY}$ − 54	ns
	t$_{ADD2}$			(3 + 2n)t$_{CY}$ − 60	ns
Address output time from $\overline{RD}$↓	t$_{RDAD}$		0	100	ns
Data input time from $\overline{RD}$↓	t$_{RDD1}$			(2 + 2n)t$_{CY}$ − 87	ns
	t$_{RDD2}$			(3 + 2n)t$_{CY}$ − 93	ns
Read data hold time	t$_{RDH}$		0		ns
$\overline{RD}$ low-level width	t$_{RDL1}$		(1.5 + 2n)t$_{CY}$ − 33		ns
	t$_{RDL2}$		(2.5 + 2n)t$_{CY}$ − 33		ns
$\overline{WAIT}$↓ input time from $\overline{RD}$↓	t$_{RDWT1}$			0.5t$_{CY}$ − 43	ns
	t$_{RDWT2}$			t$_{CY}$ − 43	ns
$\overline{WAIT}$↓ input time from $\overline{WR}$↓	t$_{WRWT}$			0.5t$_{CY}$ − 25	ns
$\overline{WAIT}$ low-level width	t$_{WTL}$		(0.5 + 2n)t$_{CY}$ + 10	(2 + 2n)t$_{CY}$	ns
Write data setup time	t$_{WDS}$		60		ns
Write data hold time	t$_{WDH}$		6		ns
$\overline{WR}$ low-level width	t$_{WRL}$		(1.5 + 2n)t$_{CY}$ − 15		ns
$\overline{RD}$↓ delay time from ASTB↓	t$_{ASTRD}$		6		ns
$\overline{WR}$↓ delay time from ASTB↓	t$_{ASTWR}$		2t$_{CY}$ − 15		ns
ASTB↑ delay time from $\overline{RD}$↑ in external fetch	t$_{RDAST}$		0.8t$_{CY}$ − 15	1.2t$_{CY}$	ns
Address hold time from $\overline{RD}$↑ in external fetch	t$_{RDADH}$		0.8t$_{CY}$ − 15	1.2t$_{CY}$ + 30	ns
Write data output time from $\overline{RD}$↑	t$_{RDWD}$		40		ns
Write data output time from $\overline{WR}$↓	t$_{WRWD}$		10	60	ns
Address hold time from $\overline{WR}$↑	t$_{WRADH}$		0.8t$_{CY}$ − 15	1.2t$_{CY}$ + 30	ns
$\overline{RD}$↑ delay time from $\overline{WAIT}$↑	t$_{WTRD}$		0.8t$_{CY}$	2.5t$_{CY}$ + 25	ns
$\overline{WR}$↑ delay time from $\overline{WAIT}$↑	t$_{WTWR}$		0.8t$_{CY}$	2.5t$_{CY}$ + 25	ns

Remarks 1. t$_{CY}$ = T$_{CY}$/4

2. n indicates the number of waits.

Preliminary Data Sheet

(2) Read/Write Operation (T$_A$ = −40 to + 85°C, V$_{DD}$ = 2.7 to 4.5 V) (2/3)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t$_{ASTH}$		0.5t$_{CY}$		ns
Address setup time	t$_{ADS}$		0.5t$_{CY}$ − 54		ns
Address hold time	t$_{ADH}$		10		ns
Data input time from address	t$_{ADD1}$			(2 + 2n)t$_{CY}$ − 108	ns
	t$_{ADD2}$			(3 + 2n)t$_{CY}$ − 120	ns
Address output time from $\overline{RD}$↓	t$_{RDAD}$		0	200	ns
Data input time from $\overline{RD}$↓	t$_{RDD1}$			(2 + 2n)t$_{CY}$ − 148	ns
	t$_{RDD2}$			(3 + 2n)t$_{CY}$ − 162	ns
Read data hold time	t$_{RDH}$		0		ns
$\overline{RD}$ low-level width	t$_{RDL1}$		(1.5 + 2n)t$_{CY}$ − 40		ns
	t$_{RDL2}$		(2.5 + 2n)t$_{CY}$ − 40		ns
$\overline{WAIT}$↓ input time from $\overline{RD}$↓	t$_{RDWT1}$			0.5t$_{CY}$ − 60	ns
	t$_{RDWT2}$			t$_{CY}$ − 60	ns
$\overline{WAIT}$↓ input time from $\overline{WR}$↓	t$_{WRWT}$			0.5t$_{CY}$ − 50	ns
$\overline{WAIT}$ low-level width	t$_{WTL}$		(0.5 + 2n)t$_{CY}$ + 10	(2 + 2n)t$_{CY}$	ns
Write data setup time	t$_{WDS}$		60		ns
Write data hold time	t$_{WDH}$		10		ns
$\overline{WR}$ low-level width	t$_{WRL}$		(1.5 + 2n)t$_{CY}$ − 30		ns
$\overline{RD}$↓ delay time from ASTB↓	t$_{ASTRD}$		10		ns
$\overline{WR}$↓ delay time from ASTB↓	t$_{ASTWR}$		2t$_{CY}$ − 30		ns
ASTB↑ delay time from $\overline{RD}$↑ in external fetch	t$_{RDAST}$		0.8t$_{CY}$ − 30	1.2t$_{CY}$	ns
Address hold time from $\overline{RD}$↑ in external fetch	t$_{RDADH}$		0.8t$_{CY}$ − 30	1.2t$_{CY}$ + 60	ns
Write data output time from $\overline{RD}$↑	t$_{RDWD}$		40		ns
Write data output time from $\overline{WR}$↓	t$_{WRWD}$		20	120	ns
Address hold time from $\overline{WR}$↑	t$_{WRADH}$		0.8t$_{CY}$ − 30	1.2t$_{CY}$ + 60	ns
$\overline{RD}$↑ delay time from $\overline{WAIT}$↑	t$_{WTRD}$		0.5t$_{CY}$	2.5t$_{CY}$ + 50	ns
$\overline{WR}$↑ delay time from $\overline{WAIT}$↑	t$_{WTWR}$		0.5t$_{CY}$	2.5t$_{CY}$ + 50	ns

Remarks 1. t$_{CY}$ = T$_{CY}$/4

    2. n indicates the number of waits.

(2) Read/Write Operation (T$_A$ = −40 to + 85°C, V$_{DD}$ = 1.8 to 2.7 V) (3/3)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t$_{ASTH}$		0.5t$_{CY}$		ns
Address setup time	t$_{ADS}$		0.5t$_{CY}$ − 60		ns
Address hold time	t$_{ADH}$		20		ns
Data input time from address	t$_{ADD1}$			(2 + 2n)t$_{CY}$ − 233	ns
	t$_{ADD2}$			(3 + 2n)t$_{CY}$ − 240	ns
Address output time from $\overline{RD}$↓	t$_{RDAD}$		0	400	ns
Data input time from $\overline{RD}$↓	t$_{RDD1}$			(2 + 2n)t$_{CY}$ − 325	ns
	t$_{RDD2}$			(3 + 2n)t$_{CY}$ − 332	ns
Read data hold time	t$_{RDH}$		0		ns
$\overline{RD}$ low-level width	t$_{RDL1}$		(1.5 + 2n)t$_{CY}$ − 92		ns
	t$_{RDL2}$		(2.5 + 2n)t$_{CY}$ − 92		ns
$\overline{WAIT}$↓ input time from $\overline{RD}$↓	t$_{RDWT1}$			0.5t$_{CY}$ − 132	ns
	t$_{RDWT2}$			t$_{CY}$ − 132	ns
$\overline{WAIT}$↓ input time from $\overline{WR}$↓	t$_{WRWT}$			0.5t$_{CY}$ − 100	ns
$\overline{WAIT}$ low-level width	t$_{WTL}$		(0.5 + 2n)t$_{CY}$ + 10	(2 + 2n)t$_{CY}$	ns
Write data setup time	t$_{WDS}$		60		ns
Write data hold time	t$_{WDH}$		20		ns
$\overline{WR}$ low-level width	t$_{WRL}$		(1.5 + 2n)t$_{CY}$ − 60		ns
$\overline{RD}$↓ delay time from ASTB↓	t$_{ASTRD}$		20		ns
$\overline{WR}$↓ delay time from ASTB↓	t$_{ASTWR}$		2t$_{CY}$ − 60		ns
ASTB↑ delay time from $\overline{RD}$↑ in external fetch	t$_{RDAST}$		0.8t$_{CY}$ − 60	1.2t$_{CY}$	ns
Address hold time from $\overline{RD}$↑ in external fetch	t$_{RDADH}$		0.8t$_{CY}$ − 60	1.2t$_{CY}$ + 120	ns
Write data output time from $\overline{RD}$↑	t$_{RDWD}$		40		ns
Write data output time from $\overline{WR}$↓	t$_{WRWD}$		40	240	ns
Address hold time from $\overline{WR}$↑	t$_{WRADH}$		0.8t$_{CY}$ − 60	1.2t$_{CY}$ + 120	ns
$\overline{RD}$↑ delay time from $\overline{WAIT}$↑	t$_{WTRD}$		0.5t$_{CY}$	2.5t$_{CY}$ + 100	ns
$\overline{WR}$↑ delay time from $\overline{WAIT}$↑	t$_{WTWR}$		0.5t$_{CY}$	2.5t$_{CY}$ + 100	ns

Remarks 1. t$_{CY}$ = T$_{CY}$/4
     2. n indicates the number of waits.

Preliminary Data Sheet

(3) Serial Interface (T_A = −40 to +85°C, V_{DD} = 1.8 to 5.5 V)

(a) 3-wire serial I/O mode ($\overline{SCK30}$... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK30}$ cycle time	t_{KCY1}	4.5 V ≤ V_{DD} ≤ 5.5 V	954			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK30}$ high-/low-level width	t_{KH1}, t_{KL1}	V_{DD} = 4.5 to 5.5 V	$t_{KCY1}/2 − 50$			ns
			$t_{KCY1}/2 − 100$			ns
SI30 setup time (to $\overline{SCK30}$↑)	t_{SIK1}	4.5 V ≤ V_{DD} ≤ 5.5V	100			ns
		2.7 V ≤ V_{DD} < 4.5V	150			ns
			300			ns
SI30 hold time (from $\overline{SCK30}$↑)	t_{KSI1}		400			ns
SO30 output dealy time from $\overline{SCK30}$↓	t_{KSO1}	C = 100 pF[Note]			300	ns

Note C is the load capacitance of the $\overline{SCK30}$ and SO30 output lines.

(b) 3-wire serial I/O mode ($\overline{SCK30}$... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK30}$ cycle time	t_{KCY2}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.7 V ≤ V_{DD} < 4.5 V		1600			ns
				3200			ns
$\overline{SCK30}$ high-/low-level width	t_{KH2}, t_{KL2}	4.5 V ≤ V_{DD} ≤ 5.5 V		400			ns
		2.7 V ≤ V_{DD} < 4.5 V		800			ns
				1600			ns
SI30 setup time (to $\overline{SCK30}$↑)	t_{SIK2}			100			ns
SI30 hold time (from $\overline{SCK30}$↑)	t_{KSI2}			400			ns
SO30 output dealy time from SCK30↓	t_{KSO2}	C = 100 pF[Note]				300	ns
$\overline{SCK30}$ rise, fall time	t_{R2}, t_{F2}	When using external device expansion function				160	ns
		When not using external device expansion function	When using 16-bit timer output function			700	ns
			When not using 16-bit timer output function			1000	ns

Note C is the load capacitance of the SO30 output line.

(c) UART mode (Dedicated baud rate generator output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		4.5 V ≤ V$_{DD}$ ≤ 5.5 V			125000	bps
		2.7 V ≤ V$_{DD}$ < 4.5 V			78125	bps
					39063	bps

(d) UART mode (External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
ASCK0 cycle time	t$_{KCY3}$	4.5 V ≤ V$_{DD}$ ≤ 5.5 V	800			ns
		2.7 V ≤ V$_{DD}$ < 4.5 V	1600			ns
			3200			ns
ASCK0 high-/low-level width	t$_{KH3}$, t$_{KL3}$	4.5 V ≤ V$_{DD}$ ≤ 5.5 V	400			ns
		2.7 V ≤ V$_{DD}$ < 4.5 V	800			ns
			1600			ns
Transfer rate		4.5 V ≤ V$_{DD}$ ≤ 5.5 V			39063	bps
		2.7 V ≤ V$_{DD}$ < 4.5 V			19531	bps
					9766	bps
ASCK0 rise, fall time	t$_{R3}$, t$_{F3}$	V$_{DD}$ = 4.5 to 5.5 V, when not using external device expansion function			1000	ns
					160	ns

(e) UART mode (Infrared ray data transfer mode)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Transfer rate		V$_{DD}$ = 4.5 to 5.5 V		115200	bps
Bit rate allowable error		V$_{DD}$ = 4.5 to 5.5 V		±0.87	%
Output pulse width		V$_{DD}$ = 4.5 to 5.5 V	1.2	0.24/fbr[Note]	μs
Input pulse width		V$_{DD}$ = 4.5 to 5.5 V	4/fx		μs

Note fbr: Specified baud rate

(f) I²C bus Mode

Parameter		Symbol	Standard Mode		High-speed Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCL0 clock frequency		f_{CLK}	0	100	0	400	kHz
Bus free time (between stop and start condition)		t_{BUF}	4.7	—	1.3	—	μs
Hold time[Note 1]		$t_{HD:STA}$	4.0	—	0.6	—	μs
SCL0 clock low-level width		t_{LOW}	4.7	—	1.3	—	μs
SCL0 clock high-level width		t_{HIGH}	4.0	—	0.6	—	μs
Start/restart condition setup time		$t_{SU:STA}$	4.7	—	0.6	—	μs
Data hold time	CBUS compatible master	$t_{HD:DAT}$	5.0	—	—	—	μs
	I²C bus		0[Note 2]	—	0[Note 2]	0.9[Note 3]	μs
Data setup time		$t_{SU:DAT}$	250	—	100[Note 4]	—	ns
SDA0 and SCL0 signal rise time		t_R	—	1000	20 + 0.1Cb[Note 5]	300	ns
SDA0 and SCL0 signal fall time		t_F	—	300	20 + 0.1Cb[Note 5]	300	ns
Stop condition setup time		$t_{SU:STO}$	4.0	—	0.6	—	μs
Spike pulse width controlled by input filter		t_{SP}	—	—	0	50	ns
Capacitive load per each bus line		Cb	—	400	—	400	pF

Notes 1. On start condition, the first clock pulse is generated after hold period.

2. To fulfill undefined area of the SCL0 falling edge, it is necessary for the device to provide internally SDA0 signal (on $V_{IHmin.}$ of SCL0 signal) with at least 300 ns of hold time.

3. If the device does not extend the SCL0 signal low hold time (t_{LOW}), only maximum data hold time $t_{HD:DAT}$ needs to be fulfilled.

4. The high-speed mode I²C bus is available in the standard mode I²C bus system. At this time, the conditions described below must be satisfied.

• If the device does not extend the SCL0 signal low state hold time

$t_{SU:DAT} \geq$ 250 ns

• If the device extends the SCL0 signal low state hold time

Be sure to transmit the next data bit to the SDA0 line before the SCL0 line is released ($t_{Rmax.}$ + $t_{SU:DAT}$ = 1000 + 250 = 1250 ns by standard mode I²C bus specification).

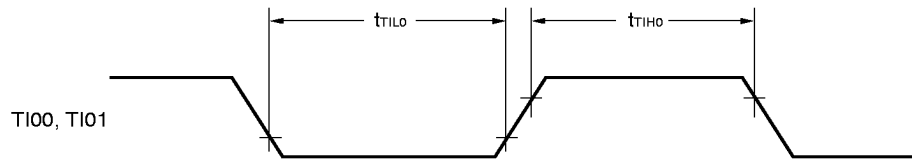**5.** Cb : total capacitance per one bus line (unit : pF)

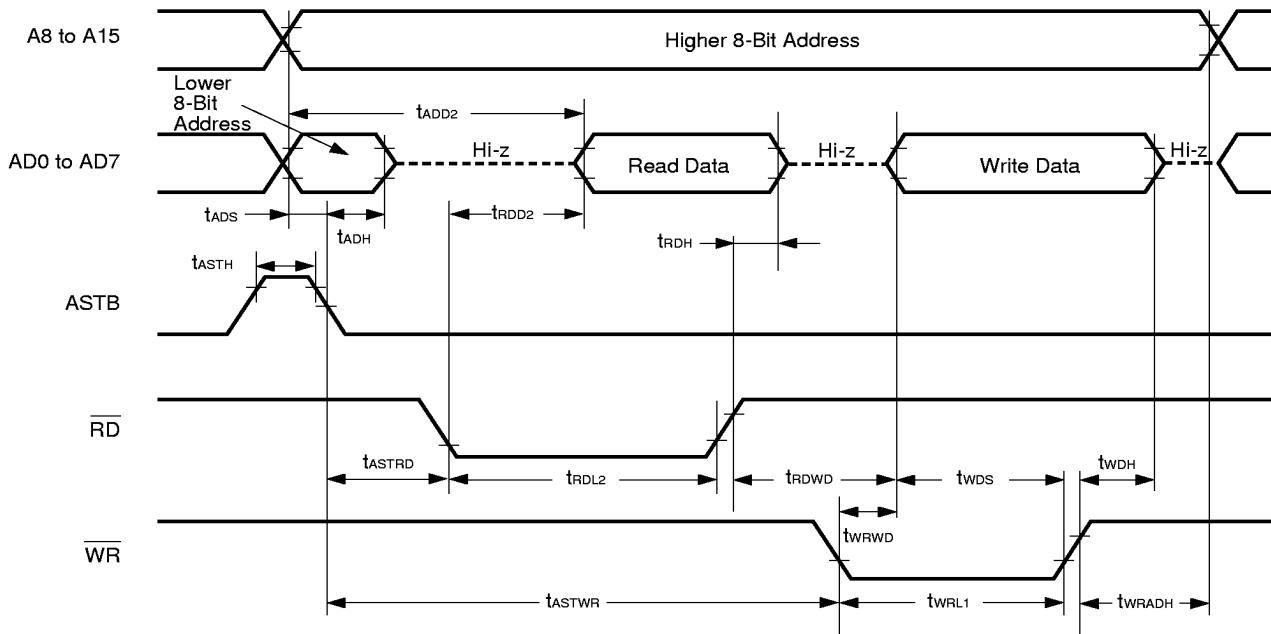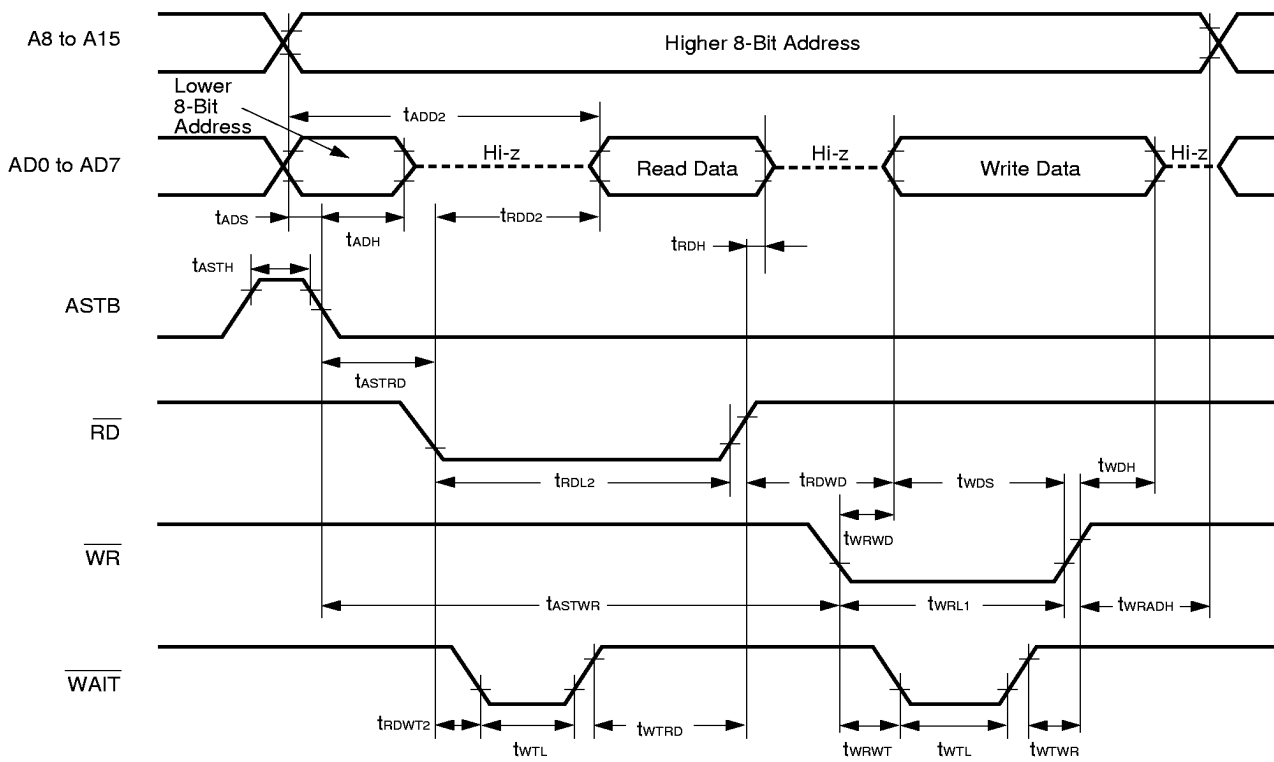**AC Timing Test Point (Excluding X1, XT1 Input)**

Clock Timing

TI Timing

Read/Write Operation

External Fetch (No Wait) :
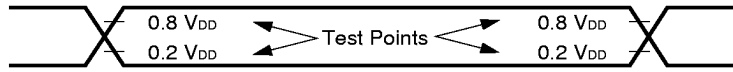
External Fetch (Wait Insertion) :
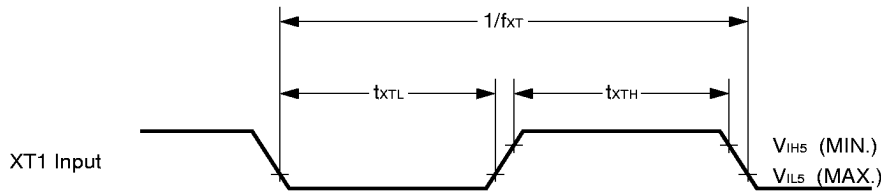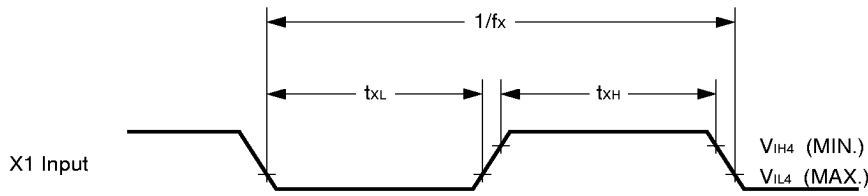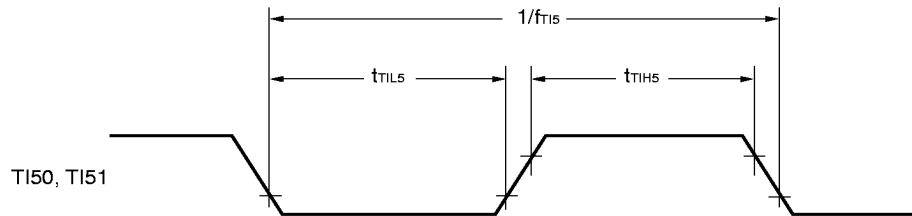
External Data Access (No Wait) :

External Data Access (Wait Insertion) :

Serial Transfer Timing

3-wire Serial I/O Mode :

m = 1, 2
n = 2
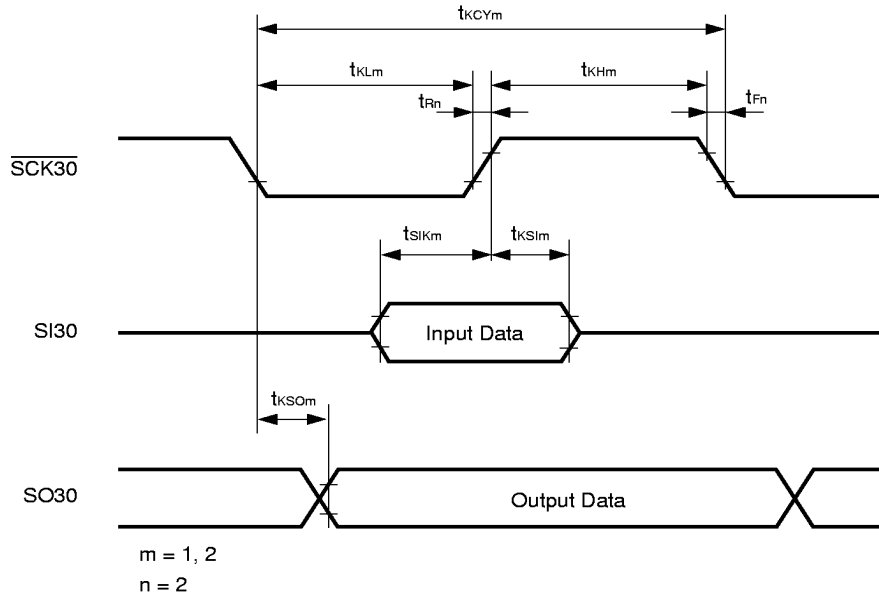
UART Mode (External Clock Input) :
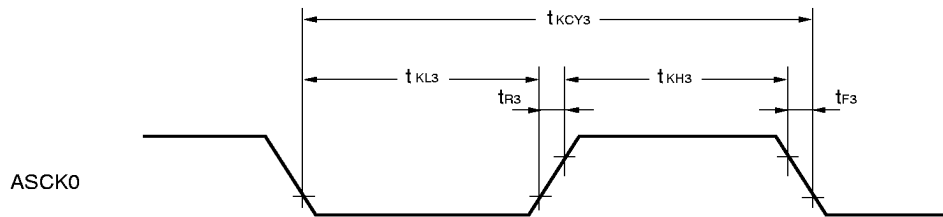
I²C Bus Mode
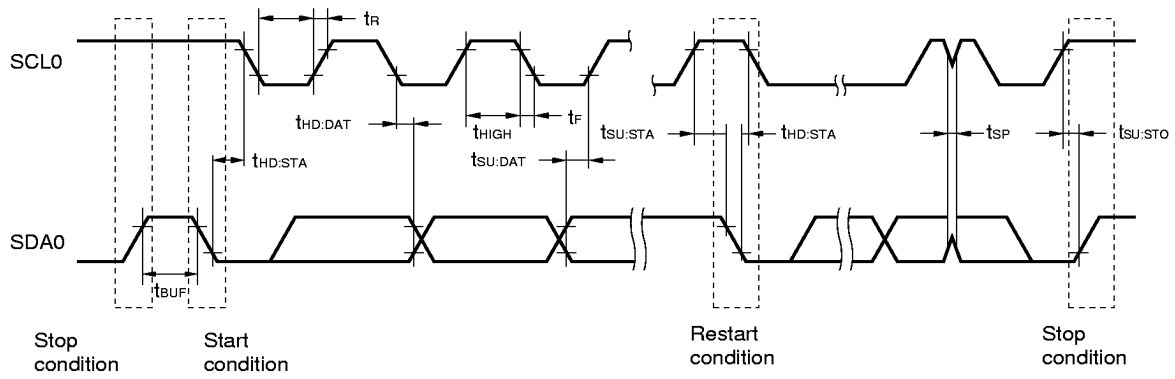
A/D Converter Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = AV_{REF} = 2.7 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	bit
Overall error[Note]		4.5 V ≤ AV_{REF} ≤ 5.5 V			±0.4	%
		2.7 V ≤ AV_{REF} < 4.5 V			±0.7	%
Conversion time	T_{CONV}	4.5 V ≤ AV_{REF} ≤ 5.5 V	14		200	μs
		2.7 V ≤ AV_{REF} < 4.5 V	20		200	μs
Analog input voltage	V_{IAN}		0		AV_{REF} + 0.3	V
Reference voltage	AV_{REF}		2.7		AV_{DD}	V
AV_{REF} resistance	R_{AIREF}		10	20		kΩ

Note Overall error excluding quantization error (±1/2 LSB). It is indicated as a ratio to the full-scale value.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

| Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		1.6		5.5	V
Data retention power supply current	I_{DDDR}	V_{DDDR} = 1.6 V Subsystem clock stop and feed-back resistor disconnected		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabiliza-tion wait time	t_{WAIT}	Release by $\overline{\text{RESET}}$		2^{17}/fx		ms
		Release by interrupt request		**Note**		ms

Note Selection of 2^{12}/fx and 2^{14}/fx to 2^{17}/fx is possible with bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS).

Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)
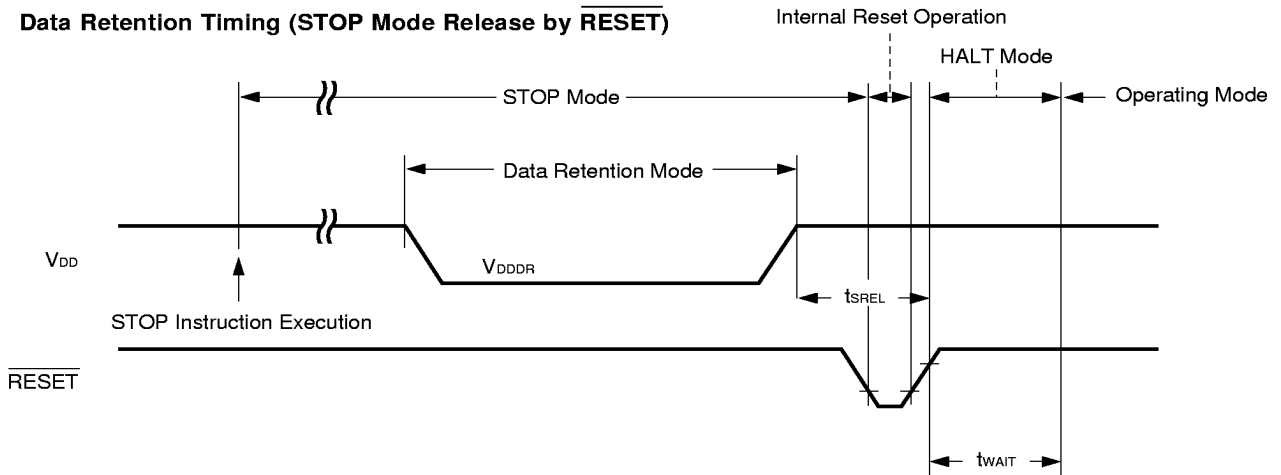
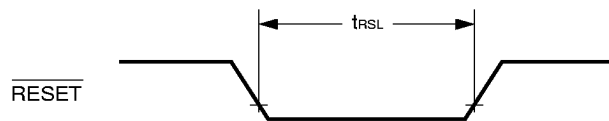**Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Request Signal)**
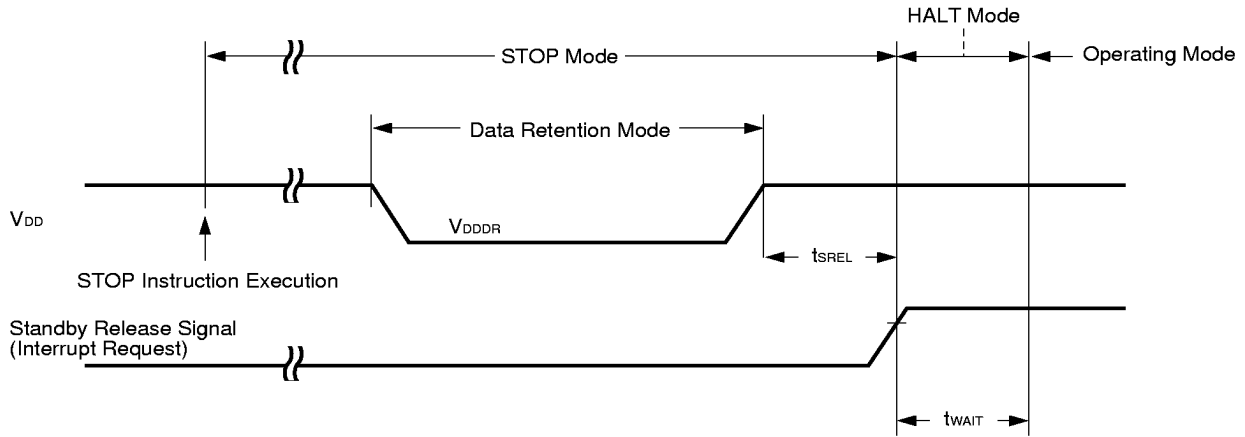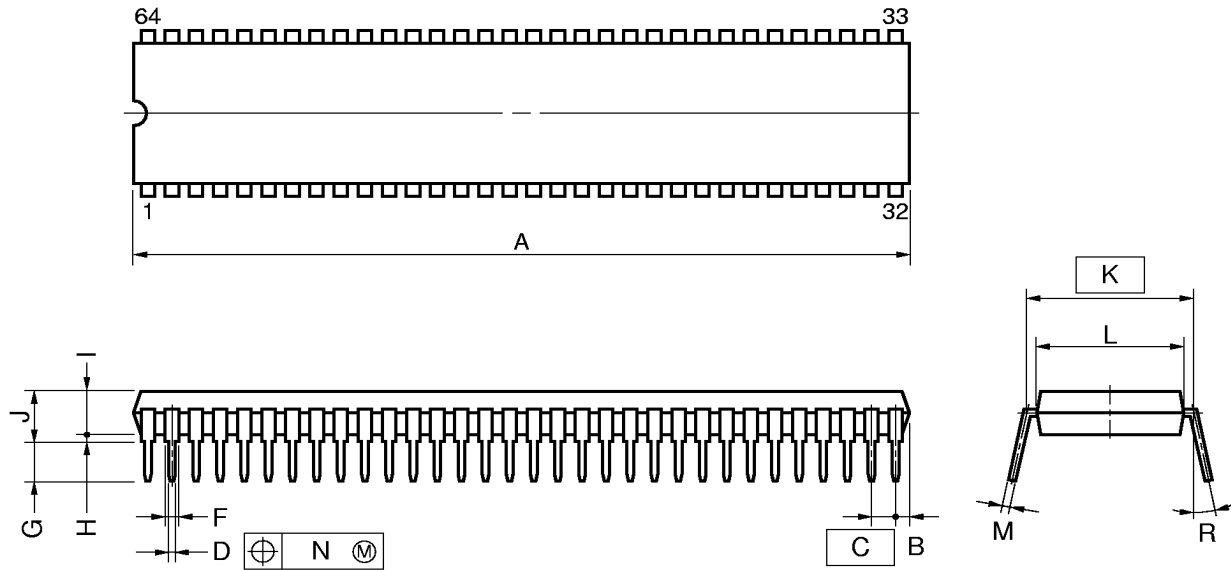

Interrupt Request Input Timing
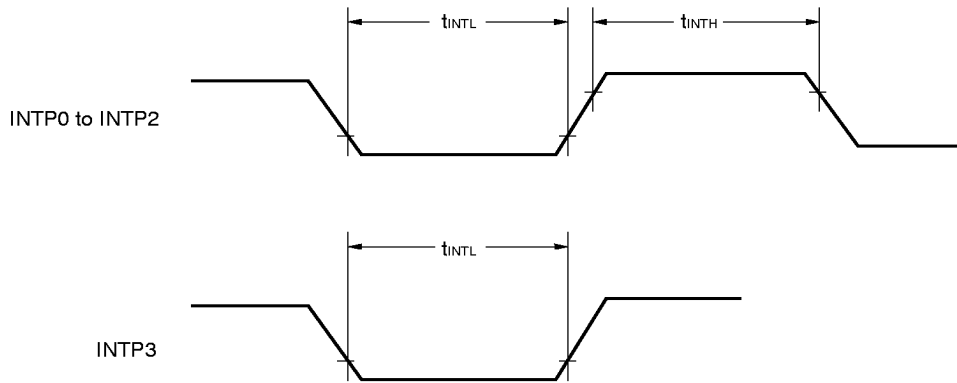
$\overline{\text{RESET}}$ **Input Timing**

12. PACKAGE DRAWINGS
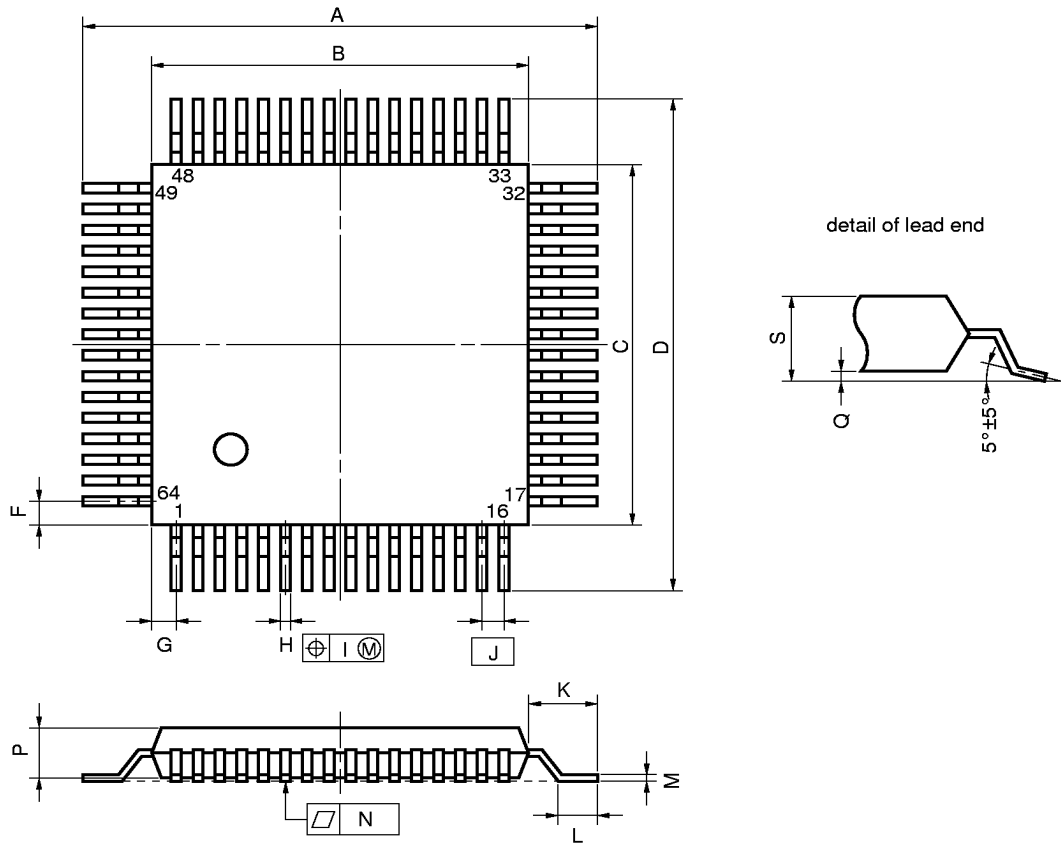
64-PIN PLASTIC SHRINK DIP (750 mils)

NOTE

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50±0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

P64C-70-750A,C-1

64-PIN PLASTIC QFP (14 × 14)

detail of lead end

5°±5°

P64GC-80-AB8-3

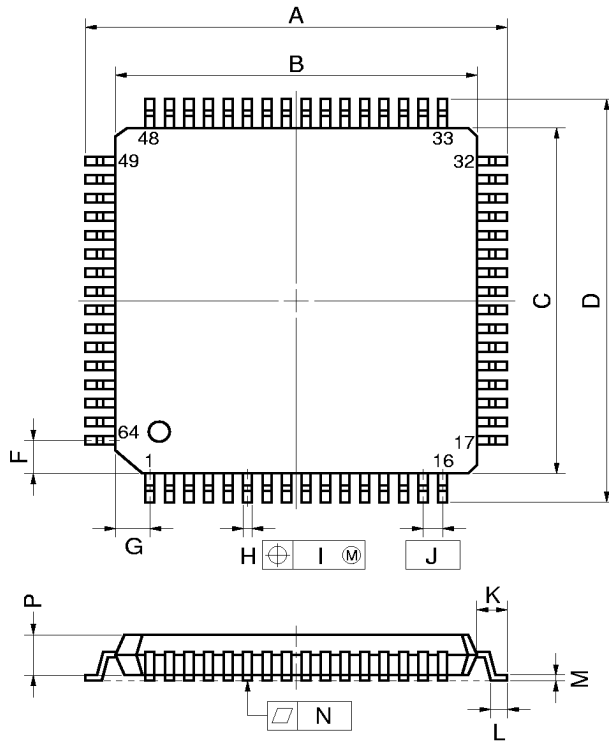**NOTE**

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

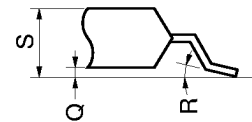| ITEM	MILLIMETERS	INCHES
A	17.6±0.4	0.693±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.55	0.100
Q	0.1±0.1	0.004±0.004
S	2.85 MAX.	0.112 MAX.

64-PIN PLASTIC LQFP (12 × 12)

detail of lead end

NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	14.8±0.4	0.583±0.016
B	12.0±0.2	$0.472^{+0.009}_{-0.008}$
C	12.0±0.2	$0.472^{+0.009}_{-0.008}$
D	14.8±0.4	0.583±0.016
F	1.125	0.044
G	1.125	0.044
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.4±0.2	0.055±0.008
L	0.6±0.2	$0.024^{+0.008}_{-0.009}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	1.4	0.055
Q	0.125±0.075	0.005±0.003
R	5°±5°	5°±5°
S	1.7 MAX.	0.067 MAX.

P64GK-65-8A8-1

Preliminary Data Sheet

57

★ **APPENDIX A. DEVELOPMENT TOOLS**

The following development tools are available for system development using the µPD780034Y Subseries.
Also refer to **(5) Cautions on using development tools.**

(1) Language Processing Software

RA78K/0	Assembler package common to 78K/0 Series
CC78K/0	C compiler package common to 78K/0 Series
DF780034	Device file for µPD780034 Subseries
CC78K/0-L	C compiler library source file common to 78K/0 Series

(2) Flash Memory Writing Tools

Flashpro II (FL-PR2)	Flash programmer dedicated to on-chip flash memory microcontroller
FA-64CW FA-64GC FA-64GK**Note**	Adapter for flash memory writing

    Note   Under development

(3) Debugging Tool
    • When using in-circuit emulator IE-78K0-NS

IE-78K0-NS**Note**	In-circuit emulator common to 78K/0 Series
IE-70000-MC-PS-B	Power supply unit for IE-78K0-NS
IE-70000-98-IF-C**Note**	Interface adapter when using PC-9800 series as host machine (excluding notebook PCs)
IE-70000-CD-IF**Note**	PC card and interface cable when using notebook PC of PC-9800 series as host machine
IE-70000-PC-IF-C**Note**	Interface adapter when using IBM PC/AT™ or compatible as host machine
IE-780034-NS-EM1 **Note**	Emulation board common to µPD780034 Subseries
NP-64CW	Emulation probe for 64-pin plastic shrink DIP (CW type)
NP-64GC	Emulation probe for 64-pin plastic QFP (GC-AB8 type)
NP-64GK**Note**	Emulation probe for 64-pin plastic LQFP (GC-8A8 type)
TGK-064SBW	Conversion adapter for connecting target system board designed to mount a 64-pin plastic LQFP (GK-8A8 type) and NP-64GK
EV-9200GC-64	Socket to be mounted on target system board manufactured for 64-pin plastic QFP (GC-AB8 type)
ID78K0-NS**Note**	Integrated debugger for IE-78K0-NS
SM78K0	System simulator common to 78K/0 Series
DF780034	Device file common to µPD780034 Subseries

    Note   Under development

• **When using in-circuit emulator IE-78001-R-A**

IE-78001-R-A[Note]	In-circuit emulator common to 78K/0 Series
IE-70000-98-IF-B IE-70000-98-IF-C[Note]	Interface adapter when using PC-9800 series as host machine (excluding notebook PCs)
IE-70000-PC-IF-B IE-70000-PC-IF-C[Note]	Interface adapter when using IBM PC/AT or compatible as host machine
IE-78000-R-SV3	Interface adapter and cable when using EWS as host machine
IE-780034-NS-EM1[Note]	Emulation board common to μPD780034 Subseries
IE-78K0-R-EX1[Note]	Emulation probe conversion board necessary to use IE-780034-NS-EM1 on IE-78001-R-A
EP-78240CW-R	Emulation probe for 64-pin plastic shrink DIP (CW type)
EP-78240GC-R	Emulation probe for 64-pin plastic QFP (GC-AB8 type)
EP-78012GK-R	Emulation probe for 64-pin plastic LQFP (GK-8A8 type)
TGK-064SBW	Conversion adapter for connecting target system board designed to mount a 64-pin plastic LQFP　(GK-8A8) and EP-78012GK-R.
EV-9200GC-64	Socket to be mounted on target system board manufactured for 64-pin plastic QFP (GC-AB8 type)
ID78K0	Integrated debugger for IE-78001-R-A
SM78K0	System simulator common to 78K/0 Series
DF780034	Device file common to μPD780034 Subseries

Note   Under development

(4) Real-time OS

RX78K/0	Real-time OS for 78K/0 Series
MX78K0	OS for 78K/0 Series

(5) Cautions on using development tools

- The ID-78K0-NS, ID78K0, and SM78K0 are used in combinaiton with the DF780034.
- The CC78K/0 and RX78K/0 are used in combination with the RA78K/0 and the DF780034.
- The Flashpro II, FA-64CW, FA-64GC, FA64GK, NP-64CW, NP-64GC, and NP-64GK are products made by Naitou Densei Machidaseisakusho (044-822-3813).
  Contact an NEC distributor when purchasing of these products.
- The TGK-064SBW is a product made by TOKYO ELETECH CORPORATION.
  Refer to: Daimaru Kogyo, Ltd.
  Tokyo Electronic Components Division (03-3820-7112)
  Osaka Electronic Components Division (06-244-6672)
- For third party development tools, see the **78K/0 Series Selection Guide (U11126E)**.
- The host machines and OSs supporting each software are as follows.

Host Machine [OS] / Software	PC — PC-9800 series [Windows™] IBM PC/AT or compatible [Japanese/English Windows]	EWS — HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™] NEWS™ (RISC) [NEWS-OS™]
RA78K/0	√ Note	√
CC78K/0	√ Note	√
ID78K0-NS	√	—
ID78K0	√	√
SM78K0	√	—
RX78K/0	√ Note	√
MX78K0	√ Note	√

Note DOS-based software

★   ## APPENDIX B. RELATED DOCUMENTS

Device Related Documents

Document Name	Document No. (English)	Document No. (Japanese)
μPD780024, 780024Y, 780034, 780034Y Subseries User's Manual	U12022E	U12022J
μPD780031Y, 780032Y, 780033Y, 780034Y Data Sheet	This document	U12166J
μPD78F0034Y Data Sheet	U11994E	U11994J
78K/0 Series User's Manual — Instructions	U12326E	U12326J
78K/0 Series Instruction Table	—	U10903J
78K/0 Series Instruction Set	—	U10904J
μPD780034Y Subseries Special Function Register Table	—	To be prepared

Development Tool Documents (User's Manual)

Document Name		Document No. (English)	Document No. (Japanese)
RA78K0 Assembler Package	Operation	U11802E	U11802J
	Assembly Language	U11801E	U11801J
	Structured Assembly Language	U11789E	U11789J
RA78K Series Structured Assembler Preprocessor		EEU-1402	U12323J
CC78K0 C Compiler	Operation	U11517E	U11517J
	Language	U11518E	U11518J
CC78K/0 C Compiler Application Note	Programming Know-how	EEA-1208	EEA-618
CC78K Series Library Source File		—	U12322J
IE-78K0-NS		To be prepared	To be prepared
IE-78001-R-A		To be prepared	To be prepared
IE-780034-NS-EM1		To be prepared	To be prepared
EP-78240		U10332E	EEU-986
EP-78012GK-R		EEU-1538	EEU-5012
SM78K0 System Simulator — Windows based	Reference	U10181E	U10181J
SM78K Series System Simulator	External Part User Open Interface Specifications	U10092E	U10092J
ID78K0-NS Integrated Debugger	Reference	To be prepared	U12900J
ID78K0 Integrated Debugger, EWS based	Reference	—	U11151J
ID78K0 Integrated Debugger, PC based	Reference	U11539E	U11539J
ID78K0 Integrated Debugger, Windows based	Guide	U11649E	U11649J

Caution   The above related documents are subject to change without notice. Be sure to read the latest documents before designing.

Embedded Software Documents (User's Manual)

Document Name		Document No. (English)	Document No. (Japanese)
78K/0 Series Real-time OS	Basics	U11537E	U11537J
	Installation	U11536E	U11536J
78K/0 Series OS MX78K0	Basics	U12257E	U12257J

Other Documents

Document Name	Document No. (English)	Document No. (Japanese)
IC Package Manual	C10943X	
Semiconductor Device Mounting Technology Manual	C10535E	C10535J
Quality Grades on NEC Semiconductor Devices	C11531E	C11531J
NEC Semiconductor Device Reliability/Quality Control System	C10983E	C10983J
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E	C11892J
Guide to Quality Assurance for Semiconductor Devices	MEI-1202	—
Microcomputer Product Series Guide	—	U11416J

Caution The above related documents are subject to change without notice. Be sure to read the latest documents before designing.