MV1821

VIDEO CASSETTE RECORDER PDC AND VPS INTERFACE CIRCUIT

(Supersedes version in April 1994 Consumer IC Handbook, HB3120–2.0)

The MV1821 is a member of the Enhanced Video Automation (EVA) family for receiving Programme Delivery Control (PDC) messages broadcast in World System Teletext (WST) format two Broadcast Service Data Packets (BSDP). It will also receive Video Programme System (VPS) data from TV line 16 in Manchester bi–phase format. The data from either service can be read via the I²C bus connections in a standard format (see page 7). Additional data is appended to include new PDC features and differentiate between data sources.

It is intended for use in Video Cassette Recorders to provide automatic recording of suitably tabelled Television programmes requested by the user.

FEATURES

- Fully automatic PDC/VPS switching
- Full error checking of both data formats
- Low external component count
- I²C Bus for low cost Interfacing
- I²C Bus and $\overline{DAV}$ released during power down
- Low frequency 6·9375MHz oscillator
- Full decoding of Hamming data (PDC)
- Supports 'fast mode' I²C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	–0·3V to +7·0V
All inputs	–0·3 to V_{DD}+0·3V
Operating temperature	–10°C to +75°C
Storage temperature	–65°C to +150°C

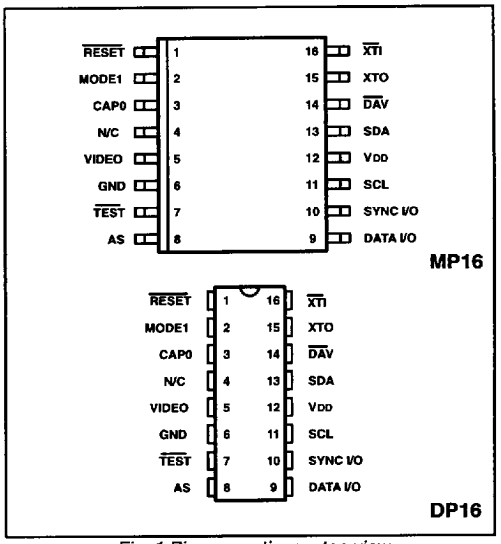


Fig. 1 Pin connections – top view

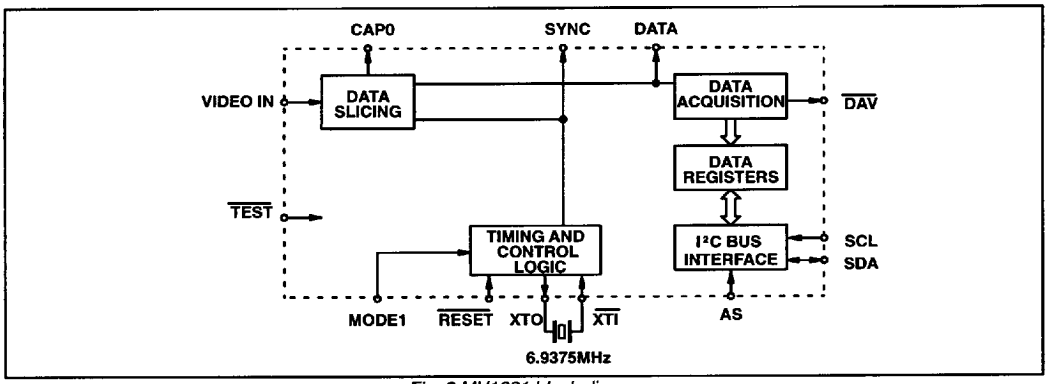


Fig. 2 MV1821 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
T_{amb} = −10 to +75°C, V_{DD} = 5V ±10%

Characteristics	Pin	Min	Typ	Max	Units	Conditions
Supply voltage	12	4·5	5·0	5·5	V	
Supply Current	12		20		mA	
Video Input	5					
Voltage amplitude		0·7	1·0	2·0	Vpp	Bottom of sync to white (pk to pk)
Source impedance				250	Ω	220nF input capacitor
CAP0	3					
Capacitor value			220		nF	Connected to GND
Capacitor tolerance		−10%		+10%		
Effective series resistance				5	Ω	1MHz
DATA & SYNC OUTPUTS	9 & 10					
Output voltage High		$0·8V_{DD}$	$0·95V_{DD}$		V	I_{OH} = −2·0mA
Output voltage Low			0·1	0·4	V	I_{OL} = 2·0mA
MODE1 & AS	2 & 8					75k (nom) pull–down resistor
Input voltage Low		0		$0·2V_{DD}$	V	
Input voltage High		$0·8V_{DD}$		V_{DD}	V	
Input current Low		−10		+10	µA	$V_{IN} = V_{SS}$
Input current High		18	67	275	µA	$V_{IN} = V_{DD}$
$\overline{\text{XTI}}$ input	16					1M (nom) resistor to XTO
Input voltage Low		0		$0·2V_{DD}$	V	
Input voltage High		$0·8V_{DD}$		V_{DD}	V	
Input current Low		−0·5	−5·0	−20	µA	$-0·3 < V_{IN} < V_{IL}$ max
Input current High		0·5	1.5	20	µA	V_{IH} min $< V_{IN} < (V_{DD} + 0·3)$
XTO output	15					
Output voltage High		$0·8V_{DD}$	$0·9V_{DD}$		V	I_{OH} = −0·1mA
Output voltage Low			0·1	0·4	V	I_{OL} = 0·1mA
Frequency			6·9375		MHz	±100ppm
I^2C bus						
SCL, SDA Schmitt inputs	11, 13					
Input voltage Low		0		1·5	V	
Input voltage High		3·0		V_{DD}	V	
Output voltage Low (SDA only)			0·1	0·6	V	I_{OL} = 6·0mA
SCL Clock Frequency	11		400	775	kHz	
Hysteresis voltage		0·2	0·4		V	
$\overline{\text{DAV}}$ Data available	14					
Output voltage Low			0·1	0·4	V	I_{OL} = 2·0mA

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
T_{amb} = −10 to +75°C, V_{DD} = 5V ±10%

Characteristics	Pin	Min	Typ	Max	Units	Conditions
RESET Schmitt Input	1					75k (nom) pull–up resistor
Threshold voltage falling		1·4	2·0		V	
Threshold voltage rising			3·0	3·8	V	
Hysteresis Voltage		0·6	1·0		V	
Input current Low		−18	−67	−275	µA	$V_{IN} = V_{SS}$
Input current High		−10		+10	µA	$V_{IN} = V_{DD}$

Table 1

Pins	Test	Test Levels	Notes
SDA & SCL	Human body model	1kV on 100pF through 1k5Ω	< 15% LTPD
SDA & SCL	Machine model	100V on 200pF through 0Ω & <500nH	
All others	Human body model	4kV on 100pF through 1k5Ω	Meets Mil. Std. 883D class 3 requirements
All others	Machine model	400V on 200pF through 0Ω & <500nH	

LTPD=Lot Tolerant Percent Defective

Table 2 ESD data

PIN DESCRIPTION

Symbol	Pin No	Pin Name and Description
$\overline{\text{RESET}}$	1	Active low reset. Includes a 75kΩ pull–up resistor
MODE1	2	When low or not connected, both PDC and VPS data are received automatically. When high during reset positive going edge VPS ONLY mode is forced. The pin must be returned low after reset for proper operation. Includes a 75kΩ pull–down resistor. (See †)
CAP0	3	Capacitor zero. Storage for reference voltage.
N/C	4	No connection.
VIDEO	5	Input for composite video signal with negative going syncs.
GND	6	Ground 0 volts.
$\overline{\text{TEST}}$	7	Test pin, for factory use only, leave open circuit or connected to V_{DD}.
AS	8	Address select for I^2C bus, 0010 0001 if set high, or 0010 0011 if set low.
DATA	9	Data output
SYNC	10	Sync output
SCL	11	I^2C bus serial clock input
V_{DD}	12	Positive supply voltage +5V
SDA	13	I^2C bus bi–directional data port
$\overline{\text{DAV}}$	14	Active low open drain output data available signal to microprocessor
XTO	15	Crystal out, 6·9375MHz fundamental crystal with on–chip 1MΩ resistor to $\overline{\text{XTI}}$
$\overline{\text{XTI}}$	16	Crystal input

CRYSTAL SPECIFICATION

Parallel resonant fundamental frequency 6·9375000MHz. AT cut.

Tolerance at –10°C to 60°C	±50ppm
Tolerance overall	±100ppm
Nominal load capacitance	30pF
Equivalent series resistance	<20Ω

FUNCTIONAL DESCRIPTION

The video signal is sliced to produce data and synchronising signals. Timing circuits monitor the sync signal to enable the MV1821 to lock to the broadcast signal. A timing window, for the Vertical Blanking Interval (VBI) lines 6–22 and 318–335, is established to enable the acquisition circuit to monitor the sliced data signal for valid teletext or VPS line 16 data.

PDC reception

The framing code is checked for valid World System Teletext (WST) data. Magazine, packet and designation code bytes are checked and valid Broadcast Service Data Packets (BSDP) format two type only are accepted. These are also known as packet 8/30. Format two is signalled by byte six, data bit two being set high and bits 3 and 4 set low. Bytes 13 to 25 inclusive are Hamming decoded (8, 4) and stored in seven registers each of eight bits. If the complete message is received with no uncorrectable Hamming errors, an interrupt to the microprocessor is signalled by setting the $\overline{DAV}$ pin low. At the same time the data is transferred to a second bank of registers, provided there is no I²C bus activity at the time, reorganised with original numbered bytes 14, 15, 24, 25 and 13 placed after byte 23, to read out on the I²C bus when so requested. See page 7.

VPS reception

The VPS data consists of 15 eight bit words encoded in Manchester bi–phase format with a data rate of 2.5Mbits/sec. It is only transmitted in TV line 16, so similar data on other TV lines is excluded. A data low to high transition indicates a binary zero and a high to low transition indicates a binary one. Word 1 acts as a clock run (10/10/10/10/10/10/10/10) to synchronise the decoder. Word 2 is a start code (10/00/10/10/10/01/10/01) to verify the required data. Note, the second element 00 contains a deliberate violation of the Manchester bi–phase format which is only permitted in word 2. Words 5, 11, 12, 13, 14 and 15 are Manchester bi–phase decoded and if verified are stored in the input registers. When all the message is correctly received, an interrupt to the microprocessor is signalled by the $\overline{DAV}$ pin going low. At the same time the data is transferred to a second bank of registers, provided there is no I²C bus activity at the time, reorganised into the word sequence11, 12, 13, 14, 5, 15, followed by 11111110, to be read out on the I²C bus when requested, see page 7.

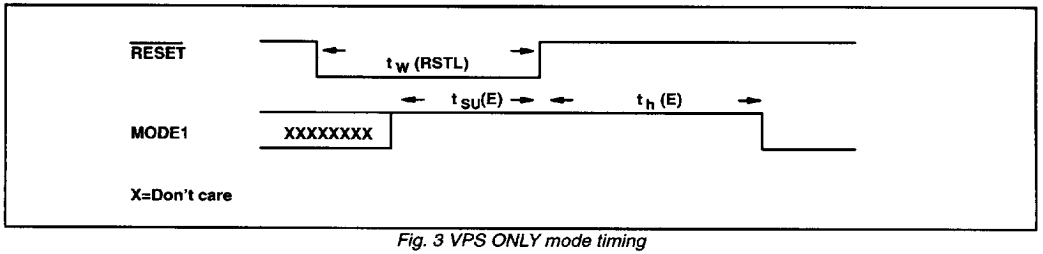


Fig. 3 VPS ONLY mode timing

PARAMETER		FROM POWER UP			FROM RESET		
		MIN	NOM	MAX	MIN	NOM	MAX
t_w(RSTL)	Pulse duration $\overline{RESET}$ low	300ms			150ns		
t_{su}(E)	MODE1 set–up time before $\overline{RESET}$ high	150ns			150ns		
t_h(E)	MODE1 hold time after $\overline{RESET}$ high	150ns			150ns		

† VPS ONLY mode

In an area where VPS is the only form of Programme Delivery Control then because of the algorithm employed by MV1821 when searching for the presence of either packet 8/30 format 2 or VPS in the broadcast signal, a delay of approximately 2·5 seconds would occur at power–up, reset and whenever a channel change occurred. This mode alleviates this problem in VPS only areas.

To force the MV1821 into VPS ONLY mode the following events must occur:

At power–up/reset the $\overline{RESET}$ pin must be low and the MODE1 pin must be high, the reset pin is then taken high after which the MODE1 pin is taken low. (see Fig. 3).

The ideal way of generating the timing shown in Fig.3 is under microcontroller or microprocessor control using output pins or some from of decoder e.g. 74HCT138.

In order to return to AUTO PDC/VPS mode it is only necessary to perform a reset with MODE1 held low.

I²C bus interface

The MV1821 is configured as an I²C bus slave transmitter with a selectable address. The I²C bus address is 0010 0001 (20+1 hex) with the address select (AS) pin set high, or 0010 0011(22+1 hex) with the AS pin set low. The read bit (LSB) must be set, it is not possible to write to the MV1821.

On recognising its address, the MV1821 will send an acknowledge, and then transmit on the SDA line the first byte from the output registers most significant bit (MSB) first. It will then monitor the SDA line for an acknowledge from the microprocessor. If the microprocessor does NOT send an acknowledge, the MV1821 will release the data line to allow the microprocessor to send a stop condition and the output registers are all set high. If the microprocessor does send an acknowledge, the following bytes of the message will be output provided each byte is acknowledged. The final data will be either, PDC byte 13 followed by1111, or 1111110 for VPS messages, see page 7. The last bit of the message serves to indicate the source of data: 1=PDC, 0=VPS.

When readout is complete, the $\overline{DAV}$ pin is reset high and the output registers are all set high. If the microprocessor continues to send clocks on the SCL line, the MV1821 will output FF bytes on the SDA line. Also, if the MV1821 is re–addressed before another PDC message is received, the MV1821 will output FF bytes on the SDA line. The microprocessor can prematurely stop the message by NOT sending an acknowledge followed optionally by a STOP condition after any byte has been sent by the MV1821. The registers will then be reset to FF and the $\overline{DAV}$ pin will be reset high. Also, if after a partial readout, the microprocessor sends a repeat START condition followed by the MV1821 I²C bus address, the registers will be reset to FF, $\overline{DAV}$ pin will be reset high and the MV1821 will output FF bytes on the SDA line.

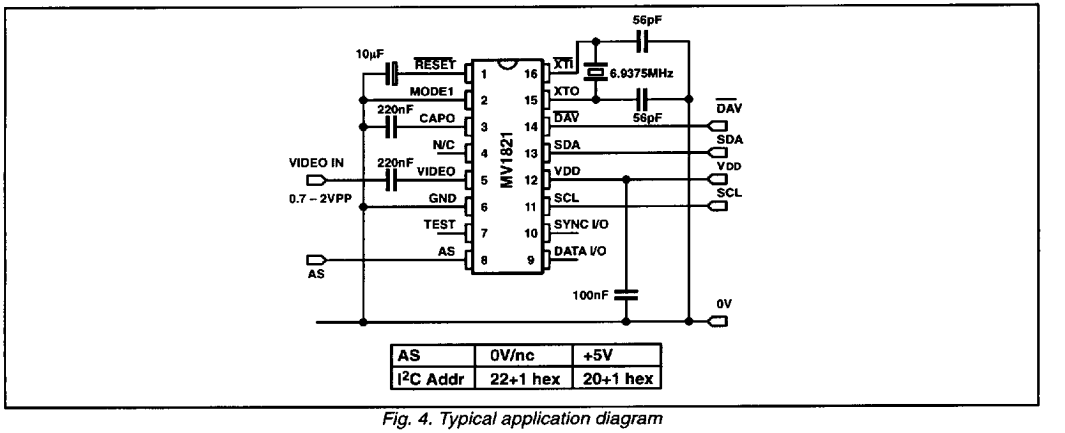
To prevent any corruption of the data in the output registers during I²C bus activity, valid PDC or VPS messages are held in the incoming registers until I²C bus activity ceases. Here they may be over written by new PDC or VPS messages until the I²C bus activity ceases and they can be transferred to the output registers. In the absence of I²C bus reads, subsequent valid messages will continue to be transferred to the output registers over–writing any existing data. In this way the output registers always contain the latest PDC or VPS message.

General information

PDC data transmitted via Teletext packets 8–30 Format 2, will take precedence over VPS data. A 64 state frame counter is reset by every valid PDC packet, which will inhibit VPS reception until the counter reaches maximum. This will ensure that if receiving both signals on a given transmission, the PDC data will dominate, but if it does at any time cease to be received, the VPS data will be enabled within 2.56 seconds of the last PDC packet. This allows for one pkt. 8–30 to be missed without changing to VPS operation. See Fig. 6.

The system clock is provided by an on chip 6·9375MHz oscillator together with an external parallel resonant fundamental frequency AT cut crystal.

Following a reset ($\overline{RESET}$ pulled low), the output I²C bus registers will contain FF bytes and the $\overline{DAV}$ pin will be set high. When the MV1821 is powered down, the I²C bus will be released so that it can be used by other devices.



AS	0V/nc	+5V
I²C Addr	22+1 hex	20+1 hex

Fig. 4. Typical application diagram

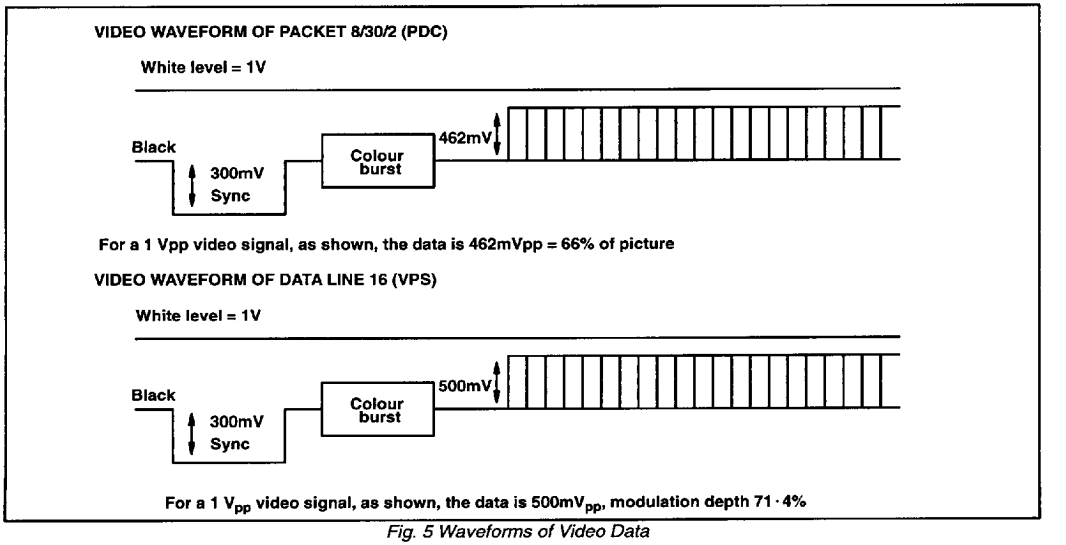


Fig. 5 Waveforms of Video Data

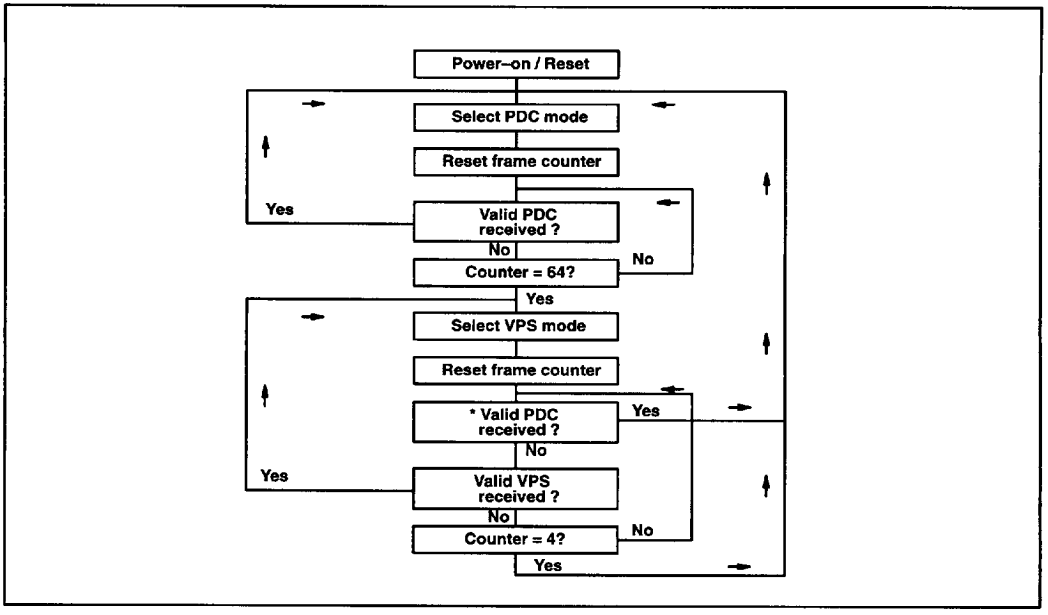


Fig. 6 Flow chart of VPS/PDC Switching

* The operation of the MV1821, in the presence of both Line 16 (VPS) and packet 8/30/2, follows the guidelines of the EBU Code of practice, SPB459 Revision2, February 1992, page 49:

"–When both Line 16 (VPS) and teletext delivered labels are available simultaneously, decoders should default to the teletext delivered service."

The counter is incremented once / frame

One line = 64µs One frame = 625 lines

PDC timeout count =	64 frames =	625 x 64µs x 64 =	2·56s
VPS timeout count =	4 frames =	625 x 64µs x 4 =	160ms

ORDERING INFORMATION

MV1821/KG/DPAS
MV1821/KG/MPES
MV1821/KG/MPEE (Tape and Reel)

ORDER OF DATA OUTPUT ON THE I²C BUS

BIT ORDER		PDC DATA		BIT VALUE		VPS data
byte 1	bit 7	byte 16	bit 0 – CNI b9	———	reserved	byte 11
	bit 6		bit 1 – CNI b10	64	Network (or programme provider)	
	bit 5		bit 2 – PIL b1	16		
	bit 4		bit 3 – PIL b2	8		
	bit 3	byte 17	bit 0 – PIL b3	4	Day	
	bit 2		bit 1 – PIL b4	2		
	bit 1		bit 2 – PIL b5	1		
	bit 0		bit 3 – PIL b6	8		
byte 2	bit 7	byte 18	bit 0 – PIL b7	4		byte 12
	bit 6		bit 1 – PIL b8	2	Month	
	bit 5		bit 2 – PIL b9	1		
	bit 4		bit 3 – PIL b10	16		
	bit 3	byte 19	bit 0 – PIL b11	8		
	bit 2		bit 1 – PIL b12	4	Hour	
	bit 1		bit 2 – PIL b13	2		
	bit 0		bit 3 – PIL b14	1		
byte 3	bit 7	byte 20	bit 0 – PIL b15	32		byte 13
	bit 6		bit 1 – PIL b16	16		
	bit 5		bit 2 – PIL b17	8		
	bit 4		bit 3 – PIL b18	4	Minute	
	bit 3	byte 21	bit 0 – PIL b19	2		
	bit 2		bit 1 – PIL b20	1		
	bit 1		bit 2 – CNI b5	8		
	bit 0		bit 3 – CNI b6	4		
byte 4	bit 7	byte 22	bit 0 – CNI b7	2	Country	byte 14
	bit 6		bit 1 – CNI b8	1		
	bit 5		bit 2 – CNI b11	32		
	bit 4		bit 3 – CNI b12	16		
	bit 3	byte 23	bit 0 – CNI b13	8	Network (or programme provider)	
	bit 2		bit 1 – CNI b14	4		
	bit 1		bit 2 – CNI b15	2		
	bit 0		bit 3 – CNI b16	1		
byte 5	bit 7	byte 14	bit 0 – PCS b1	2	Status (define the analog sound	byte 5
	bit 6		bit 1 – PCS b2	1	transmission system)	
	bit 5		bit 2 – MI	1	Mode Indicator	
	bit 4		bit 3 – unallocated			
	bit 3	byte 15	bit 0 – CNI b1	128		
	bit 2		bit 1 – CNI b2	64		
	bit 1		bit 2 – CNI b3	32	Country	
	bit 0		bit 3 – CNI b4	16		
byte 6	bit 7	byte 24	bit 0 – PTY b1	128		byte 15
	bit 6		bit 1 – PTY b2	64		
	bit 5		bit 2 – PTY b3	32		
	bit 4		bit 3 – PTY b4	16	Programme Type	
	bit 3	byte 25	bit 0 – PTY b5	8		
	bit 2		bit 1 – PTY b6	4		
	bit 1		bit 2 – PTY b7	2		
	bit 0		bit 3 – PTY b8	1		
byte 7	bit 7	byte 13	bit 0 – LC1 b1	2	Label Channel Identifier	– set to 1
	bit 6		bit 1 – LC1 b2	1	interleave up to four PIL messages	– set to 1
	bit 5		bit 2 – LUF	1	Label Update Flag	– set to 1
	bit 4		bit 3 – PRF	1	Prepare to Record Flag	– set to 1
	bit 3		– set to 1			– set to 1
	bit 2		– set to 1		NOTE. Data is output on the I²C bus MSB first	– set to 1
	bit 1		– set to 1			– set to 1
	bit 0		– set to 1			– set to 0