T-46-23-12

MHS

MATRA M H S

January 1991

HI-REL DATA SHEET

HM 65764

8 k x 8
HIGH SPEED CMOS SRAM

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FEATURES

- FAST ACCESS TIME : 25*/35/45/55 ns
- LOW POWER CONSUMPTION
  ACTIVE : 380 mW (typ)
  STANDBY : 110 mW (typ)
- WIDE TEMPERATURE RANGE :
  - 55°C TO 125°C

* Preliminary

- 300 AND 600 MILS WIDTH PACKAGE
- TTL COMPATIBLE INPUTS AND OUTPUTS
- ASYNCHRONOUS
- CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE
- SINGLE 5 VOLT SUPPLY

DESCRIPTION

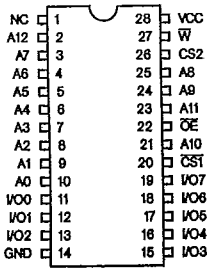
The HM 65764 is a high speed CMOS static RAM organized as 8192 x 8 bits. It is manufactured using MHS high performance CMOS technology.
Access times as fast as 25 ns are available with maximum power consumption of only 550 mW.
The HM 65764 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 73 % when the circuit is deselected.

Easy memory expansion is provided by active low chip select ($\overline{CS1}$), an active high chip select (CS2), an active low output enable ($\overline{OE}$) and three state drivers.
All inputs and outputs of the HM 65764 are TTL compatible and operate from single 5 V supply thus simplifying system design.
The HM 65764 is 100 % processed following the test methods of MIL STD 883C and/or ESA/SCC 9000, making it ideally suitable for military/space applications that demand superior levels of performance and reliability.

PACKAGES

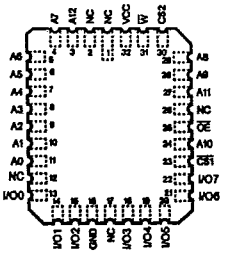
Ceramic 300 mils, 600 mils, 22 pins, DIL.

Pinout DIL 28 pins (top view)

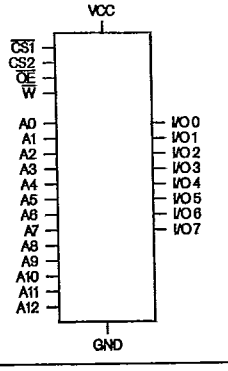


LCC, 32 pins.

Pinout LCC 32 pins (top view)



LOGIC SYMBOL



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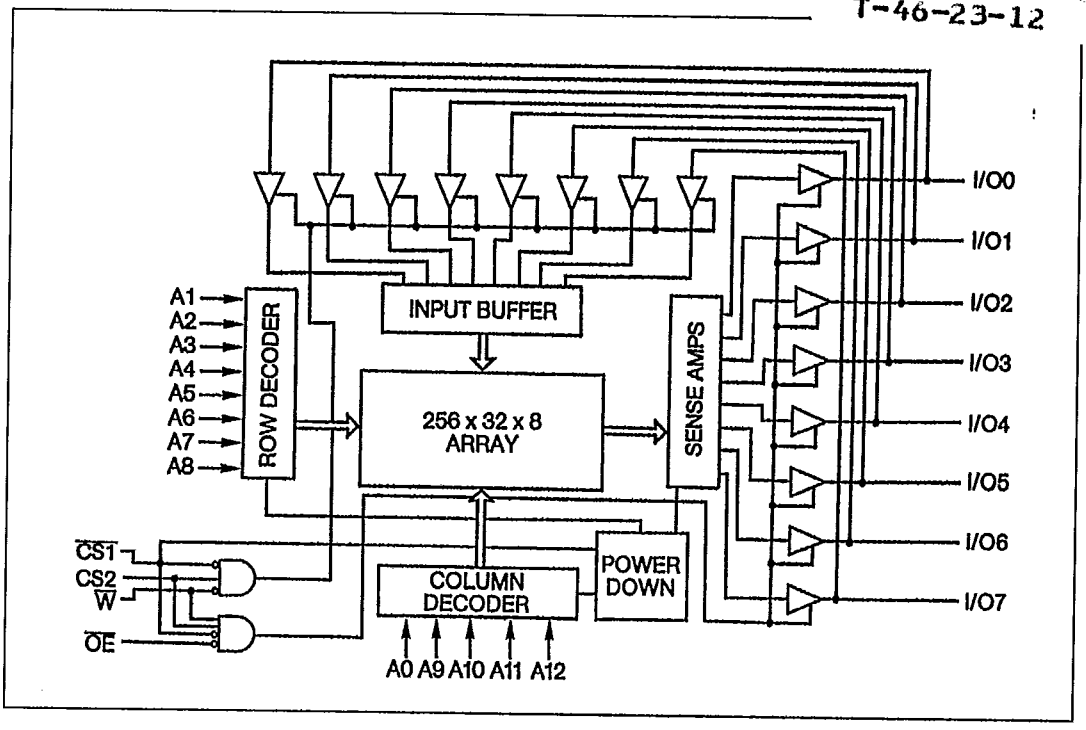
BLOCK DIAGRAM



PIN NAMES

A0-A13	: Address inputs	$\overline{CS1}$	: Chip Select 1
I/00-I/07	: Inputs/Outputs	CS2	: Chip Select 2
VCC	: Power	$\overline{OE}$	: Output enable
GND	: Ground	$\overline{W}$	: Write enable

TRUTH TABLE

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{W}$	DATA-IN	DATA-OUT	MODE
H	X	X	X	Z	Z	Deselect
L	H	L	H	Z	Valid	Read
L	H	X	L	Valid	Z	Write
L	H	H	H	Z	Z	Output disable

L = low, H = high, X = H or L, Z = high impedance.

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : - 0.5 V to + 7.0 V
DC input voltage : - 3.0 V to 7.0 V
DC output voltage in high Z state : - 0.5 V to + 7.0 V
Storage temperature : - 65°C to + 150°C

Output current into outputs (low) : 20 mA
Electro static discharge voltage : >2000 V (MIL STD 883C method 3015)

OPERATING RANGE	OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	5 V ± 10 %	- 55°C to + 125°C
Industrial	5 V ± 10 %	- 40°C to + 85°C

ELECTRICAL CHARACTERISTICS

DC PARAMETERS : MIL STD 883C FOR GROUP A (Subgroups 1, 2, 3, 4)

Parameter	Description	65764 H	65764 k	65764 M	65764 N	Unit	Value	Note 6
ICCSB (1)	Standby supply current	20	20	20	20	mA	Max	M
ICCSB (1a)	Standby supply current	40	30	30	30	mA	Max	M
ICCOP (2)	Operating supply current	125	125	125	125	mA	Max	M
IIX (3)	Input leakage current	+ / - 10	+ / - 10	+ / - 10	+ / - 10	µA	Max	M
IOZ (3)	Output leakage current	+ / - 10	+ / - 10	+ / - 10	+ / - 10	µA	Max	M
VIL (4)	Input low voltage	0.8	0.8	0.8	0.8	V	Max	T
VIH (4)	Input high voltage	2.2	2.2	2.2	2.2	V	Min	T
VOL (5)	Output low voltage	0.4	0.4	0.4	0.4	V	Max	M
VOH (5)	Output high voltage	2.4	2.4	2.4	2.4	V	Min	M
C IN	Input capacitance	5	5	5	5	pF	Max	G
C OUT	Output capacitance	7	7	7	7	pF	Max	G

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Notes : 1. $\overline{CS1}$ > = Vcc - 0.3V, Vin > = Vcc - 0,3V
1a. CS1 ≥ VIH Max Vcc, Min Duty cycle = 100 %
2. Vcc max, Output current = 0 mA, Minimum cycle
3. Vcc max, Vin = Gnd to Vcc
4. VIL min = - 3.0V VIH max = Vcc
5. Vcc min, IOL = 8 mA, IOH = - 1 mA
6. Including open/short test or inputs clamp voltage.
G - Guaranted - Not tested : Parameter measured at design validation and at any design change.
M - Measured : Parameter measured and data-log capability.
T - Tested : Parameter verification during testing.

AC TEST LOADS WAVEFORMS

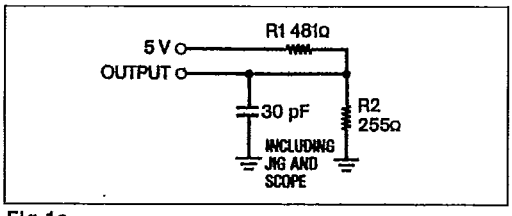


Fig.1a.

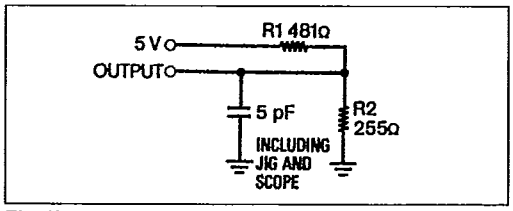
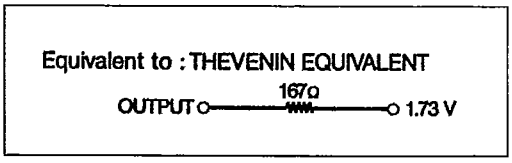


Fig.1b



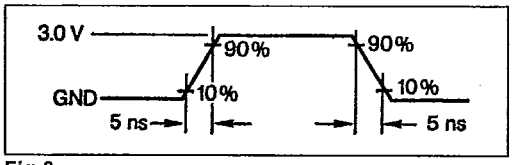


Fig.2

AC PARAMETERS : MIL STD 883C FOR GROUP A (SUBGROUPS 7, 8, 9, 10, 11)

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Conditions
- VCC 5V ± 10 %
- Input pulse levels Gnd to 3.ov
- Input rise 5 ns
- Input timing reference levels 1.5V
- Output loading IOL / IOH + 30 pF
- Operating temperature - 55°C to + 125°C

WRITE CYCLE

SYMBOL	PARAMETER (8)	65764 H	65764 K	65764 M	65764 N	UNIT	VALUE
TAVAV	Write cycle time	20	25	40	50	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to end of write	20	25	30	40	ns	min
TDVWH	Data set-up time	10	15	15	25	ns	min
TEL1WH	$\overline{CS1}$ low to write end	20	25	30	40	ns	min
TEH2WH	CS2 high to write end	20	20	25	30	ns	min
TWLQZ (7)	Write low to high Z	7	15	15	20	ns	max
TWLWH	Write pulse width	20	20	20	25	ns	min
TWHAX	Address hold to end of write	0	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	0	ns	min
TWHQX	Write high to low Z	5	5	5	5	ns	min

Notes : 7. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
8. All parameters tested only.
All parameters are screened during full speed functional test.
For subgroups 7 and 8 (functional test).
Tested at 1 MHz with VIL = OV and VIH = 3V.
HM 65764 is verified with differents patterns unit for basic function, latch-up, maximum rating, data-retention.

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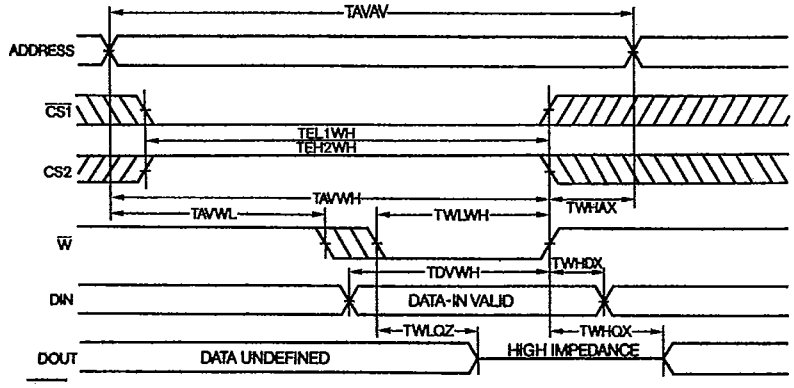
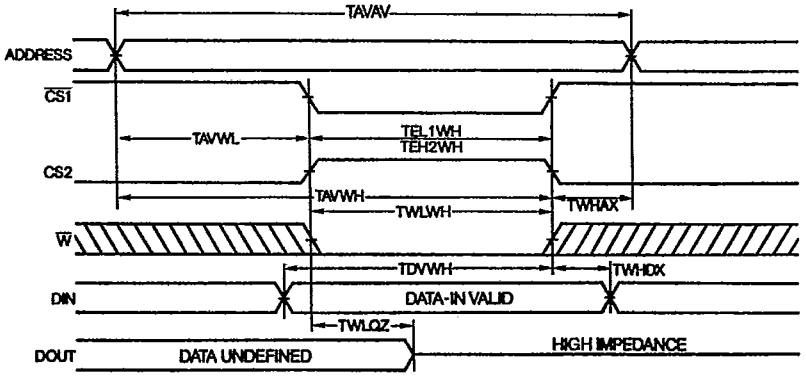
WRITE CYCLE 1 $\overline{W}$ CONTROLLED (note 9)



WRITE CYCLE 2 $\overline{CS1}$ CONTROLLED (note 9)



Note : 9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write. Data out is HIGH impedance if $\overline{OE}$ = VIH.

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READ CYCLE :

SYMBOL	PARAMETER (8)	65764 H	65764 K	65764 M	65764 N	UNIT	VALUE
TAVAV	Read cycle time	25	35	45	55	ns	min
TAVQV	Address access time	25	35	45	55	ns	max
TAVQX	Address valid to low Z	3	3	3	3	ns	min
TEL1QV	Chip-select 1 access time	25	35	45	55	ns	max
TEH2QV	Chip-select 2 access time	25	25	30	40	ns	max
TEL1QX	$\overline{CS1}$ low to low Z	5	5	5	5	ns	min
TEH2QX	CS2 high to high Z	3	3	3	3	ns	min
TEH1QZ (11)	$\overline{CS1}$ high to high Z	10	15	15	20	ns	max
TEL2QZ (11)	CS2 high to high Z	10	15	15	20	ns	max
TEL1IC	$\overline{CS1}$ low to power up	0	0	0	0	ns	min
TEH1ICCL	CS1 high to power down	20	20	25	25	ns	max
TGLQV	Output enable access time	12	15	20	25	ns	max
TGLQX	$\overline{OE}$ low to low Z	3	3	3	3	ns	min
TGHQZ	$\overline{OE}$ high to high Z	10	12	15	20	ns	min

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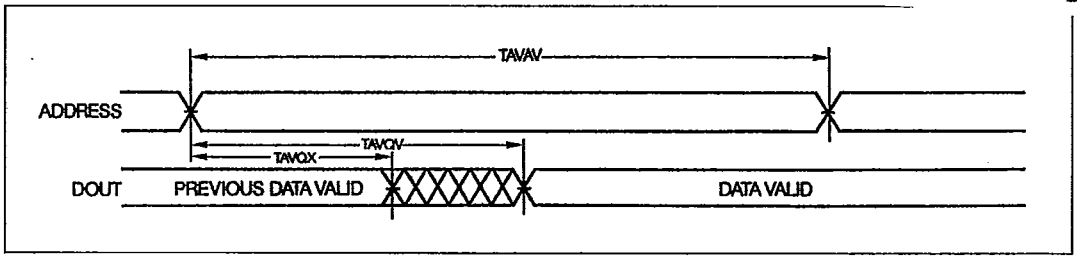
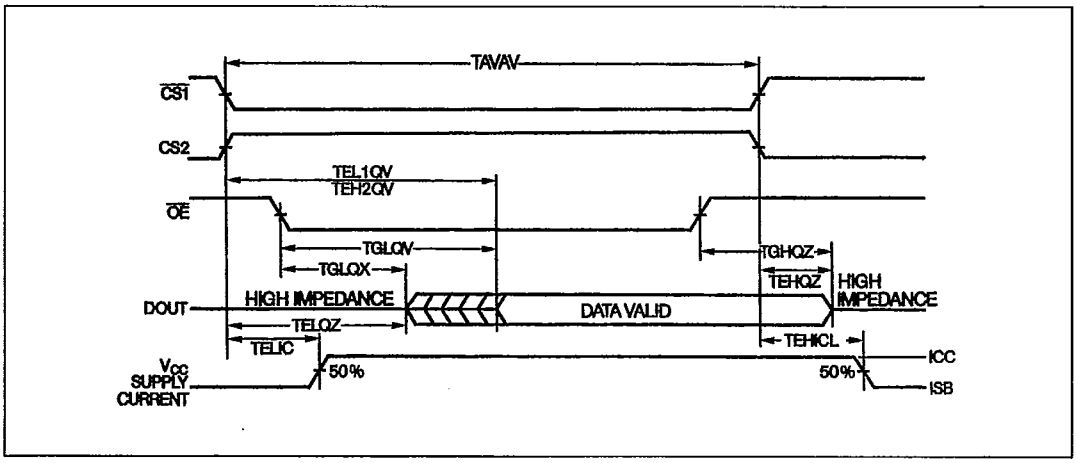
READ CYCLE nb 1 (notes 10, 11)



READ CYCLE nb 2 (notes 10, 12)



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Notes : 10. $\overline{W}$ is HIGH for read cycle.
11. Device is continuously selected $\overline{CS}_1$ & $\overline{OE}$ = VIL and CS_2 = VIH.
12. Address valid prior to or coincident with $\overline{CS}$ transition LOW.

ORDERING INFORMATION

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PROCESS FLOW

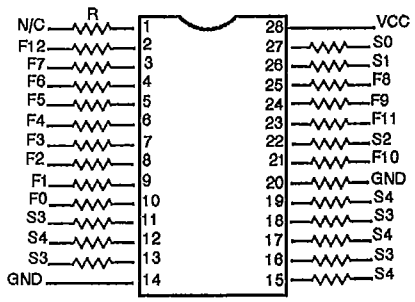
Package	Device Type	Grade	Type	Level/Class	Lot Acceptance Level
HM1	65764	M	S	B	2 *

- **Package**
  - 1 - Ceramic DIL 28
  - 4 - LCC 32 pins
  - 0 - Chip form
  - W - Wafer form
- **Device Type**
  - 8K x 8 high speed Static RAM
- **Grade**
  - H : 25 ns
  - K : 35 ns
  - M : 45 ns
  - N : 55 ns
- **Type**
  - - 9 : Industrial
  - - 2 : Military
  - - 8 : Military Program
  - M : MIL STD 883C
  - S : SCC 9000
  - C : CECC 90000
  - D : Dice HI-REL
- **Level/Class**
  - Blank : MHS test method
  - B Class : MIL STD 883C
  - B Level : SCC 9000
  - C Level : SCC 9000
  - B Level : CECC 90000
- **Lot Acceptance Level**
  - 1 : LAT 1
  - 2 : LAT 2
  - 3 : LAT 3

* only SCC 9000 specification

	PACKAGED PRODUCT						DIE FORM	
SUFFIX →	- 2	- 8	MB	CB	SB	SC	- 2	DB
DESCRIPTION →	- 55°C TO + 125°C	MILITARY PROGRAM	MIL-STD 883C CLASS B	COMPLIANT WITH CECC 90000 LEVEL B	COMPLIANT WITH SCC 9000 LEVEL B	COMPLIANT WITH SCC 9000 LEVEL C	25°C AND 125°C PROBE	HI-REL FLOW

BURN IN SCHEMATICS



R = 1K Ω per pin

Fo = 25 KHz ± 20 %
Fn = 1/2 F n-1

So, S1, S2, S3, S4 : programmable signals for write / read cycle

VCC = 5.5V

N/C not connected

Drawings for reference only.

PACKAGE OUTLINES

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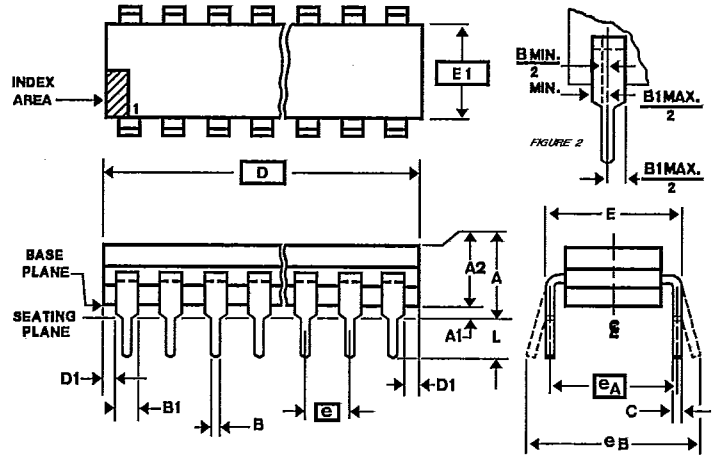

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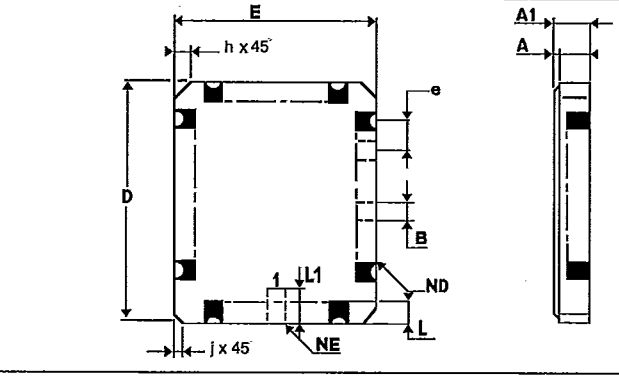
28 PINS CERDIP .300

		A	A1	A2	B	B1	C	D	D1	E	E1	e	eA	eB	L
MM	MIN	—	0.38	2.92	0.36	1.14	0.20	36.58	0.13	7.62	6.10	2.54	7.62	—	3.05
	MAX	5.84	—	4.95	0.58	1.78	0.38	37.50	—	8.25	7.87	BSC	BSC	11.43	5.08
INCHES	MIN	—	.015	.115	.014	.045	.008	1.440	.005	.300	.240	.100	.300	—	.125
	MAX	.230	—	.195	.023	.070	.015	1.476	—	.325	.310	BSC	BSC	.450	.200



32 LDS .050 CENTER LEADLESS RECTANGULAR CHIP CARRIER.

		A	A1	B	D	E	e	h	j	L	L1	ND	NE
MM	MIN	1.37	1.62	0.635	13.81	11.30	1.27	1.016	0.51	1.14	1.8	9	7
	MAX	1.93	2.23	TYP	14.22	11.63	BSC			1.4	2.11		
INCHES	MIN	.054	.064	.025	.544	.445	.050	0.40	.020	.045	.077	9	7
	MAX	.076	.088	TYP	.560	.458	BSC			.055	.083		

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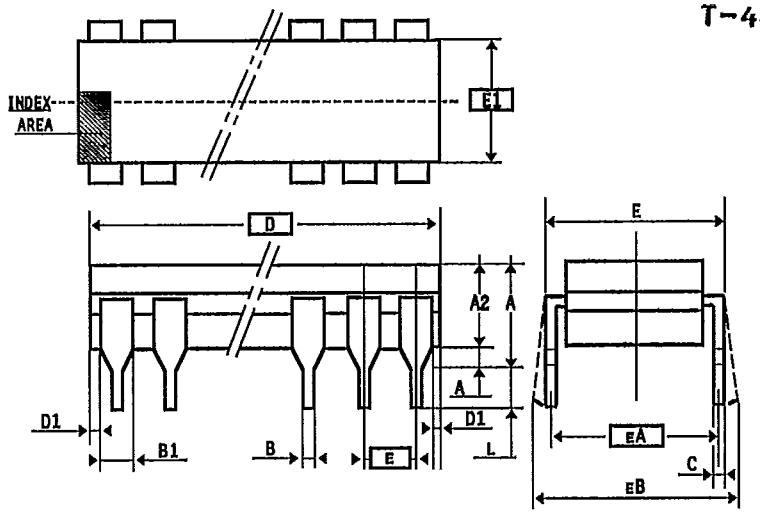

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28 LEADS CERDIP .600

		A	A1	A2	B	B1	C	D	D1	E	E1	e	eA	eB	L
MM	MIN	4.31	0.51	—	0.38	1.27	0.20	36.90	0.25	15.24	13.05	2.54	15.54	—	3.17
	MAX	5.71	1.52	4.57	0.51	1.78	0.38	38.90	—	15.75	13.66	BSC	BSC	17.78	5.08
INCHES	MIN	.170	.020	—	.014	.050	.008	1.452	.010	.600	.514	.100	.600	—	.125
	MAX	.225	.060	.180	.020	.070	.015	1.531	—	.620	.538	BSC	BSC	.700	.200