

# 1-Mbit (64K x 16) Static RAM

## Features

- Pin-and function-compatible with CY7C1021B
- High speed
  - $t_{AA} = 10 \text{ ns}$
- Low active power
  - $I_{CC} = 80 \text{ mA @ } 10 \text{ ns}$
- Low CMOS Standby Power
  - $I_{SB2} = 3 \text{ mA}$
- 2.0V Data Retention
- Automatic power-down when deselected
- CMOS for optimum speed/power
- Independent control of upper and lower bits
- Available in Pb-free 44-pin 400-Mil wide Molded SOJ and 44-pin TSOP II packages

## Functional Description <sup>[1]</sup>

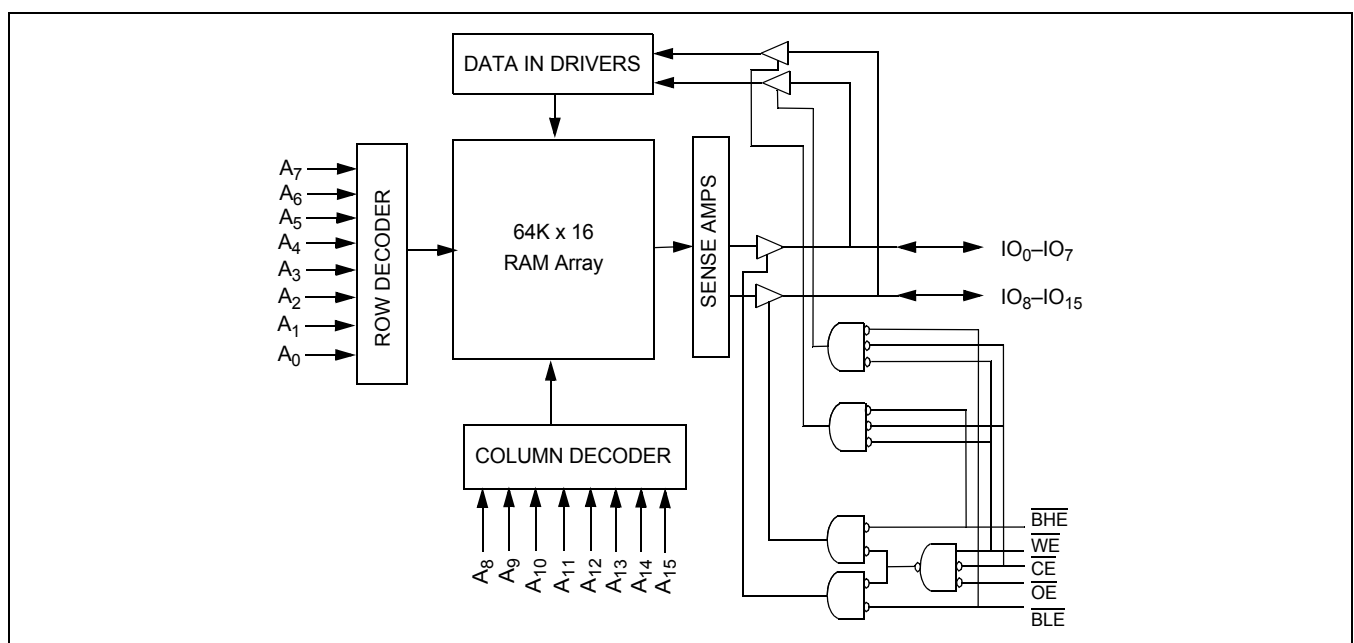
The CY7C1021D is a high-performance CMOS static RAM organized as 65,536 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected. The input/output pins (IO<sub>0</sub> through IO<sub>15</sub>) are placed in a high-impedance state when:

- Deselected ( $\overline{CE}$  HIGH)
- Outputs are disabled ( $\overline{OE}$  HIGH)
- BHE and BLE are disabled (BHE, BLE HIGH)
- When the write operation is active ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW)

Write to the device by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from IO pins (IO<sub>0</sub> through IO<sub>7</sub>), is written into the location specified on the address pins (A<sub>0</sub> through A<sub>15</sub>). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from IO pins (IO<sub>8</sub> through IO<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>15</sub>).

Read from the device by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins appears on IO<sub>0</sub> to IO<sub>7</sub>. If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory appears on IO<sub>8</sub> to IO<sub>15</sub>. See the "Truth Table" on page 8 for a complete description of read and write modes.

## Logic Block Diagram



### Note

1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at [www.cypress.com](http://www.cypress.com).

**Pin Configuration** <sup>[2]</sup>
**SOJ/TSOP II  
Top View**

A <sub>4</sub>	□ 1	44	□ A <sub>5</sub>
A <sub>3</sub>	□ 2	43	□ A <sub>6</sub>
A <sub>2</sub>	□ 3	42	□ A <sub>7</sub>
A <sub>1</sub>	□ 4	41	□ $\overline{OE}$
A <sub>0</sub>	□ 5	40	□ $\overline{BHE}$
$\overline{CE}$	□ 6	39	□ $\overline{BLE}$
IO <sub>0</sub>	□ 7	38	□ IO <sub>15</sub>
IO <sub>1</sub>	□ 8	37	□ IO <sub>14</sub>
IO <sub>2</sub>	□ 9	36	□ IO <sub>13</sub>
IO <sub>3</sub>	□ 10	35	□ IO <sub>12</sub>
V <sub>CC</sub>	□ 11	34	□ V <sub>SS</sub>
V <sub>SS</sub>	□ 12	33	□ V <sub>CC</sub>
IO <sub>4</sub>	□ 13	32	□ IO <sub>11</sub>
IO <sub>5</sub>	□ 14	31	□ IO <sub>10</sub>
IO <sub>6</sub>	□ 15	30	□ IO <sub>9</sub>
IO <sub>7</sub>	□ 16	29	□ IO <sub>8</sub>
$\overline{WE}$	□ 17	28	□ NC
A <sub>15</sub>	□ 18	27	□ A <sub>8</sub>
A <sub>14</sub>	□ 19	26	□ A <sub>9</sub>
A <sub>13</sub>	□ 20	25	□ A <sub>10</sub>
A <sub>12</sub>	□ 21	24	□ A <sub>11</sub>
NC	□ 22	23	□ NC

**Selection Guide**

	<b>-10 (Industrial)</b>	<b>-12 (Automotive)</b> <sup>[3]</sup>	<b>Unit</b>
Maximum Access Time	10	12	ns
Maximum Operating Current	80	120	mA
Maximum CMOS Standby Current	3	15	mA

**Notes**

- NC pins are not connected on the die.
- Automotive Product Information is Preliminary.

### Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied..... -55°C to +125°C

Supply Voltage on  $V_{CC}$  to Relative GND <sup>[4]</sup> ... -0.5V to +6.0V

DC Voltage Applied to Outputs in High-Z State <sup>[4]</sup> ..... -0.5V to  $V_{CC}+0.5V$

DC Input Voltage <sup>[4]</sup>..... -0.5V to  $V_{CC}+0.5V$

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current ..... > 200 mA

### Operating Range

Range	Ambient Temperature	$V_{CC}$	Speed
Industrial	-40°C to +85°C	5V ± 10%	10 ns
Automotive	-40°C to +125°C		12 ns

### Electrical Characteristics (Over the Operating Range)

Parameter	Description	Test Conditions	-10 (Industrial)		-12 (Automotive)		Unit	
			Min	Max	Min	Max		
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -4.0 \text{ mA}$	2.4		2.4		V	
$V_{OL}$	Output LOW Voltage	$I_{OL} = 8.0 \text{ mA}$		0.4		0.4	V	
$V_{IH}$	Input HIGH Voltage		2.2	$V_{CC} + 0.5V$	2.0	$V_{CC} + 0.5V$	V	
$V_{IL}$	Input LOW Voltage <sup>[4]</sup>		-0.5	0.8	-0.5	0.8	V	
$I_{IX}$	Input Leakage Current	$GND \leq V_I \leq V_{CC}$	-1	+1	-5	+5	$\mu\text{A}$	
$I_{OZ}$	Output Leakage Current	$GND \leq V_I \leq V_{CC}$ , Output Disabled	-1	+1	-5	+5	$\mu\text{A}$	
$I_{CC}$	$V_{CC}$ Operating Supply Current	$V_{CC} = \text{Max}$ , $I_{OUT} = 0 \text{ mA}$ , $f = f_{\text{max}} = 1/t_{RC}$	100 MHz	80		-	mA	
			83 MHz		72		120	mA
			66 MHz		58		100	mA
			40 MHz		37		63	mA
$I_{SB1}$	Automatic CE Power-down Current —TTL Inputs	$\text{Max } V_{CC}$ , $\overline{CE} \geq V_{IH}$ , $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{\text{max}}$		10		50	mA	
$I_{SB2}$	Automatic CE Power-down Current —CMOS Inputs	$\text{Max } V_{CC}$ , $\overline{CE} \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ , or $V_{IN} \leq 0.3V$ , $f = 0$		3		15	mA	

**Note**

4.  $V_{IL}(\text{min}) = -2.0V$  and  $V_{IH}(\text{max}) = V_{CC} + 1V$  for pulse durations of less than 5 ns.

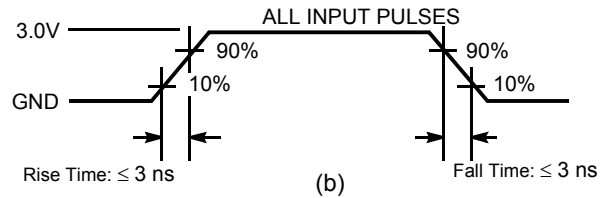
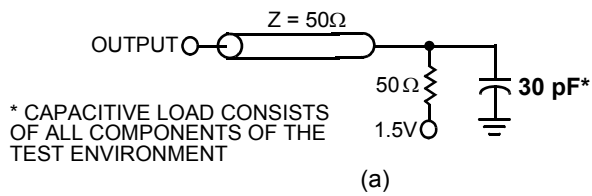
**Capacitance** [5]

Parameter	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	8	pF
C <sub>OUT</sub>	Output Capacitance		8	pF

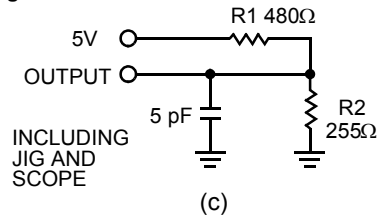
**Thermal Resistance** [5]

Parameter	Description	Test Conditions	SOJ	TSOP II	Unit
Θ <sub>JA</sub>	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	59.52	53.91	°C/W
Θ <sub>JC</sub>	Thermal Resistance (Junction to Case)		36.75	21.24	°C/W

**AC Test Loads and Waveforms** [6]



**High-Z characteristics:**



**Notes**

5. Tested initially and after any design or process changes that may affect these parameters.
6. AC characteristics (except High-Z) are tested using the load conditions shown in Figure (a). High-Z characteristics are tested for all speeds using the test load shown in Figure (c).

**Switching Characteristics** (Over the Operating Range) <sup>[7]</sup>

Parameter	Description	-10 (Industrial)		-12 (Automotive)		Unit
		Min	Max	Min	Max	
<b>Read Cycle</b>						
$t_{power}^{[8]}$	$V_{CC}$ (typical) to the first access	100		100		$\mu$ s
$t_{RC}$	Read Cycle Time	10		12		ns
$t_{AA}$	Address to Data Valid		10		12	ns
$t_{OHA}$	Data Hold from Address Change	3		3		ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid		10		12	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		5		6	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z <sup>[9]</sup>	0		0		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[9, 10]</sup>		5		6	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low Z <sup>[9]</sup>	3		3		ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High Z <sup>[9, 10]</sup>		5		6	ns
$t_{PU}$	$\overline{CE}$ LOW to Power-Up	0		0		ns
$t_{PD}$	$\overline{CE}$ HIGH to Power-Down		10		12	ns
$t_{DBE}$	Byte Enable to Data Valid		5		6	ns
$t_{LZBE}$	Byte Enable to Low Z	0		0		ns
$t_{HZBE}$	Byte Disable to High Z		5		6	ns
<b>Write Cycle</b> <sup>[12]</sup>						
$t_{WC}$	Write Cycle Time	10		12		ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	7		10		ns
$t_{AW}$	Address Set-Up to Write End	7		10		ns
$t_{HA}$	Address Hold from Write End	0		0		ns
$t_{SA}$	Address Set-Up to Write Start	0		0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	7		10		ns
$t_{SD}$	Data Set-Up to Write End	6		7		ns
$t_{HD}$	Data Hold from Write End	0		0		ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[9]</sup>	3		3		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[9, 10]</sup>		5		6	ns
$t_{BW}$	Byte Enable to End of Write	7		10		ns

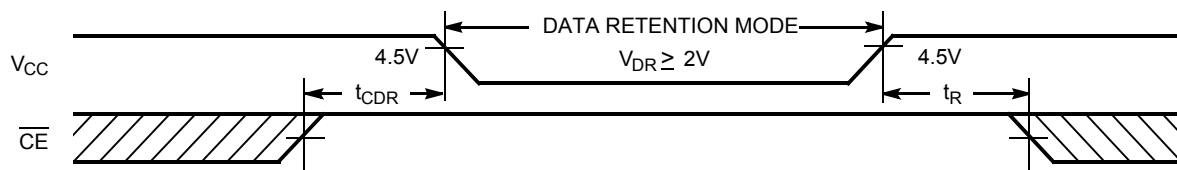
**Notes**

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
- $t_{POWER}$  gives the minimum amount of time that the power supply should be at typical  $V_{CC}$  values until the first memory access can be performed.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- $t_{HZOE}$ ,  $t_{HZBE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in (c) of "AC Test Loads and Waveforms [6]" on page 4. Transition is measured when the outputs enter a high impedance state.
- This parameter is guaranteed by design and is not tested.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW,  $\overline{WE}$  LOW and  $\overline{BHE}/\overline{BLE}$  LOW.  $\overline{CE}$ ,  $\overline{WE}$  and  $\overline{BHE}/\overline{BLE}$  must be LOW to initiate a write, and the transition of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

**Data Retention Characteristics** (Over the Operating Range)

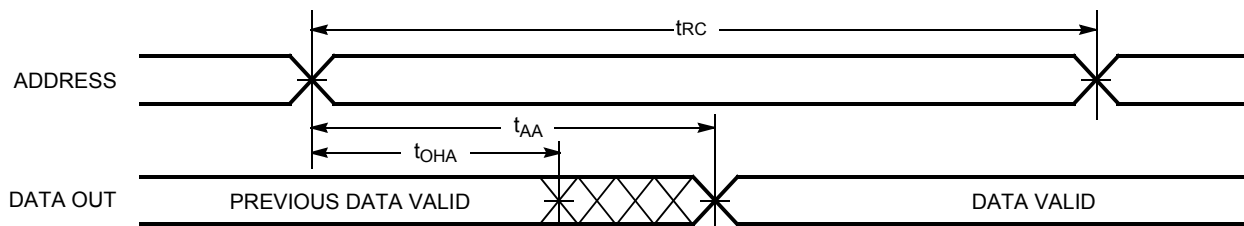
Parameter	Description	Conditions	Min	Max	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		2.0		V
$I_{CCDR}$	Data Retention Current	$V_{CC} = V_{DR} = 2.0\text{ V}$ , $\overline{CE} \geq V_{CC} - 0.3\text{ V}$ , $V_{IN} \geq V_{CC} - 0.3\text{ V}$ or $V_{IN} \leq 0.3\text{ V}$		3	mA
$t_{CDR}^{[4]}$	Chip Deselect to Data Retention Time		0		ns
$t_R^{[13]}$	Operation Recovery Time		$t_{RC}$		ns

**Data Retention Waveform**

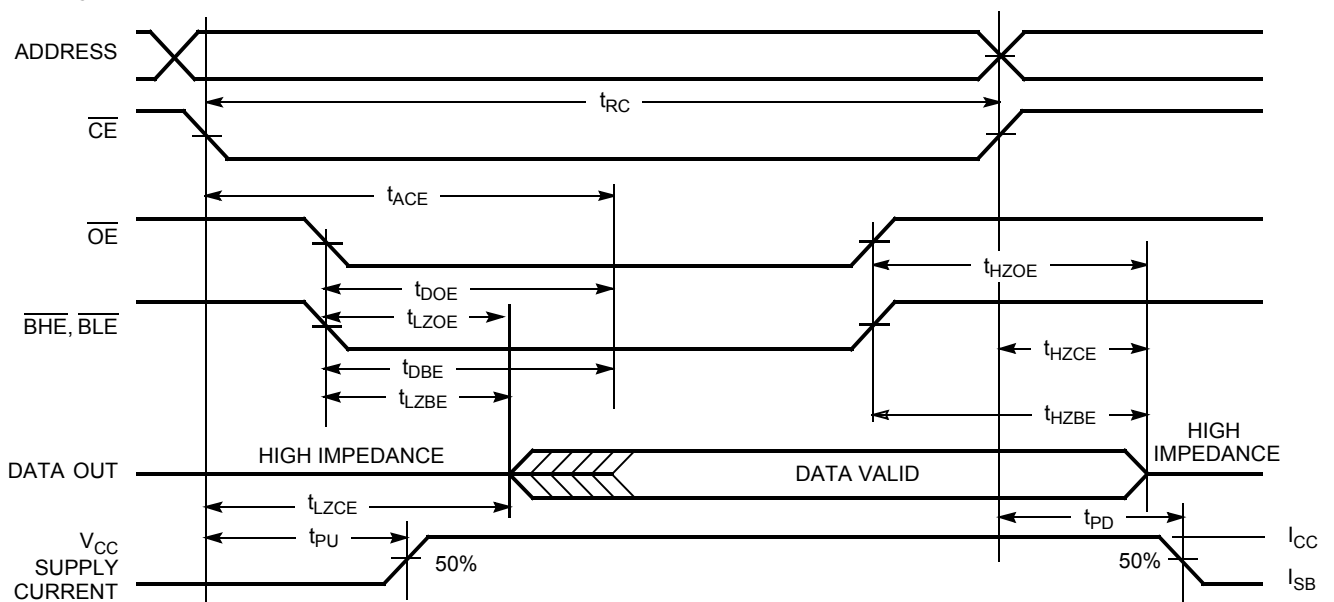


**Switching Waveforms**

**Read Cycle No. 1** (Address Transition Controlled) [14, 15]



**Read Cycle No. 2** ( $\overline{OE}$  Controlled) [15, 16]

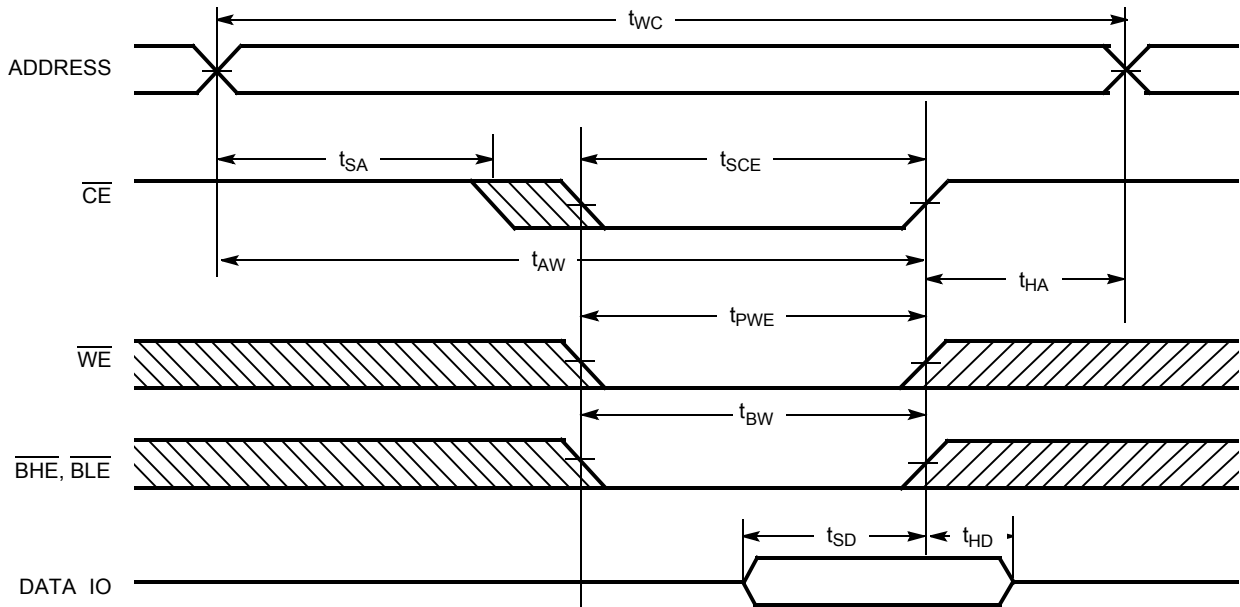


**Notes**

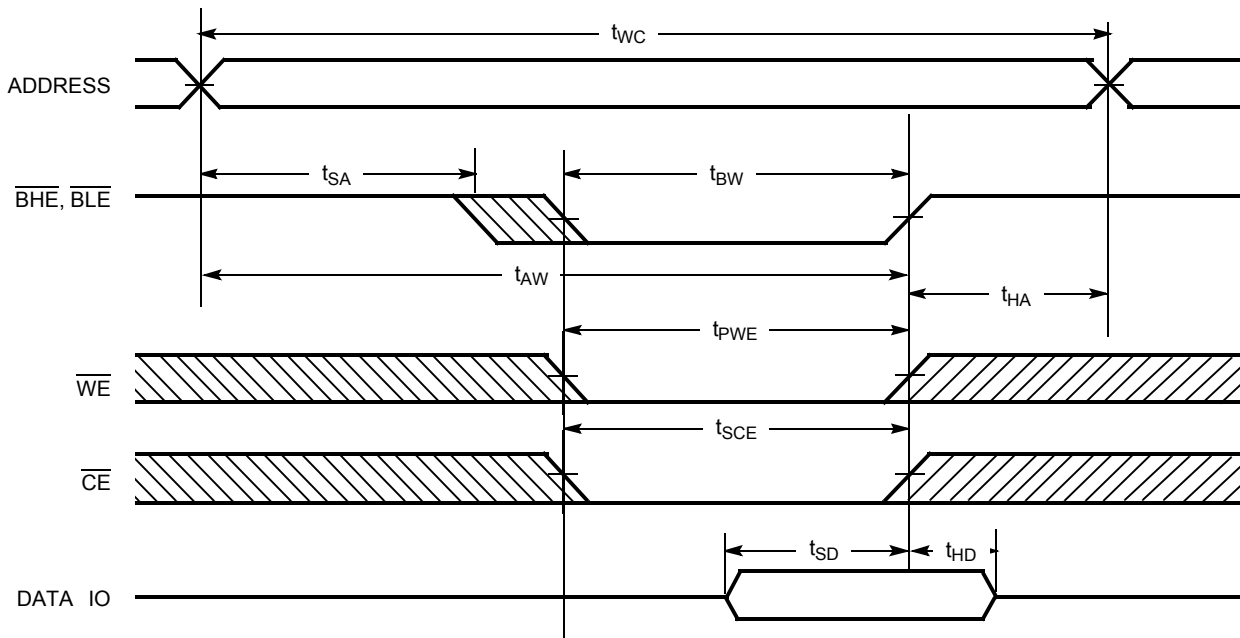
- 13. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \geq 50\ \mu\text{s}$  or stable at  $V_{CC(min)} \geq 50\ \mu\text{s}$ .
- 14. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ .
- 15.  $\overline{WE}$  is HIGH for read cycle.
- 16. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

**Switching Waveforms** (continued)

**Write Cycle No. 1** ( $\overline{CE}$  Controlled) [17, 18]



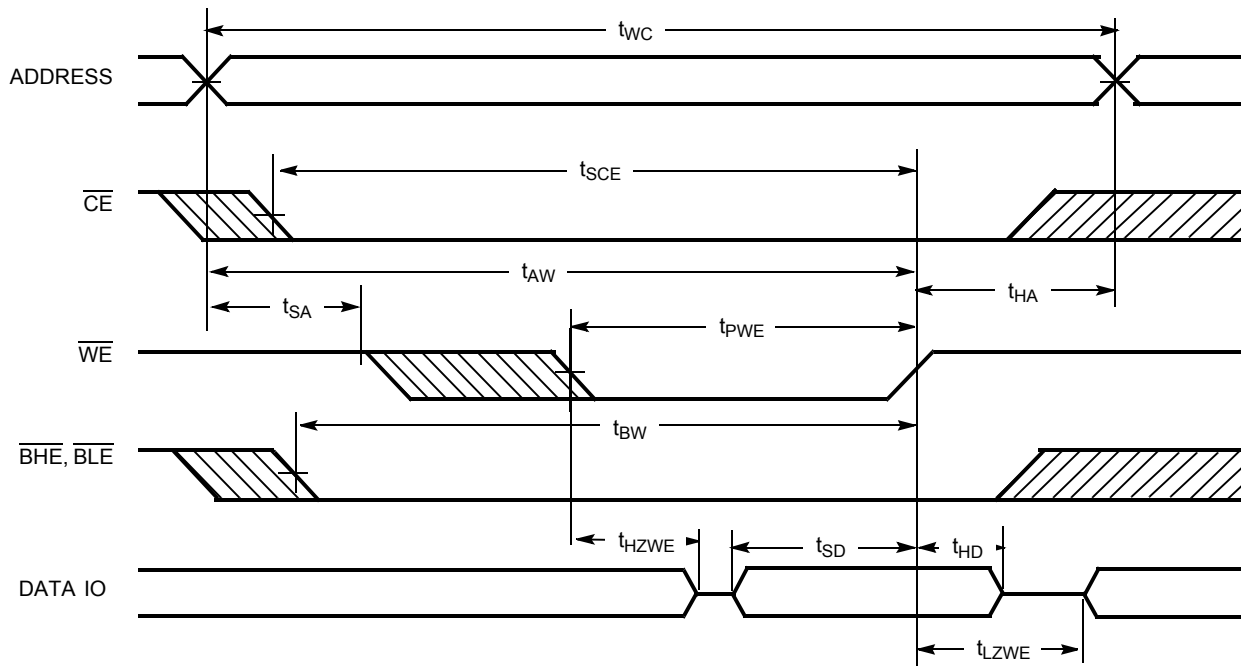
**Write Cycle No. 2** ( $\overline{BLE}$  or  $\overline{BHE}$  Controlled)



**Notes**

- 17. Data IO is high impedance if  $\overline{OE}$  or  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IH}$ .
- 18. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.

**Switching Waveforms** (continued)

**Write Cycle No. 3** ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)

**Truth Table**

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	$IO_0-IO_7$	$IO_8-IO_{15}$	Mode	Power
H	X	X	X	X	High Z	High Z	Power-Down	Standby ( $I_{SB}$ )
L	L	H	L	L	Data Out	Data Out	Read – All bits	Active ( $I_{CC}$ )
			L	H	Data Out	High Z	Read – Lower bits only	Active ( $I_{CC}$ )
			H	L	High Z	Data Out	Read – Upper bits only	Active ( $I_{CC}$ )
L	X	L	L	L	Data In	Data In	Write – All bits	Active ( $I_{CC}$ )
			L	H	Data In	High Z	Write – Lower bits only	Active ( $I_{CC}$ )
			H	L	High Z	Data In	Write – Upper bits only	Active ( $I_{CC}$ )
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active ( $I_{CC}$ )
L	X	X	H	H	High Z	High Z	Selected, Outputs Disabled	Active ( $I_{CC}$ )

**Ordering Information**

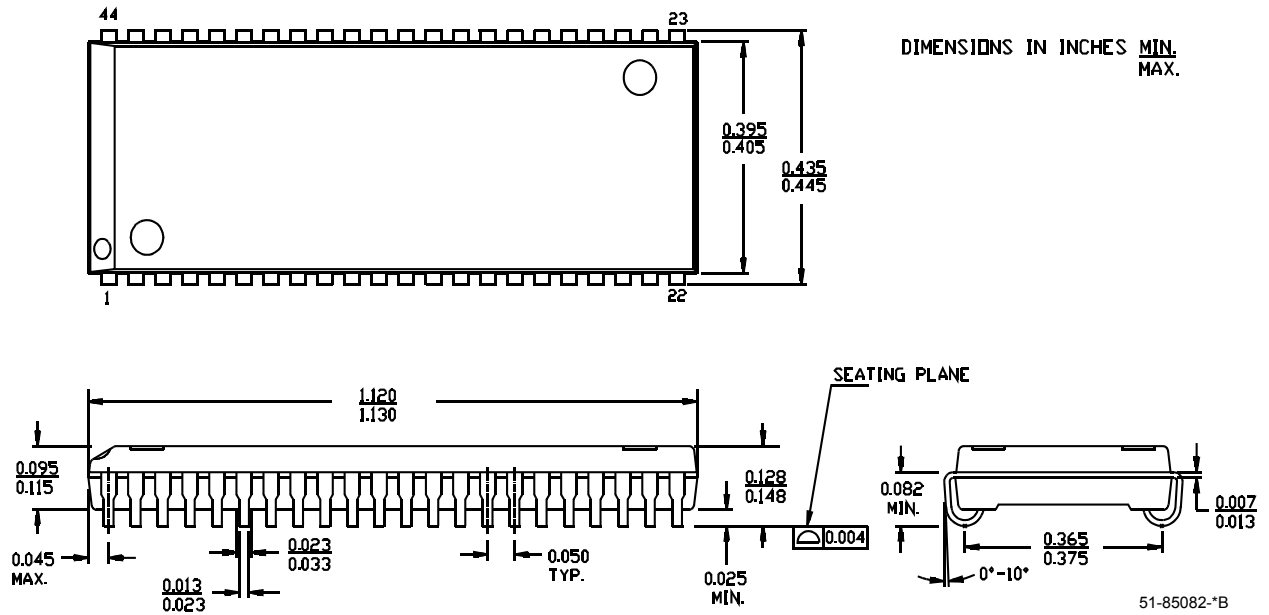
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1021D-10VXI	51-85082	44-pin (400-Mil) Molded SOJ (Pb-free)	Industrial
	CY7C1021D-10ZSXI	51-85087	44-pin TSOP Type II (Pb-free)	
12	CY7C1021D-10ZSXE	51-85087	44-pin TSOP Type II (Pb-free)	Automotive

Shaded areas contain advance information. Please contact your local Cypress sales representative for availability of these parts.



Package Diagrams

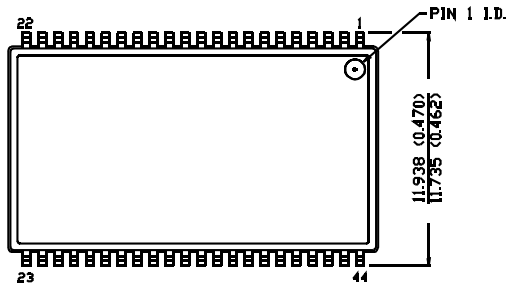
Figure 1. 44-pin (400-Mil) Molded SOJ, 51-85082



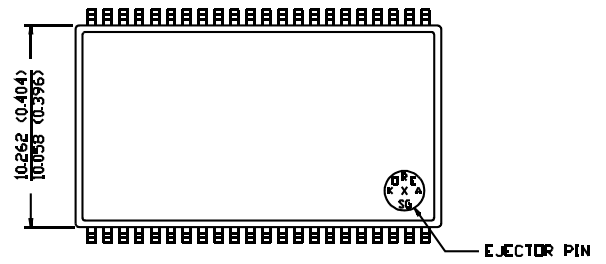
Package Diagrams (continued)

Figure 2. 44-Pin Thin Small Outline Package Type II, 51-85087

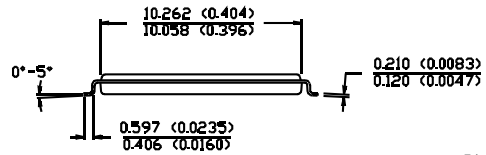
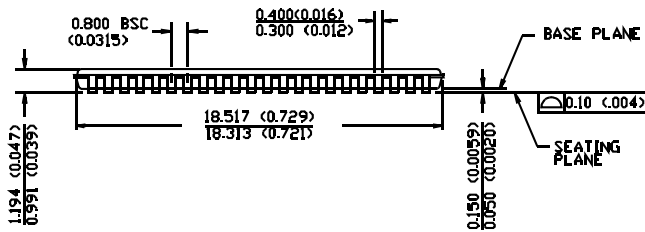
DIMENSION IN MM (INCH)  
MAX  
MIN



TOP VIEW



BOTTOM VIEW



51-85087-A

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**Document History Page**

Document Title: CY7C1021D, 1-Mbit (64K x 16) Static RAM				
Document Number: 38-05462				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	201560	See ECN	SWI	Advance Information data sheet for C9 IPP
*A	233695	See ECN	RKF	DC parameters modified as per EROS (Spec # 01-02165) Pb-free Offering in the Ordering Information
*B	263769	See ECN	RKF	Added Data Retention Characteristics Table Added T <sub>power</sub> Spec in Switching Characteristics Table Shaded Ordering Information
*C	307601	See ECN	RKF	Reduced Speed bins to -10 and -12 ns
*D	520647	See ECN	VKN	Converted from Preliminary to Final Removed Commercial Operating range Added I <sub>CC</sub> values for the frequencies 83MHz, 66MHz and 40MHz Updated Thermal Resistance table Added Automotive Product Information Updated Ordering Information Table Changed Overshoot spec from V <sub>CC</sub> +2V to V <sub>CC</sub> +1V in footnote #4
*E	802877	See ECN	VKN	Changed Commercial operating range I <sub>CC</sub> spec from 60 mA to 80 mA for 100MHz, 55 mA to 72 mA for 83MHz, 45 mA to 58 mA for 66MHz, 30 mA to 37 mA for 40MHz Changed Automotive operating range I <sub>CC</sub> spec from 100 mA to 120 mA for 83MHz, 90 mA to 100 mA for 66MHz, 60 mA to 63 mA for 40MHz