AML 8613 A/V Processor User's Guide

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Revision History

Revision Number	Revised Date	By	Changes
0.1	May 28,2008	Jesse W	Initial Version
0.2	Oct 15, 2008	QL Tu	Revision
0.3	Nov 11, 2008	Julius Z	Revision
0.4	Nov 13, 2008	QL Tu	Revision
0.41	Dec 12, 2008	QL Tu	Modify reset config(remove M2), change Max SDRAM to 32MB

1. Introduction

The AML8613 A/V processor is a complete integrated system targeting Media box (MBX) backend applications. The AML8613 device includes a 333 MHz embedded RISC CPU, A/V decoders, crypto-engine, transport interface, smartcard interface and USB for the MBX applications. The AML8613 firmware provides all A/V decoding functions, and USB stacks.

The AML8613 combines full function of MPEG-1, MPEG-2, MPEG-4 and Real-Video decoding, numerous dedicated and general-purpose peripherals, and a high speed 32-bit host CPU in a single device. The AML8613 has two built-in AMRISC™ RISC processors with special instructions to accommodate audio and video digital signal processing. The AML8613 device provides many on-chip I/O peripherals. The peripherals include one USB 2.0 High-Speed OTG controllers and PHYs; a memory card reader controller.

The embedded 32-bit core CPU controls all system related application software. It executes AVOS, the base operating system for AML8613. All applications and drivers run on top of AVOS. Drivers including MBX processing, smartcard driver, USB drivers and other hardware related programming interfaces are provided by AVOS. Applications including, graphical user interfaces, on-screen displays (OSD), and file system sub-system are also included in AVOS. Developers can add additional applications to customize AVOS for each unique product platform.

The core CPU interfaces to the video and audio processing hardware. MPEG1/2/4, HVD/EVD, Real-Video and JPEG/M-JPEG streams are processed by dedicated video decoding hardware and the flexible Video AMRISC™ engine. The hardware and microcode combination is capable of decoding normal D1 size video sequence at full speed, and JPEG pictures with no limits. Pixel based de-interlacing is applied to the video sequence for high quality video output.

Once decoded, the output pictures are passed to a sophisticated video sub-system that performs video enhancement and scaling functions. Contrast enhancement, hue adjustment, video scaling, video interpolation, pan-scan, letter-box, and zoom are also supported. The scalar supports both up-scaling and down-scaling of images and video. The scalar can also mix in multiple graphics and OSD layers for the final display.

The integrated Audio AMRISC™ RISC processor performs advanced digital audio decoding and post-processing. The micro-coded engine provides support for all existing audio formats and it also has enough flexibility to accommodate new audio standards. Popular audio formats like MPEG, LPCM, Dolby AC-3 5.1, HDCD, MP-3, WMA, AAC, Real-Audio can be supported. In addition, SPDIF (IEC958) outputs are supported.

The AML8613 also integrated one USB 2.0 High Speed OTG controllers and PHYs for connecting to USB hard disk, FLASH memory, digital cameras and MP3 players. The AVOS drivers and applications for AML8613 firmware includes the basic USB device driver, USB protocol stacks to support bulk and INTR transfer, Hub, Mass-Storage (MS) class, Picture Transfer Protocol (PTP) and PictBridge protocol. The AVOS USB firmware also supports multiple file systems and includes flexible file transfer functions between USB devices.

The AML8613 supports all popular memory card formats and protocols. For example, Secure Digital cards (SD/SDHC), Sony Memory Stick (MS), MMC.

AML8613 A/V processor has a set of very flexible clocking circuits that implement the adaptive AMPOWER-II power reduction algorithms. The chip works in conjunction with the AVOS software to reduce total power consumption based on processing load, type of media streams being processed and the output requirements. With AMPOWER-II, the system can reduce power consumption for portable applications and helps consumer electronics to achieve the Energy Star rating. In addition, AMPOWER-II also provides higher performance within smaller, thermally constrained environments.

2. Features

The AML8613 chip is very flexible and most of the capabilities are under firmware control. The following list of features may or may not be included in the firmware library or binary, depending on the actual application and platform.

High Integration

- Embedded 32-bit core RISC processor for system control
- Complete RealVideo, MPEG 1/2/4 decoding backend and video post processing logic
- Complete audio decoding backend
- Integrated one USB 2.0 High Speed OTG ports
- Integrated card reader controllers
- Integrated TV encoder and triple video DACs

RealVideo Decoding

- RealVideo decoding engine controlled by a dedicated Video AMRISC™ processor
- Decodes RealVideo-8/9/10 video streams
- *.rm and *.rmvb file formats can be handled by AVOS

MPEG 1/2 Decoding

- MPEG video engine controlled by a dedicated Video AMRISC™ processor
- MPEG-2 ML/MP conforming to ISO-13818
- MPEG-1 ML/MP conforming to ISO-11172
- Sub-picture and highlight decoding and display
- Advanced error detection, concealment, and recovery scheme
- *.mpg, *.mpeg, *.dat, and *.avi file formats can be handled by AVOS and CPU subsystems

MPEG 4 Decoding

- MPEG-4 ASP and XVID compliant
- GMC and Q-Pel
- Multiple language and multiple formats DivX sub-title support
- *.avi file formats can be handled by AVOS and CPU subsystems

JPEG/M-JPEG Decoding

- Super fast hardware decoding of JPEG picture
- Unlimited pixel resolution (currently test with 16M pixel pictures)
- Supports scaling (zoom in or out), rotation and transition effects
- M-JPEG engine supports up to full frame rate (30 fps) quality movies

Other Images/Pictures Decoding

- Decodes BMP, PNG, GIF, TIFF and other popular picture formats
- Supports zoom in and out, rotation and transition effects
- Zoom supported in 2x mode

Video Processing

- 3:2 pull-down for 24 fps displaying at 30 fps0
- 2:2 pull-down for 24 fps displaying at 25 fps
- Adaptive pixel-based de-interlacing algorithm
- Variable steps video zooming (up to 8x)
- Letterbox and pan/scan
- Built-in NTSC to PAL scaling or vice-versa
- 1st On-Screen-Display (OSD1) capable of supporting 4/16/256/16k colors or True-Color
- OSD alpha-blending over video display
- 2nd OSD supporting 16 colors (OSD2).
- Global Alpha for OSD1/OSD2

TV Encoder

- Interlaced NTSC output 720x480 at 30 fps, with Macrovision 7.1L1 anti-taping
- Interlaced PAL output 720x576 at 25 fps, with Macrovision 7.1L1 anti-taping
- Progressive NTSC output 480p at 60 fps, with Macrovision 1.03 anti-taping
- Progressive PAL output 576p at 50 fps, with Macrovision 1.03 anti-taping
- High definition output of 720p
- component, composite(Y/Pb/Pr, YUV) output
- Closed caption modulation in the vertical blanking intervals
- Programmable tint, brightness and other TV enhancements

Graphics

- Graphics can be scaled independently of the video output
- Unified MPEG video and graphics memory architecture for maximum flexibility and system cost savings

Audio Decoding

- Built-in Audio AMRISC™ processor with extensions specifically designed for audio processing
- On-the-fly switching of audio streams during playback
- Full RealAudio decoding
- Full MPEG audio layers I, II and III
- Compliant with Dolby AC-3 5.1 channel decoding
- HDCD support
- Capable of decoding many audio formats including: MP3, WMA, WAV, Ogg Vorbis, AAC.

Audio Post Processing and Output

- Integrated a 2-channel delta-sigma audio DAC for low cost system configuration.
- Two channels analog output or 8 channels linear PCM output. I^2S or EIAJ DAC-compatible
- IEC958 (S/PDIF) digital output
- DTS audio pass-through
- AC-3 two channels down-mixing
- Virtual surround sound to create 3-D spatial sound field from two audio channels
- Prologic II to convert stereo audio source to multi-channel audio output
- Full speaker configurations and bass management with adjustable crossover settings
- Muting, volume control, etc.

USB Interface

- Integrated one OTG 2.0 High Speed controllers and PHYs
- Backward compatible with USB 1.1 devices
- USB port can be configured as USB device, host or OTG port
- DMA support for data movement for BULK, INTR and ISO transfer
- USB device driver, native USB protocol stack supported in AVOS firmware
- Integrated support for Mass-storage class (MS-Class), Picture Transfer Protocol (PTP), PictBridge protocol and USB communication class
- USB Hub support
- Video, audio and image decoding from USB attached MS-Class or PTP devices
- Photo printing to USB attached PictBridge devices
- Connecting to PCs or Apple computers as USB MS-Class devices

Card Reader Interfaces and Controllers

- Supports MS, SD/SDHC, and MMC memory card formats
- Supports reading and play back of audio, picture and video multimedia files
- AVOS software supports all file operations via file system on each memory card

Core CPU Sub-system

- High speed 333MHz 32-bit core CPU dedicated for user applications
- Embedded debug interface using ICE/JTAG
- Shared MPEG SDRAM as run time data storage for minimal system cost

- Integrated interrupt controller, general purpose timers and counters
- Integrated general purpose DMA controllers
- Supports 8-bit or 16-bit NAND or 4 wire SPI NOR FLASH
- Support for MLC NAND Flash with 9-bits of ECC
- SDRAM interface can support up to 32M bytes of SDRAM

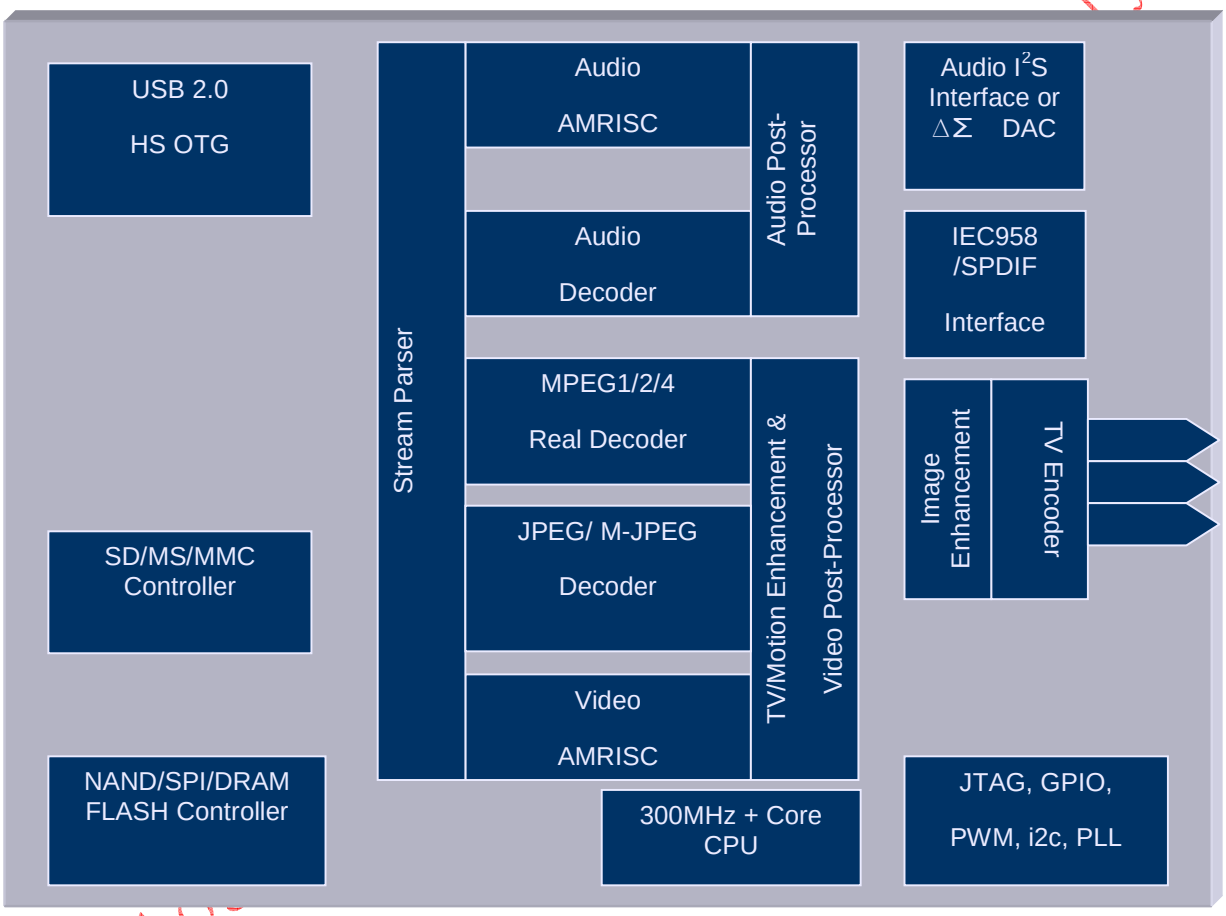
System, Peripherals and Misc. Interfaces

- Single 27 MHz crystal oscillator input
- AMPOWER-II power reduction algorithm for portable devices
- Numerous programmable GPIO pins for system control and interrupts
- Integrated i2c slave and master controllers,
- Enhanced UART controller
- Remote control input circuit with digital input filter
- PWM output pins
- 1.2 volt and 3.3 volt power supplies
- 3.3 volt I/O support
- 144 pins LQFP RoHS package

3. Architecture Overview

3.1 Architecture

The AML8613 is a highly integrated SOC device that provides cost-effective solutions for media players, Media boxes, and integrated entertainment centers. Since the device is very sophisticated, the following discussion is divided into multiple areas: Back-end MPEG decoders, audio decoders, output stages, I/O interfaces like USB, card-readers, NAND, etc.



3.2 Video/Picture Processing

The decoder architecture is optimized for audio and video streaming applications. With the architecture separation of the application specific interface (e.g. USB file system), and the output stage, the decoders can be used in a large variety of applications. The decoder utilizes external SDRAM for input video, photo, audio, sub-pictures, navigation, OSD data buffers, and decoded frame buffers.

3.2.1 A/V Stream Parser

The A/V Stream Parser is a programmable engine that works in conjunction with the Video AMRISC™ processor for the following functions:

- Accepts audio/video bit stream as the input
- Performs decryption and unscrambling for encrypted bit streams
- De-multiplexes the bit streams into multiple buffers, like encoded video, audio, sub-pictures, and navigation information

- Deposits the parsed data into the SDRAM
- Controls the buffer level of the audio decoding core and video decoding core
- A/V Sync handling

Once the stream is decrypted, the parser searches for stream IDs within the stream, looking for the correct video, audio or other data to extract. The extracted data is stored into multiple buffers in the system SDRAM. All buffer sizes and locations are programmable depending on the application

3.2.2 RealVideo, MPEG 1/2/4 Video Decoder

The MPEG Decoder works in conjunction with the Video AMRISC™ processor for the following functions:

- RealVideo 8/9/10 decoding
- MPEG 1/2/4 decoding
- Adaptive pixel-based de-interlacing (including 3:2 pull-down detection)
- Frame rate conversion (3:2 pull-down, 2:2 pull-down, 50/60Hz conversion and any combination conversion)

The MPEG decoder performs all necessary MPEG video streams decoding logic for MPEG-1, MPEG-2 and MPEG-4 ASP. That includes VLD decoding, IQ, IDCT, motion vector parsing, motion compensation, block predication and picture reconstruction. Multiple decoded pictures are placed in the frame buffers in SDRAM. Frame buffers are used to store I (Intra Coded Pictures), P (Predicted Pictures) and B (Bi-directionally predicted) pictures. The video post-processor pulls decoded pictures for display purposes.

The RealVideo decoder decodes RealVideo 8/9/10 formatted movies. A dedicated RealVideo loop filter is added especially for Real processing.

In addition to the traditional RealVideo, MPEG processing, the MPEG decoder performs adaptive pixel-based de-interlacing and 3:2 pull-down detection/reversal to improve output picture quality for progressive displays.

3.2.3 JPEG/M-JPEG Picture/Movie Decoder

The MPEG decoder can decode picture formats like JPEG and Motion JPEG (M-JPEG). Both JPEG (*.jpg) and M-JPEG (*.avi) are popular formats used by digital cameras. JPEG is used as the still picture format. M-JPEG is used as the video capture format.

The video decoder will read and decode the JPEG picture and scale the decoded output to the proper size to store in memory for display purpose. Since the MPEG processor has a streaming interface, there is no size limitation of the original compressed JPEG picture.

The MPEG decoder can also process Motion JPEG sequence. It is capable of supporting VGA resolution MJPEG streams at 30 frames-per-second. M-JPEG streams can be rotated or flip (to adjust for customers using digital camera to film home video) in real-time while being displayed.

3.2.4 Video Post-Processor

The Video Post-Processor (VPP) performs functions related to combining and scaling multiple video, graphics, OSD and sub-pictures video planes. The video post processor fetches data from each image plane (e.g. decoded video frames), performs sophisticated multi-taps filtering/scaling to generate a new pixel for output, and combines the result with other filtered data to generate the final video image. The video post-processor is capable of performing alpha-bending between multiple image planes. The VPP is capable of both scaling up (zoom in) and scaling down (zoom out).

3.2.5 Video Encoder, Video DAC and Digital Video Output

The AML8613 device contains a video encoder that can handle both progressive and interlace video output. In addition to the analog video DAC output interface, the video encoder's TTL output module

also generates high-definition digital video signals for external transmitter devices. The following is the basic features of the AML8613 internal TV encoder:

- output capability 576P/720P
- NTSC and PAL output (including progressive 480 and 576 outputs and SCART)

The video encoder also provides many video adjustment options. The video encoder has luma and chroma bandwidth control, programmable saturation, hue, contrast, black level and brightness adjustments.

The video encoders generate up to three video output streams to the built-in high performance video DACs. The video DAC outputs are fully programmable to support composite video, component video (YUV), YPbPr. Also, simultaneous progressive and interlace modes are also supported.

3.3 Audio Processing

3.3.1 Audio Decoding and Post-Processing

The audio processing architecture is based on the Audio AMRISC™ processor with direct hardware assist functions from the audio decoder hardware. Since the Audio AMRISC™ processor is a micro-coded engine, the AML8613 device is capable of supporting the decoding of all existing audio formats (PCM, Dolby AC-3 5.1, MPEG Layer I/II/III, WMA, MP3, AAC, RealAudio, Ogg Vobris) and can be programmed to support customer specific audio requirements. The Audio AMRISC™ processor has its own internal code/data RAM/ROM for supporting the high frequency requirements (e.g. 320kbps for MP3) for realistic sound reproduction.

In addition to supporting multiple audio formats, the AML8613 device implements many different audio post-processing algorithms. Post processing algorithms are used to optimize the audio output for a specific speaker's capabilities, and to personalize the audio set up for individuals. Post-processing algorithms supported included:

- Dolby Prologic II, Dolby Prologic IIx, or Dolby Digital EX
- Down-mixing 5.1 channels to two audio channels
- Virtual surround sound effect for 2-channel audio output
- DSP effects (e.g. Concert Hall, Party, etc.)
- Equalizer effects (e.g. Rock, Dance, Techno, Jazz, Classical, Live, Movie, etc.)
- Full speaker settings and bass management
- Audio channel delay
- Gain control
- DC filtering

Depending on the specific application, one or more post-processing modes can be enabled by firmware.

3.3.2 Audio Interfaces

The audio output is implemented via three independent interfaces: I^2S, IEC-958 (S/PDIF) and delta-sigma audio DACs. The IEC958 (S/PDIF) audio interface can outputs a decoded stream or just a pass-through stream from the source (e.g. DTS stream from a DVD-Video disc). The IEC958 interface can be used for both "digital out" and "optical out" signals.

In addition to the digital outputs, the AML8613 chip includes two $\Delta\sum$ audio DACs for low-cost stereo output. $\Delta\sum$ Modulation method is used to generate an internal PWM signal, and then the PWM signal is passed to a pair of multi-stage audio filters for output processing. The audio DAC can drive RCA connection directly, or it needs a simple amplifier to driver speakers.

3.4 Peripherals Interface Architecture

The AML8613 A/V processor can be connected to a variety of peripherals, including USB OTG, card reader interfaces.

3.4.1 USB Interfaces

The AML8613 A/V processor has one built-in USB OTG controller and PHY. The OTG is capable of high-speed (480Mbps) data transfer between external USB host/devices and internal SDRAM. It has built-in DMA engines to handle data transfer with minimal core CPU processing.

The AVOS firmware for AML8613 provides the necessary driver for handling the USB OTG ports. When behaving as an USB host port, the AML8613 can be connected to any external Mass-Storage class USB devices or Picture-Transfer-Protocol (PTP) class USB devices. The USB OTG port can be connected to any PC's or MAC's USB port for file transfer. The AML8613 A/V processor's internal core processor is used to perform higher-level USB protocols, and new functions are being added. Please contact AMLOGIC sales team for more up-to-date information about new additions to the USB protocol stack.

3.4.2Card Reader Interfaces

The AML8613 processor also integrates multiple FLASH memory card controllers and a flexible programmable card controller for interfacing with varies FLASH card standards. Current firmware can support SD/MS/MMC card standards. The AVOS firmware includes device drivers for the card reader controllers and the upper layer file-system drivers.

3.5 Host CPU and System Architecture

3.5.1 Embedded Host CPU

A 333MHz internal (core) RISC CPU is embedded in the AML8613 A/V processor. The processor is a 32-bit RISC CPU with I+D cache structure and MMU. The program can be run from the FLASH or SDRAM interface. Data, BSS and stack are stored in the SDRAM. The internal RISC performs general house keeping functions, user interface and graphic programming and USB protocol stacks. The RISC CPU has a side DSP engine with flexible ALU and MAC to accelerate computation intensive tasks.

3.5.2 Memory Interfaces

The AML8613 A/V processor provides two memory interfaces: SDRAM interface and FLASH interface. The FLASH interface is meant for external storage of executable binaries and graphics on FLASH memory chips. The 4 wire SPI NOR FLASH interface accommodates up to 64M bits of FLASH storage. The 8/16-bits NAND FLASH interface can accommodate more than 1G bytes of storage. The AML8613 can boot from either NOR FLASH or NAND FLASH. The internal FLASH controller has built-in state-machines to work with either types of FLASH and includes all the ECC calculation and DMA mechanism for effective transfer of data between SDRAM and FLASH devices. the AML8613 also supports MLC NAND Flash.

The system SDRAM is used as program memory for the internal RISC processor and the A/V decoder core. it can accommodate up to 32M bytes of SDRAM. In order to optimize the SDRAM memory access, the SDRAM interface module has specific extensions to stream parser, A/V decoding core, video/audio post processors, core RISC processor, DMA engines, USB OTGs and peripheral interfaces. Sophisticated prioritized time sharing algorithm is used arbitrate the SDRAM access between all the internal modules.

3.5.3 Clock and Power Supplies

The AML8613 processor requires one crystal oscillators. One 27MHz external crystal oscillator is used as clock input for the system and decoding operation. It has multiple internal clock circuits (PLLs) to drive all the clocks needed.

The AML8613 device uses 1.2V as its core logic voltage and uses 3.3V power supplies for I/O. The analog devices (PLL, OTG PHY and VDAC) need to have isolated/filtered power/ground supplies as specified by in the pin list.

The AML8613 device and firmware implement the AMPOWER-II algorithm to reduce power consumption for portable applications and to reduce heat generation for traditional A/V applications. Depending on the application, the system dynamically enables/disables clocking on each module and varies its operating frequency between 27MHz and 166MHz to optimize the system performance. In addition, the system intelligently turns on/off different subsystems to conserve power consumption.

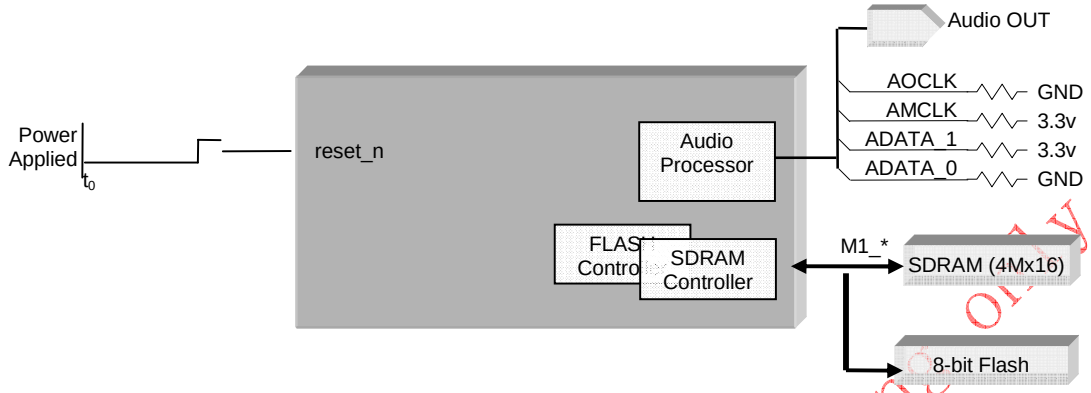
4. External Interfaces

4.1.1 Reset Configuration

The chip has a common active-low reset signal called *reset_n*. This signal puts the entire chip into a known state by resetting internal registers and state-machines to their default states. Typically this signal is held low for at least 100 millisecond after the power is applied and has stabilized. The reset process also plays a role in configuring certain functions within the chip. Using the state of the AUDIO pins and the rising edge of the *reset_n* signal, the user can dictate the configuration of the DRAM controller and the boot address in shared flash configurations. The AUDIO pins should be pulled up or down using 10k resistors to either 3.3v or ground.

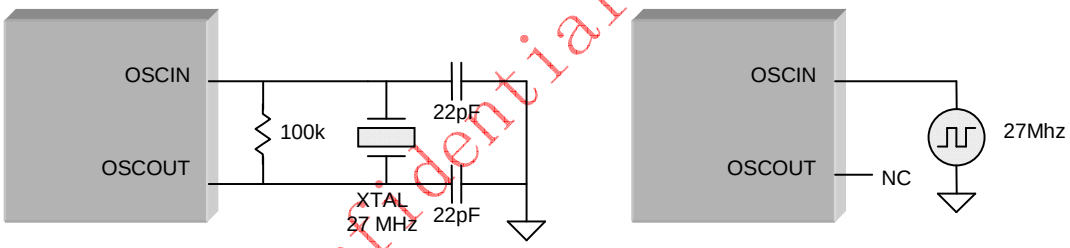
PIN	Function
m1_a_11	SPI BOOT LOCATION: If this bit is set to 1, then the SPI flash is connected to m1_d[3:0]. If this bit is set to 0, then the SPI boots from the NAND pins: GPIOA_13, NAND_we_n, NAND_rdy_bsy, NAND_ce_n, NAND_rd_n
m1_cas_n	NAND FLASH PAGE SIZE CONFIGURATION: This pin controls the page size of the NAND FLASH. Tie to 3.3v with 10k resistor when the NAND FLASH has a 2048 bytes page size. Tie to ground with a 10k resistor for NAND FLASH that has 512 bytes page size.
m1_ras_n	NAND FLASH SIZE CONFIGURATION: This pin controls the number of ALE pulses for controlling the NAND FLASH. Tie to 3.3v with 10k resistor when 3 ALE pulses are needed to set the NAND row address. This is usually needed for larger size NAND FLASH chips. Tie to ground with a 10k resistor when 2 ALE pulses are needed to set the NAND row address.
m1_we_n	BOOT OPTION CONFIGURATION: This pin controls if the chip is booting from NAND or NOR FLASH. Tie to 3.3v with 10k resistor to select NAND boot. Tie to ground with a 10k resistor to select NOR boot.
m1_a_10	JTAG CONFIGURATION: This pin controls the JTAG configuration after RESET: Tie to 3.3v with 10k resistor indicates the JTAG pins are used for communicating with CPU Tie to ground with a 10k resistor to use the JTAG pins as GPIO
m1_ba1	Tie to 3.3v with 10k resistor
m1_ba0	NAND FLASH LOCATION CONFIGURATION: This pin controls the location of NAND FLASH chip for booting. Note the NAND FLASH can only boot from SDRAM1. Tie to 3.3v with 10k resistor indicates NAND FLASH is connected to m1_* pins
m1_dqm1	Tie to 3.3v with 10k resistor for 16-bit NAND FLASH interface Tie to ground with a 10k resistor for 8-bit NAND FLASH device interface

Example:
The following example illustrates a start-up configuration for a single 8M bytes SDRAM1 and 8-bit FLASH memory during a production environment (i.e. no JTAG debugging).



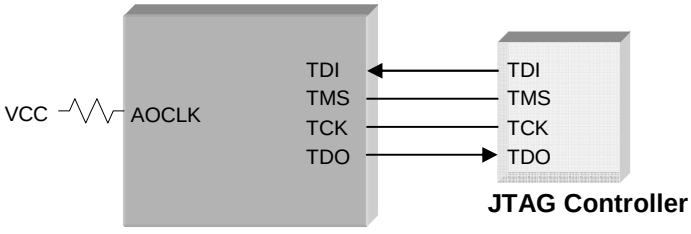
4.1.2 Clocks

The AML8613 has multiple internal clock domains, but all the internal clock domains are derived from a single external reference: *OSC*. As illustrated below, the crystal/oscillator pin pairs (OSCIN/OSCOUT) can be connected to a crystal or driven from an external oscillator. In the typical A/V application, a 27 MHz crystal is connected to the *OSC* pins. The following diagram depicts a typical crystal circuit; the actual values of the components depend on the type of crystal used in the application.



4.1.3 JTAG for Software Development

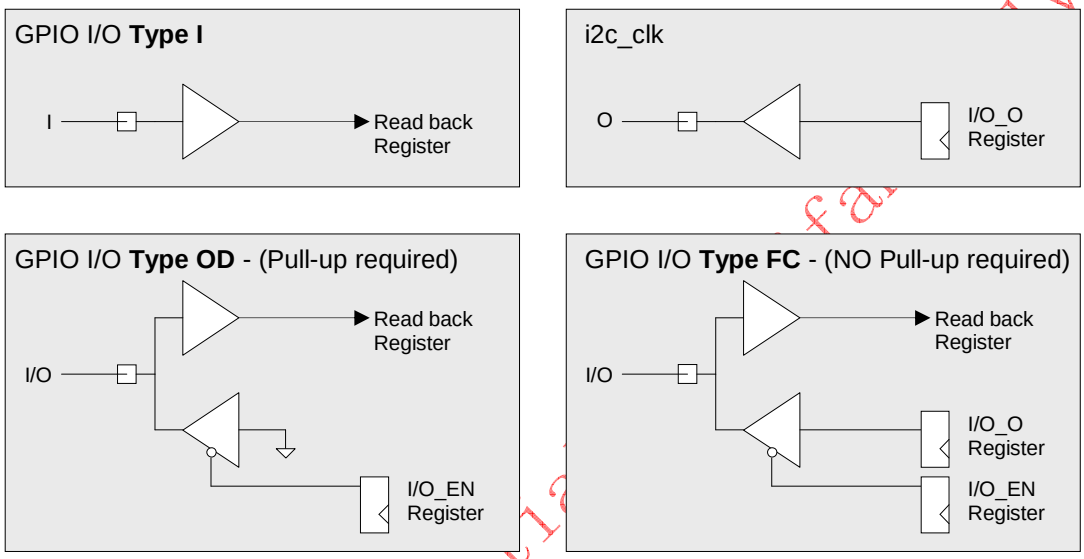
The embedded core processor can be controlled through its JTAG port using the embedded ICE interface. The embedded ICE interface allows the developer to download code/data to the SDRAM memory, probe registers on the AML8613 chip, execute and debug the RISC code using a user friendly development environment. The JTAG interface is enabled by tying *AOCLK* high as illustrated below.



4.1.4 GPIOs

Configurable hardware controllers (e.g. i2c, RS232, VFD, etc.) and DMAs are integrated into the AML8613 device to speed up the common operations and relieve the core RISC for user-level applications. Since hardware controllers and state-machines cannot cover all possible external devices or system-level signals, numerous general-purpose I/O pins are available on the chip for purpose like Portable Media Player keypads. Each GPIO pin can be independently configured to be an input or an output. As indicated in the diagram, there are various I/O types.

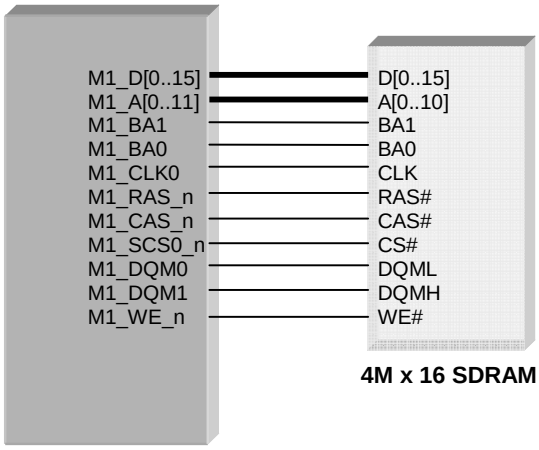
GPIO PAD TYPES



4.2 Memory Interfaces

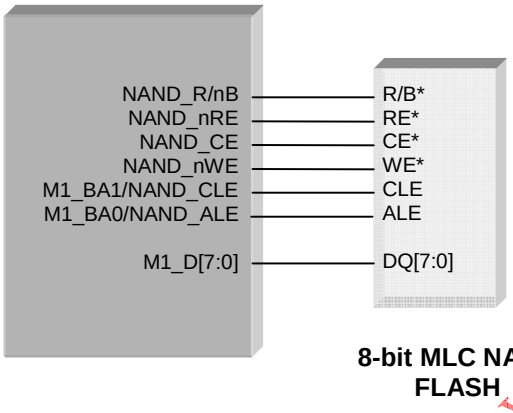
4.2.1 SDRAM Interface

The AML8613 device uses external SDRAM for data storage and code execution. The SDRAM interface is labeled as *m1_** interface. SDRAM interface can access up to 32M bytes of memory. Depending on the application, either 133MHz or 166MHz SDRAM chips can be used. The following example depicts a system with only 8M bytes of SDRAM on *m1_** interface.



4.2.2 NAND FLASH Interface

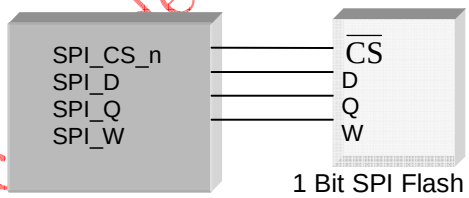
The NAND FLASH interface can accommodate an 8-bits or 16-bits NAND FLASH device. Due to the limited number of I/O pins, the FLASH interface is shared with the SDRAM (m1_*) interface. NAND FLASH has a very large capacity that ranges from 32MB to more than 1GB. The NAND FLASH should be connected as indicated in the following diagram:



8-bit MLC NAND FLASH

4.2.3 SPI NOR FLASH Interface

The SPI NOR FLASH interface can accommodate 1-bit, 2-bit and 4-bit SPI NOR FLASH devices. Up to 8M bytes of NOR FLASH is accessible with the SPI FLASH interface design. The FLASH should be connected as indicated in the following diagram:



1 Bit SPI Flash

4.3 Audio Interfaces

The audio output interface is composed of three independent interfaces: I^2S, IEC-958 (S/PDIF) and analog DAC output.

The IEC958 audio output interface can send compressed data or uncompressed PCM data to external audio device. For example, compressed audio data can be sent to an external Dolby/DTS decoder, and uncompressed PCM data can be sent to a digital audio recording device such as a DAT or minidisk recorder.

Two sigma-delta audio DACs are integrated into the AML8613 chip for low-cost audio solution. The two internal DACs can generate high quality stereo audio output without any external DAC chip. Also, an analog audio filter is integrated for direct connection to RCA jacks.

The audio input pin is provided so that an external audio source such as a microphone can be digitized and mixed with other audio sources.

4.3.1 I²S Audio Output Interface

I²S output interface is used to communicate directly with audio DACs. The 16, 20 and 24-bit resolution DACs are supported. The PCM data can be configured to be either signed or offset binary with the MSB first or last. The audio interface provides "on-the-fly" control commands for L/R channel swap individually for each DAC, stereo to mono conversion, and individual speaker mute controls.

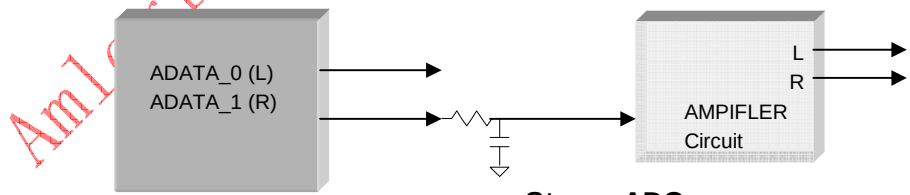
4.3.2 IEC-958 / SPDIF Audio Output

IEC-958 is a consumer version of the AES/EBU-interface that supersedes AES/EBU, as well as S/PDIF. The two formats are quite compatible with each other, differing only in the sub-code information and connector. IEC-958 interface is designed to communicate either to an external AC-3 decoder, or to a device that expects PCM data encoded over the IEC-958 protocol standard interface. IEC958 is supported using a single output pin. This output pin may be also used to drive a differential driver in cases where common mode rejection is required.

4.3.3 Stereo Audio DAC Output

The AML8613 A/V processor implements two internal audio DACs for stereo audio output. The audio DACs are designed for connecting to internal TV audio sub-system or small speaker or ear buds for portable devices. A simple external filter amplifier is needed. Please see the following sample filter diagram.

Internally, the delta-sigma algorithm is used to improve the performance and ensure high SNR output. The implementation includes a multi-tap interpolation filter which increases the sample rate of the audio channels to the modulator rate. Then the audio stream is passed through a sigma-delta modulator that generates the serial PWM data stream. An external analog filter is then used for out-of-band noise filtering and analog signal reconstruction. External amplifier is needed to provide the necessary current to drive the speakers. Connections to RCA jacks do not need external amplifier chips.



Stereo ADC
CS5331 or equiv.

4.4 Video Output Interfaces

4.4.1 Analog Video Output

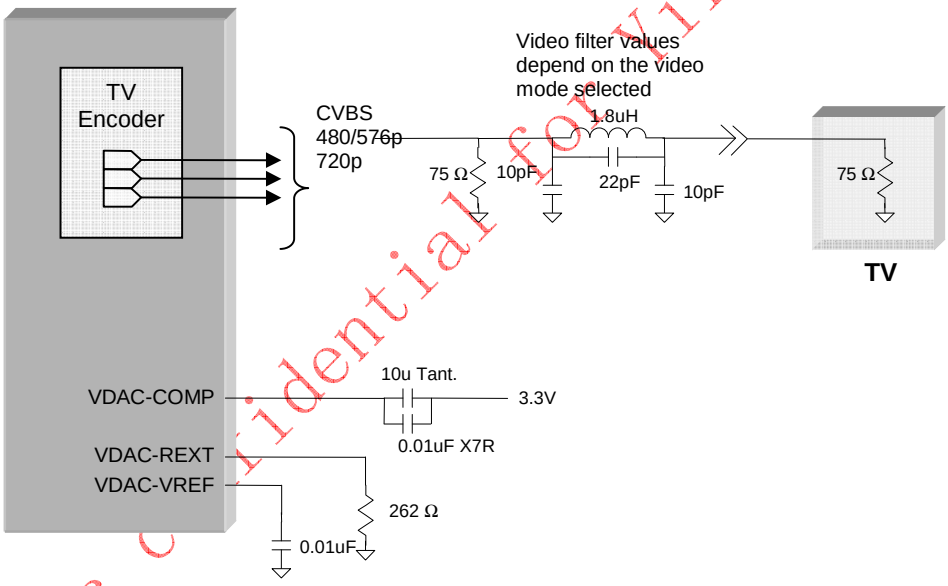
The AML8613 integrated internal video encoder and high resolution tri-video DACs for optimal analog video output. The video encoder is capable of both progressive and interlaced video output. The high frequency, high resolution video DAC can support from NTSC video to 720p output frequency.

For the interlaced mode, the video encoder has Luma and Chroma bandwidth control, programmable saturation, hue, contrast and brightness and includes Macrovision 7.1 copy protection schemes. When configured for progressive scan output, the video DACs are programmed to output Y, Pb and Pr with Macrovision AGC copy protection.

The video DAC outputs are fully programmable and support the following output format using composite video, and component Y/Pb/Pr(YUV) video:

- Progressive HDTV: 720px50/60fps,
- Interlaced NTSC: 720x480x30fps
- Interlaced PAL: 720x576x25fps
- Progressive NTSC: 720x480px60fps
- Progressive PAL: 720x576px50fps

The video DACs use a standard doubly terminated scheme as indicated below; depending on the application, different video output filters can be applied, please consult the AMLOGIC Sales staffs for more information.



4.5 Peripherals

Card-Reader Interface

The AML8613 have an integrated hardware controller for card-reader operations. The hardware controller is programmable so it can be extended to work with new memory card formats. The hardware controller is capable of executing the low-level card interface protocols, computing the CRC or checksum, and transferring data to/from SDRAM. The hardware provides interface for the necessary signals (e.g. SD_CLK, SD_CMD, SD_D[0..3] for SD cards) but signals like card detect and write-protect are provided using GPIO only.

5. Operating Conditions

5.1DC Characteristics

Table 51 DC Characteristics

V_{DD} = 3.3 +/- 0.3V, T_A = 0 to 75°C

Symbol	Parameters	Condition	Min	Typ	Max	Unit
V_{IH}	High Level Input		2.0		3.3	V
V_{IL}	Low Level Input		-0.3		0.8	V
VT+	Schmitt trigger, positive going Threshold			1.5		V
VT-	Schmitt trigger, negative going threshold			0.93		
Voh	High-level output voltage	Ioh = -2.0mA to 24mA	2.4			V
Vol	Low-level output voltage	Iol = 2.0 mA to 24mA			0.4	V
I_{IH}	High-level input current	Vin = V_{DD}		10nA	1	uA
I_{IL}	Low-level input current			10nA	1	
Ioz	Tri-state output leakage current			10nA	1	
P_D	Power Dissipation	Vin = V_{DD}		0.8		W

5.2Absolute Maximum Ratings

The table below gives the absolute maximum ratings. Exposure to stresses beyond those listed in this table may result in permanent device damage, unreliability or both.

Table 52 Absolute Maximum Ratings

Characteristic	Value	Unit
1.2V Core Supply Voltage	1.5	V
3.3V Pads Supply Voltage	3.8	V
Input voltage, V_I	-0.5 ~ 4.6	V
Output voltage, V_O	-0.5 ~ 4.6	V
Operating Temperature	70	℃

5.3Recommended Operating Conditions

Table 53 Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max	Unit
$V_{DD(CORE)}$	1.2V Core Supply Voltage	1.00	1.2	1.5	V
$V_{DD(PADS)}$	3.3V Pads Supply Voltage	3.0	3.3	3.6	V
T_J	Junction Temperature	0		125	℃

6. Pin-out

6.1 Pin-out information

The AML8613 A/V processor pin-out is described in the following table.

Abbreviations:
I == Input digital pin
O == Output digital pin
I/O == Input/Output pin
AI == Analog input pin
AO == Analog output pin
AIO == Analog input/output pin
P == Power pin
AP == Analog power pin
NC == No connection

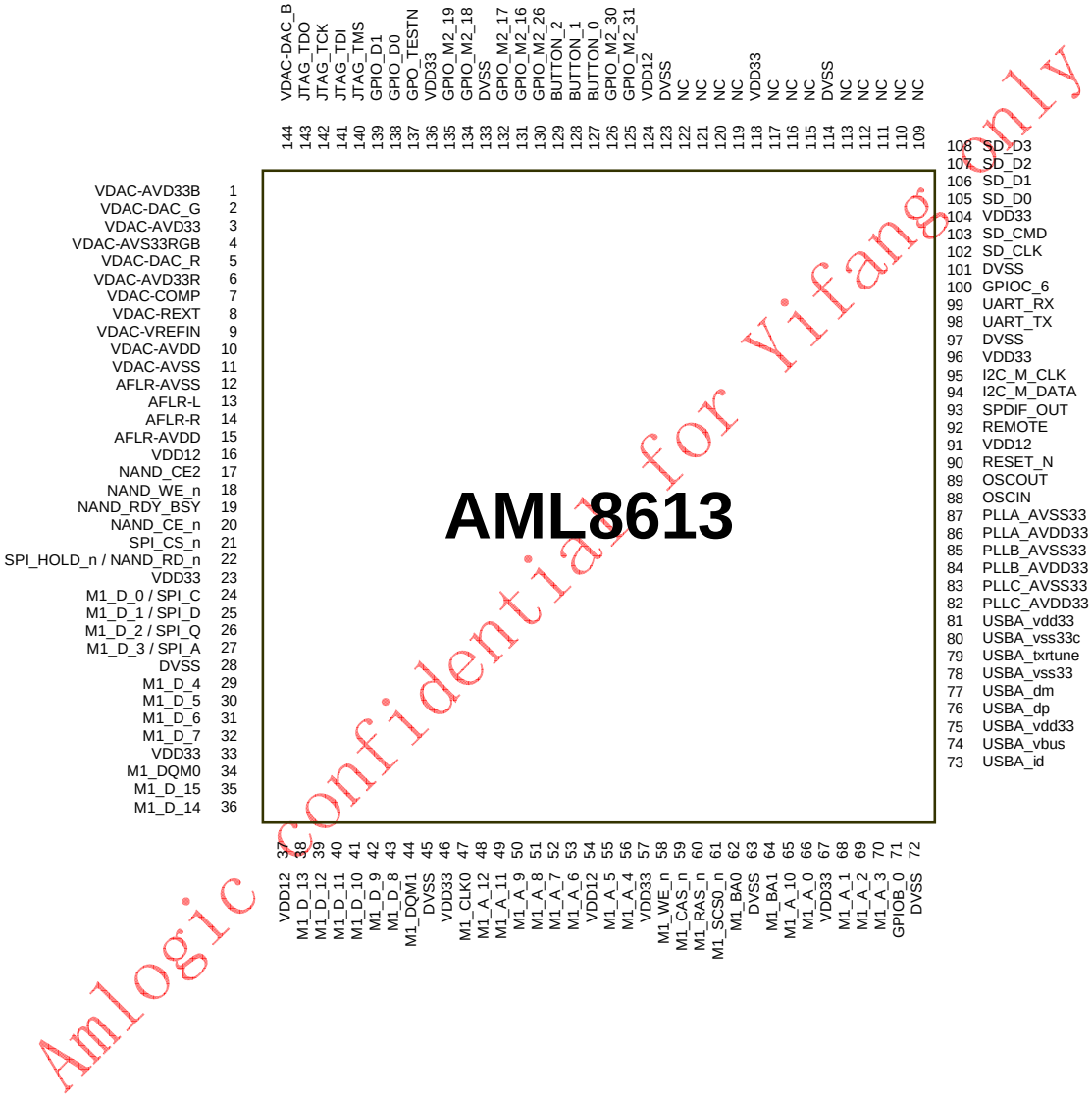
Pin #	Package Pin Name	GPIO	M1/JTAG	SPI/I2C/Audio/CARD	NAND/I2C	UART
1	VDAC-AVD33B		VDAC-AVD33B			
2	VDAC-DAC_G		VDAC-DAC_G			
3	VDAC-AVD33		VDAC-AVD33G			
4	VDAC-AVS33RGB		VDAC-AVS3B			
5	VDAC-DAC_R		VDAC-DAC_R			
6	VDAC-AVD33R		VDAC-AVD33R			
7	VDAC-COMP		VDAC-COMP			
8	VDAC-REXT		VDAC-REXT			
9	VDAC-VREFIN		VDAC-VREFIN_OUT			
10	VDAC-AVDD		VDAC-AVDD			
11	VDAC-AVSS		VDAC-AVSS			
12	AFLR-AVSS					
13	AFLR-L					
14	AFLR-R					
15	AFLR-AVDD					
16	VDD12					
17	NAND_CE2	GPIOA_13			NAND_CE2_n	
18	NAND_WE_n	GPIOA_14			NAND_WE_N	
19	NAND_RDY_BSY	GPIOA_15			NAND_RDY_BSY	
20	NAND_CE_n	GPIOA_16			NAND_CE_N	
21	SPI_CS_n			SPI_CS_n_A		
22	SPI_HOLD_n / NAND_RD_n			SPI_HOLD_n_A	NAND_RD_n	
23	VDD33					
24	M1_D_0 / SPI_C		M1_D_0	SPI_C_A	NAND_IO_0	
25	M1_D_1 / SPI_D		M1_D_1	SPI_D_A	NAND_IO_1	
26	M1_D_2 / SPI_Q		M1_D_2	SPI_Q_A	NAND_IO_2	
27	M1_D_3 / SPI_A		M1_D_3	SPI_W_A	NAND_IO_3	
28	DVSS					
29	M1_D_4		M1_D_4		NAND_IO_4	
30	M1_D_5		M1_D_5		NAND_IO_5	
31	M1_D_6		M1_D_6		NAND_IO_6	

32	M1_D_7		M1_D_7		NAND_IO_7	
33	VDD33					
34	M1_DQM0		M1_DQM0			
35	M1_D_15		M1_D_15		NAND_IO_15	
36	M1_D_14		M1_D_14		NAND_IO_14	
37	VDD12					
38	M1_D_13		M1_D_13		NAND_IO_13	
39	M1_D_12		M1_D_12		NAND_IO_12	
40	M1_D_11		M1_D_11		NAND_IO_11	
41	M1_D_10		M1_D_10		NAND_IO_10	
42	M1_D_9		M1_D_9		NAND_IO_9	
43	M1_D_8		M1_D_8		NAND_IO_8	
44	M1_DQM1		M1_DQM1			
45	DVSS					
46	VDD33					
47	M1_CLK0		M1_CLKO			
48	M1_A_12		M1_A_12			
49	M1_A_11		M1_A_11			
50	M1_A_9		M1_A_9			
51	M1_A_8		M1_A_8			
52	M1_A_7		M1_A_7			
53	M1_A_6		M1_A_6			
54	VDD12					
55	M1_A_5		M1_A_5			
56	M1_A_4		M1_A_4			
57	VDD33					
58	M1_WE_n		M1_WE_n			
59	M1_CAS_n		M1_CAS_n			
60	M1_RAS_n		M1_RAS_n			
61	M1_SCS0_n		M1_SCS0_n			
62	M1_BA0		M1_BA0		NAND_ALE	
63	DVSS					
64	M1_BA1		M1_BA1		NAND_CLE	
65	M1_A_10		M1_A_10			
66	M1_A_0		M1_A_0			
67	VDD33					
68	M1_A_1		M1_A_1			
69	M1_A_2		M1_A_2			
70	M1_A_3		M1_A_3			
71	GPIOB_0	GPIOB_0				
72	DVSS					
73	USBA_id		USB			
74	USBA_vbus		USB			
75	USBA_vdd33		USB			
76	USBA_dp		USB			
77	USBA_dm		USB			
78	USBA_vss33		USB			
79	USBA_txrtune		USB			
80	USBA_vss33c		USB			
81	USBA_vdd33		USB			
82	PLLC_AVDD33		PLL			

83	PLLC_AVSS33		PLL			
84	PLLB_AVDD33		PLL			
85	PLLB_AVSS33		PLL			
86	PLLA_AVDD33		PLL			
87	PLLA_AVSS33		PLL			
88	OSCIN		OSCIN			
89	OSCOUT		OSCOUT			
90	RESET_N					
91	VDD12					
92	REMOTE	GPIOC_0	REMOTE_IN	I2C_S_DATA		UART_TX
93	SPDIF_OUT	GPIOC_1	SPDIF_OUT	I2C_S_CLK		UART_RX
94	I2C_M_DATA	GPIOC_2	I2C_M_DATA	I2C_S_DATA		UART_TX
95	I2C_M_CLK	GPIOC_3	I2C_M_CLK	I2C_S_CLK		UART_RX
96	VDD33					
97	DVSS					
98	UART_TX	GPIOC_4	PWM_A	I2C_M_DATA	I2C_S_DATA	UART_TX
99	UART_RX	GPIOC_5	PWM_B	I2C_M_CLK	I2C_S_CLK	UART_RX
100	GPIOC_6	GPIOC_6				
101	DVSS					
102	GPIOC_15	GPIOC_15		SD_CLK		
103	GPIOC_16	GPIOC_16		SD_CMD		
104	VDD33					
105	GPIOC_17	GPIOC_17		SD_D0		
106	GPIOC_18	GPIOC_18		SD_D1		
107	GPIOC_19	GPIOC_19		SD_D2		
108	GPIOC_20	GPIOC_20		SD_D3		
109	NC					
110	NC					
111	NC					
112	NC					
113	NC					
114	DVSS					
115	NC					
116	NC					
117	NC					
118	VDD33					
119	NC					
120	NC					
121	NC					
122	NC					
123	DVSS					
124	VDD12					
125	GPIO_M2_31	GPIO_M2_31				
126	GPIO_M2_30	GPIO_M2_30				
127	BUTTON_0	BUTTON_0				
128	BUTTON_1	BUTTON_1				
129	BUTTON_2	BUTTON_2				
130	GPIO_M2_26	GPIO_M2_26				
131	GPIO_M2_16	GPIO_M2_16				
132	GPIO_M2_17	GPIO_M2_17				
133	DVSS					

134	GPIO_M2_18	GPIO_M2_18				
135	GPIO_M2_19	GPIO_M2_19				
136	VDD33					
137	GPO_TESTN			SPDIF		
138	GPIO_D0					
139	GPIO_D1			ADATA0		
140	JTAG_TMS		JTAG_TMS	AMCLK		
141	JTAG_TDI		JTAG_TDI	AOCLK		
142	JTAG_TCK		JTAG_TCK	ALRCLK		
143	JTAG_TDO		JTAG_TDO			
144	VDAC-DAC_B		VDAC-DAC_B			

7. Pin-Out Diagram



8. Mechanical Specifications

The AML8613 A/V processor is packaged using a 144 pin LQFP package. The mechanical dimensions are given in millimeters as below: