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| SHEET | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | | | | |

| REV STATUS OF SHEETS | REV | | | | | | | | | | | | | | |
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| | SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |

PMIC N/A

**STANDARD MICROCIRCUIT DRAWING**

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Thomas M. Hess

CHECKED BY
Thomas M. Hess

APPROVED BY
Thomas M. Hess

DRAWING APPROVAL DATE
95-06-12

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, RADIATION HARDENED, 1750 CHIP SET, MULTICHIP MICROCIRCUIT, SILICON

| SIZE | CAGE CODE | 5962-94667 |
|---|---|---|
| A | 67268 | |

SHEET 1 OF 29

DESC FORM 193
JUL 94

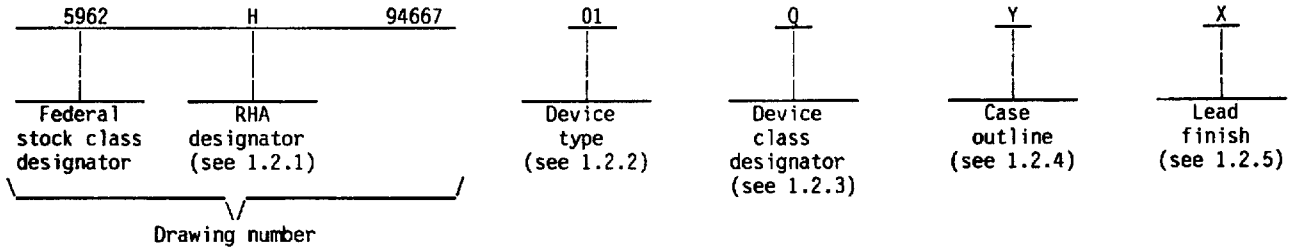


5962-E214-95

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:




1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

| Device type | Generic number | Circuit function | Minimum operating period | Propagation delay, HCLK to DOUTENA |
|---|---|---|---|---|
| 01 | RH-1750 | Microprocessor, multichip module (MCM) | 40 ns max | 8.0 ns to 33 ns |
| 02 | RH-1750 | Microprocessor, multichip module (MCM) | 55 ns max | 8.0 ns to 33 ns |
| 03 | RH-1750 | Microprocessor, multichip module (MCM) | 55 ns max | 8.0 ns to 36 ns |
| 04 | RH-1750 | Microprocessor, multichip module (MCM) | 50 ns max | 8.0 ns to 33 ns |

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

| Device class | Device requirements documentation |
|---|---|
| M | Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883 |
| Q or V | Certification and qualification to MIL-I-38535 |

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

| Outline letter | Descriptive designator | Terminals | Package style |
|---|---|---|---|
| Y | see figure 1 | 200 | Quad flat package |

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/ 2/

| | |
|---|---|
| Supply voltage range ($V_{DD}$) | -0.5 V dc to +7.0 V dc |
| DC input voltage range ($V_{IN}$) | -0.5 V dc to $V_{DD}$ + 0.5 V dc |
| DC output voltage range ($V_{OUT}$) | -0.5 V dc to $V_{DD}$ + 0.5 V dc |
| DC input current ($I_{IN}$) 3/ | ±50 mA |
| DC output current ($I_{OUT}$) 4/ | ±50 mA |
| Output voltage applied in high impedance state | -0.5 V dc to $V_{DD}$ + 0.5 V dc |
| Power dissipation ($P_D$) | 4.87 W (peak) |
| Lead temperature (soldering, 5 seconds) | +270°C |
| Maximum junction temperature ($T_J$) | +150°C |
| Thermal resistance, junction-to-case ($\theta_{JC}$) | 1.0°C/W |
| Storage temperature range | -65°C to +150°C |

1.4 Recommended operating conditions. 2/

| | |
|---|---|
| Supply voltage range ($V_{DD}$) | 4.5 V dc to 5.0 V dc |
| DC input voltage range ($V_{IN}$) | -0.3 V dc to $V_{DD}$ + 0.3 V dc |
| DC output voltage range ($V_{OUT}$) | -0.3 V dc to $V_{DD}$ + 0.3 V dc |
| DC input current ($I_{IN}$) 3/ | ±10 mA |
| DC output current ($I_{OUT}$) 4/ | ±12 mA |
| Capacitive output load ($C_L$) 5/ | 50 pF |
| Case operating temperature range ($T_C$) | -55°C to +125°C |

1.5 Digital logic testing for device classes Q and V.

| | |
|---|---|
| Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012) | 98.4 percent |

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-H-38534 - Hybrid Microcircuits, General Specification for.
MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ All voltages are with respect to $V_{SS}$ terminal and $T_C$ = -55°C to +125°C, unless otherwise specified.
3/ High impedance (input or output in three-state), driver or receiver type = input, output, or bidirectional.
4/ Low impedance (enabled), driver or receiver type = output or bidirectional.
5/ f = 20 MHz, no dc load, driver or receiver type = output or bidirectional 12 mA, maximum capacitance scales with inverse of frequency, $V_{DD}$ = 4.5 V dc.

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-88 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

ELECTRONICS INDUSTRY ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standarized Test Procedure for the Characterization of Latch-up in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2001 Pennsylvania Street, N.W., Washington, DC 20006.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The element evaluation for passive components shall be in accordance with MIL-H-38534 and as specified herein. The modification in the QM plan shall not effect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Switching test circuit and waveforms. The switching test circuit and waveforms shall be as specified on figure 4.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be maintained and made available from the vendor.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and table IB and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

TABLE IA. Electrical performance characteristics.

| Test | Symbol | Conditions 1/ 2/<br>$-55°C \le T_C \le +125°C$<br>$4.5\ V \le V_{DD} \le 5.5\ V$<br>unless otherwise specified | Group A subgroups | Device types | Limits | | Units |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| High level input threshold voltage 3/ | $V_{IH}$ | $V_{DD}$ = 5.5 V | 1, 2, 3 | All | | 3.85 | V |
| Low level input threshold voltage 3/ | $V_{IL}$ | $V_{DD}$ = 4.5 V | 1, 2, 3 | All | 1.35 | | V |
| High level input current | $I_{IH}$ | $V_{DD}$ = 5.5 V, $V_{IH}$ = $V_{DD}$ | 1, 2, 3 | All | | 10 | µA |
| Low level input current | $I_{IL}$ | $V_{DD}$ = 5.5 V, $V_{IL}$ = $V_{SS}$ | 1, 2, 3 | All | -10 | | µA |
| High level output voltage, NFTDOUTN output only 4/ | $V_{OH1}$ | $V_{DD}$ = 4.5 V, $I_{OH}$ = -9.0 mA | 1, 2, 3 | All | 4.0 | | V |
| High level output voltage, all outputs except NFTDOUTN 4/ | $V_{OH2}$ | $V_{DD}$ = 4.5 V, $I_{OH}$ = -12 mA | 1, 2, 3 | All | 4.0 | | V |
| Low level output voltage, NFTDOUTN output only | $V_{OL1}$ | $V_{DD}$ = 4.5 V, $I_{OL}$ = 9.0 mA | 1, 2, 3 | All | | 0.5 | V |
| Low level output voltage, all outputs except NFTDOUTN | $V_{OL2}$ | $V_{DD}$ = 4.5 V, $I_{OL}$ = 12 mA | 1, 2, 3 | All | | 0.5 | V |
| High level output current, NFTDOUTN output only 4/ | $I_{OH1}$ | $V_{DD}$ = 5.5 V, $V_{OH}$ = 4.0 V | 1, 2, 3 | All | -9.0 | | µA |
| High level output current, all outputs except NFTDOUTN 4/ | $I_{OH2}$ | $V_{DD}$ = 5.5 V, $V_{OH}$ = 4.0 V | 1, 2, 3 | All | -12 | | µA |
| Low level output current, NFTDOUTN output only | $I_{OL1}$ | $V_{DD}$ = 5.5 V, $V_{OL}$ = 0.5 V | 1, 2, 3 | All | | 9.0 | µA |
| Low level output current, all outputs except NFTDOUTN | $I_{OL2}$ | $V_{DD}$ = 5.5 V, $V_{OL}$ = 0.5 V | 1, 2, 3 | All | | 12 | µA |
| Three-state high level output leakage current | $I_{OZH}$ | $V_{DD}$ = 5.5 V, $V_{OH}$ = 5.5 V | 1, 2, 3 | All | -18 | | µA |
| Three-state low level output leakage current | $I_{OZL}$ | $V_{DD}$ = 5.5 V, $V_{OL}$ = 0.0 V | 1, 2, 3 | All | | 18 | µA |
| Quiescent supply current | $I_{DDSB}$ | $V_{DD}$ = 5.5 V, $f_C$ = 0 Hz | 1, 2, 3 | All | | 100 | mA |
| Operating supply current | $I_{DD}$ | $V_{DD}$ = 5.5 V, $f_C$ = 16.6 MHz | 1, 2, 3 | 01, 04 | | 325 | mA |
| | | | | 02, 03 | | 300 | |

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - continued.

| Test | Symbol | Conditions 1/ 2/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{DD} \le 5.5\ V$, unless otherwise specified | Group A subgroups | Device types | Limits | | Units |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| High level output ground bounce voltage 5/ | $V_{GBH}$ | $V_{IL}$ = 0.0 V, $V_{IH}$ = $V_{DD}$ | 1, 2, 3 | All | | 0.1 | V |
| Low level output ground bounce voltage 5/ | $V_{GBL}$ | $V_{IL}$ = 0.0 V, $V_{IH}$ = $V_{DD}$ | 1, 2, 3 | All | | 0.3 | V |
| Input capacitance | $C_{IN}$ | $V_{IN}$ = 0 V, f = 1.0 MHz, see 4.5.1c | 4, 5, 6 | All | | 9.0 | pF |
| Output capacitance | $C_{OUT}$ | $V_{OUT}$ = 0 V, f = 1.0 MHz, see 4.5.1c | 4, 5, 6 | All | | 14 | pF |
| Functional test per approved vector set 6/ | | $V_{IL}$ = 0.0 V, $V_{IH}$ = $V_{DD}$, see 4.5.1b | 7, 8A, 8B | All | | | pass |
| Minimum operating period | $t_{MIN}$ | | 9, 10, 11 | 01 | | 40 | ns |
| | | | | 02, 03 | | 55 | |
| | | | | 04 | | 50 | |
| Output rise and fall times 5/ 7/ | $t_{ro}$, $t_{fo}$ | $C_L$ = 60 pF | 9, 10, 11 | All | | 2.5 | ns |
| Propagation delay time, HCLK to PIO | $t_{PLH3}$, $t_{PHL3}$ | $V_{IL}$ = 0.0 V, $V_{IH}$ = $V_{DD}$, see figure 4 | 9, 10, 11 | All | 8.0 | 36 | ns |
| Propagation delay time, HCLK to DOUTENA | $t_{PLH4}$, $t_{PHL4}$ | | 9, 10, 11 | 01, 02, 04 | 8.0 | 33 | ns |
| | | | | 03 | 8.0 | 36 | |
| Propagation delay time, HCLK to CPUPARITY | $t_{PLH6}$, $t_{PHL6}$ | | 9, 10, 11 | All | 10.8 | 43 | ns |
| Propagation delay time, HCLK to CPUWDATAn | $t_{PLH9}$, $t_{PHL9}$ | | 9, 10, 11 | All | 8.4 | 32.9 | ns |
| Propagation delay time, HCLK to WRITE | $t_{PLH10}$, $t_{PHL10}$ | | 9, 10, 11 | All | 7.0 | 48 | ns |
| Propagation delay time, HCLK to SIOE | $t_{PLH12}$ | | 9, 10, 11 | All | 9.0 | 42 | ns |
| | $t_{PHL12}$ | | 9, 10, 11 | All | 10 | 40 | ns |
| Propagation delay time, HCLK to READ | $t_{PLH13}$, $t_{PHL13}$ | | 9, 10, 11 | All | 7.0 | 38 | ns |
| Propagation delay time, HCLK to LINSTF | $t_{PLH15}$, $t_{PHL15}$ | | 9, 10, 11 | All | 9.5 | 37.7 | ns |

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - continued.

| Test | Symbol | Conditions 1/ 2/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified | Group A subgroups | Device types | Limits | | Units |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Propagation delay time, HCLK to LRMW | $t_{PLH17}$, $t_{PHL17}$ | $V_{IL} = 0.0\ V$, $V_{IH} = V_{DD}$, see figure 4 | 9, 10, 11 | All | 7.0 | 33 | ns |
| Propagation delay time, HCLK to CPUADDRn | $t_{PLH18}$, $t_{PHL18}$ | | 9, 10, 11 | All | 8.8 | 34.5 | ns |
| Propagation delay time, HCLK to SYSCLKDn | $t_{PLH19}$, $t_{PHL19}$ | | 9, 10, 11 | All | 5.5 | 27.5 | ns |
| Propagation delay time, HCLK to DMAGRNT | $t_{PLH21}$, $t_{PHL21}$ | | 9, 10, 11 | All | 10.1 | 37.2 | ns |
| Propagation delay time, HCLK to SCPE02 | $t_{PLH23}$, $t_{PHL23}$ | | 9, 10, 11 | All | 10 | 90 | ns |
| Propagation delay time, HCLK to SCPE03 | $t_{PLH24}$, $t_{PHL24}$ | | 9, 10, 11 | All | 10 | 90 | ns |
| Propagation delay time, HCLK to BNK0 | $t_{PLH25}$, $t_{PHL25}$ | | 9, 10, 11 | All | 9.1 | 32.6 | ns |
| Propagation delay time, HCLK to BNK1 | $t_{PLH26}$, $t_{PHL26}$ | | 9, 10, 11 | All | 9.1 | 32.6 | ns |
| Propagation delay time, HCLK to BNK2 | $t_{PLH27}$, $t_{PHL27}$ | | 9, 10, 11 | All | 9.1 | 32.6 | ns |
| Setup time, HCLK to READDATAn | $t_{su5}$ | | 9, 10, 11 | All | | 5.0 | ns |
| Setup time, HCLK to LACKN | $t_{su6}$ | | 9, 10, 11 | All | | 9.5 | ns |
| Setup time, HCLK to READDATAP1 | $t_{su7}$ | | 9, 10, 11 | All | | 1.0 | ns |
| Setup time, HCLK to READDATAP2 | $t_{su8}$ | | 9, 10, 11 | All | | 1.0 | ns |
| Setup time, HCLK to DMARQST | $t_{su20}$ | | 9, 10, 11 | All | | 0 | ns |
| Hold time, HCLK to READDATAn | $t_{h5}$ | | 9, 10, 11 | All | | 13 | ns |
| Hold time, HCLK to LACKN | $t_{h6}$ | | 9, 10, 11 | All | | 9.0 | ns |
| Hold time, HCLK to READDATAP1 | $t_{h7}$ | | 9, 10, 11 | All | | 13 | ns |
| Hold time, HCLK to READDATAP2 | $t_{h8}$ | | 9, 10, 11 | All | | 13 | ns |
| Output enable time, CPU3MEN to CPUADDRn | $t_{PLZ1}$ | | 9, 10, 11 | All | | 18 | ns |

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - continued.

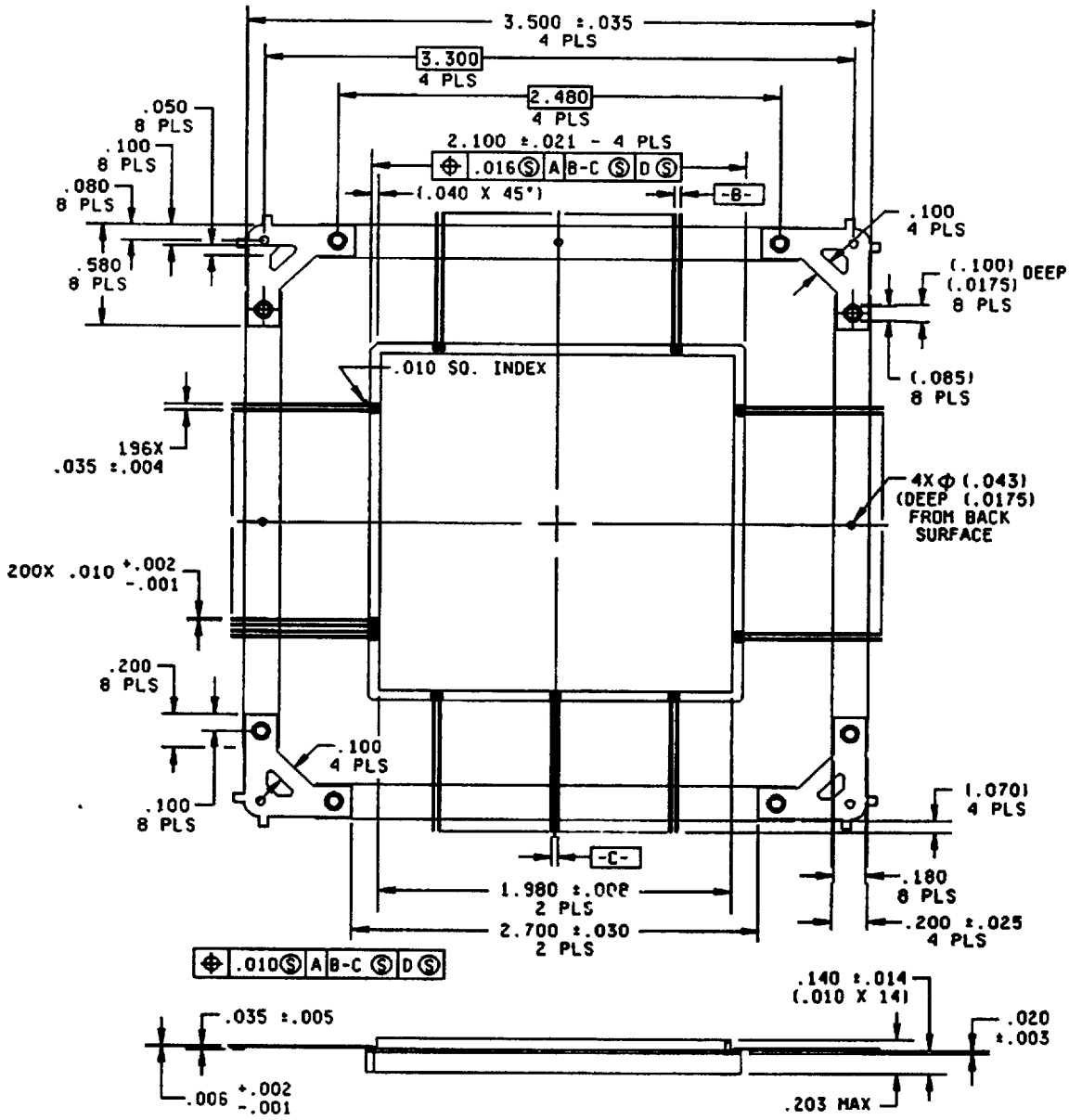
| Test | Symbol | Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified | Group A subgroups | Device types | Limits | | Units |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Output disable time, CPU3MEN to CPUADDRn | $t_{PZL1}$ | $V_{IL}$ = 0.0 V, $V_{IH} = V_{DD}$, see figure 4 | 9, 10, 11 | All | | 18 | ns |
| Output enable time, CPU2MEN to CPUDATAn | $t_{PLZ2}$, $t_{PHZ2}$ | | 9, 10, 11 | All | | 15 | ns |
| Output disable time, CPU2MEN to CPUDATAn | $t_{PZL2}$, $t_{PZH2}$ | | 9, 10, 11 | All | | 15 | ns |
| Output enable time, CPU2MEN to CPUPARITY | $t_{PLZ3}$, $t_{PHZ3}$ | | 9, 10, 11 | All | | 15 | ns |
| Output disable time, CPU2MEN to CPUPARITY | $t_{PZL3}$, $t_{PZH3}$ | | 9, 10, 11 | All | | 15 | ns |

1/ Devices supplied to this drawing have been characterized through all levels M, D, L, R, F, G, and H of irradiation. Pre and Post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, $T_A$ = +25°C.
2/ Vector sets for all group A tests shall be specified in the test program maintained by the manufacturer.
3/ This test is not required for VCP test bus pins.
4/ Test not required for open drain outputs.
5/ If not tested, shall be guaranteed to the limits specified in table IA.
6/ Conditions for the use of functional test vectors are specified.
7/ Input rise and fall times ($t_{ri}$ and $t_{fi}$) shall not exceed 5.0 ns between the 10% and 90% points as referenced to the $V_{IH}$ and $V_{IL}$ difference.

TABLE IB. SEP test limits by storage cell and chip set. (All device types) 1/ 2/ 3/

| Storage cell type | Effective LET (no upsets) [MeV/(cm$^2$/mg)] | Maximum cell cross section (LET = 120) $\sigma_2$ (cm$^2$) | Cell quantity CPU1 | Cell quantity CPU2 | Cell quantity CPU3 | Cell quantity FPP1 | Cell quantity FPP2 | Maximum chip cross section (LET = 120) $\sigma_2$ (cm$^2$) |
|---|---|---|---|---|---|---|---|---|
| FF5 | ≥20 | 7.06E-07 | 287 | 208 | 334 | 0 | 0 | 5.85E-04 |
| CELL RF | ≥40 | 1.17E-08 | 0 | 256 | 334 | 0 | 0 | 7.50E-06 |
| REGFILE | ≥56 | 1.95E-06 | 0 | 0 | 0 | 256 | 0 | 5.00E-04 |
| OUTSCAN | ≥40 | 8.93E-07 | 40 | 40 | 28 | 30 | 46 | 1.64E-04 |
| FC62R | ≥35 | 2.44E-06 | 0 | 0 | 0 | 164 | 319 | 1.18E-03 |
| ILATCH | ≥60 | 2.73E-07 | 0 | 0 | 22 | 24 | 0 | 1.25E-05 |
| OLATCH | ≥40 | 2.19E-06 | 0 | 0 | 16 | 16 | 0 | 7.00E-05 |
| MEMCELL 4/ | ≥20 | 1.95E-07 | 0 | 0 | 1024 | 10240 | 0 | 2.20E-03 |
| CLK DRIVER | ≥20 | 3.00E-06 | 2 | 0 | 0 | 0 | 0 | 6.00E-06 |
| CLK DRIVER A | ≥20 | 3.00E-06 | 0 | 2 | 2 | 0 | 0 | 1.20E-05 |
| | | | | | | | | |
| Chip set total | ≥20 | | | | | | | 4.54E-03 |

1/ For SEP test conditions, see 4.5.4.4 herein.
2/ $T_A$ = +125°C, worst case conditions.
3/ The MCM chipset is comprised of ten different memory cell types, many with unique SEP characteristics; consequently the chipset SEP response is not adequately defined by a single SEP LET threshold and saturation cross-section. The Government has conducted SEP tests of these chips with assistance from the manufacturer to determine the SEP responses of the chipset and its various storage cell types. Based on this test data, the chipset SEP rate calculated from the SEP cell data for a typical space environment (the 90% worst-case environment in a geosynchronous equatorial orbit) is 3E-5 upsets/chipset-day.
4/ This memory array is the largest contributor to the chipset SEE rate due to the large number of cells present (10240 in the FPP1 chip and 1024 in the CPU3 chip). However, the cells in the CPU3 chip are not used for processor architectures that include the FPP1 chip, and the actual number of cells used in the FPP1 depends on the amount of external memory that is addressed by the processor (the less memory used, the fewer of these memory cells that are actually used). The number 10240 for the FPP1 chip was used to calculate the maximum chipset cross section.




Note:

1. Dimensions are in inches.

FIGURE 1. Case outline Y.

| STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444 | SIZE A | | 5962-94667 |
|---|---|---|---|
| | | REVISION LEVEL | SHEET 11 |

| Device type | All | | Device type | All | |
|---|---|---|---|---|---|
| Case outline | Y | | Case outline | Y | |
| Terminal number | Signal name | Signal type 1/ | Terminal number | Signal name | Signal type 1/ |
| 1 | VCP1 | BI | 51 | CLKA | OUT |
| 2 | VCP5 | BI | 52 | SELECTN | IN |
| 3 | VCP3 | BI | 53 | INT11N | IN |
| 4 | MODEFPP2 | IN | 54 | WRITE | OUT |
| 5 | LINSTF | TRI | 55 | INT12N | IN |
| 6 | CPUADDR16 | TRI | 56 | INT10N | IN |
| 7 | NFTSFPP2 | IN | 57 | INT08N | IN |
| 8 | NFTDOUTN | OUT | 58 | INT13N | IN |
| 9 | MODEFPP1 | IN | 59 | INT14N | IN |
| 10 | VCP6 | BI | 60 | INT15N | IN |
| 11 | NFTDI | IN | 61 | INT02N | IN |
| 12 | VCP0 | BI | 62 | PWRDWN | IN |
| 13 | VCP2 | BI | 63 | CPUWDATA6 | TRI |
| 14 | VCP4 | BI | 64 | CPUWDATA5 | TRI |
| 15 | MMUSEL | IN | 65 | CPUWDATA0 | TRI |
| 16 | TMRCLK | IN | 66 | CPUWDATA1 | TRI |
| 17 | VCP7 | BI | 67 | INT01N | OUT |
| 18 | VDD | +POWER | 68 | VDD | +POWER |
| 19 | MRSTN | IN | 69 | CPUWDATA4 | TRI |
| 20 | VDD | +POWER | 70 | VDD | +POWER |
| 21 | READDATA31 | IN | 71 | CPUWDATA2 | TRI |
| 22 | VDD | +POWER | 72 | VDD | +POWER |
| 23 | INTREQN | OUT | 73 | NFTSCPU2 | IN |
| 24 | VDD | +POWER | 74 | VSS | -POWER |
| 25 | CPUADDR8 | TRI | 75 | MODECPU2 | IN |
| 26 | VSS | -POWER | 76 | VSS | -POWER |
| 27 | CPUADDR7 | TRI | 77 | ALTFLT0 | OUT |
| 28 | VSS | -POWER | 78 | VSS | -POWER |
| 29 | CPUADDR15 | TRI | 79 | CPUPARITY | TRI |
| 30 | VSS | -POWER | 80 | VSS | -POWER |
| 31 | CPUADDR11 | TRI | 81 | CPUWDATA7 | TRI |
| 32 | CPUADDR17 | TRI | 82 | CPUWDATA9 | TRI |
| 33 | CPUADDR12 | TRI | 83 | CPUWDATA8 | TRI |
| 34 | CPUADDR14 | TRI | 84 | READDATA29 | IN |
| 35 | CPUADDR9 | TRI | 85 | CPUWDATA3 | TRI |
| 36 | CPUADDR19 | TRI | 86 | CPUWDATA10 | TRI |
| 37 | CPUADDR10 | TRI | 87 | CPUWDATA11 | TRI |
| 38 | CPUADDR18 | TRI | 88 | CPUWDATA12 | TRI |
| 39 | CPUADDR13 | TRI | 89 | CPUWDATA14 | TRI |
| 40 | CPUADDR4 | TRI | 90 | CPUWDATA13 | TRI |
| 41 | ASFLT0 | OUT | 91 | CPU2MEN | IN |
| 42 | MMUWRT0 | OUT | 92 | SCPE02 | OUT |
| 43 | PROTFLT | OUT | 93 | READDATA25 | IN |
| 44 | READ | OUT | 94 | CPUWDATA15 | TRI |
| 45 | DMAGRNT | OUT | 95 | SCP2A | IN |
| 46 | SIOE | OUT | 96 | SCP2B | IN |
| 47 | NFTSCPU3 | IN | 97 | SCP1B | IN |
| 48 | MODECPU3 | IN | 98 | SCP1A | IN |
| 49 | SCPE03 | OUT | 99 | VCPBPT | OUT |
| 50 | CPU3MEN | IN | 100 | DI4 | IN |

See footnotes at end of table.

FIGURE 2. Terminal connections.

| Device type | All | | Device type | All | |
|---|---|---|---|---|---|
| Case outline | Y | | Case outline | Y | |
| Terminal number | Signal name | Signal type 1/ | Terminal number | Signal name | Signal type 1/ |
| 101 | DI3 | IN | 151 | PARFLTI | IN |
| 102 | DI7 | IN | 152 | ILLIOX | IN |
| 103 | DI5 | IN | 153 | READDATA4 | IN |
| 104 | DI6 | IN | 154 | DMARQST | IN |
| 105 | DI2 | IN | 155 | READDATA19 | IN |
| 106 | DI1 | IN | 156 | READDATA17 | IN |
| 107 | DI0 | IN | 157 | READDATA18 | IN |
| 108 | READDATA30 | IN | 158 | READDATA24 | IN |
| 109 | VCPSELN | IN | 159 | READDATA22 | IN |
| 110 | DOR5 | OUT | 160 | READDATA23 | IN |
| 111 | VCPRDE | IN | 161 | READDATA26 | IN |
| 112 | DOR6 | OUT | 162 | TSTCLK | IN |
| 113 | DOR7 | OUT | 163 | CPUADDR3 | TRI |
| 114 | DOR4 | OUT | 164 | DMAMPF | OUT |
| 115 | DOR1 | OUT | 165 | DMACPF | IN |
| 116 | DOR0 | OUT | 166 | ASFLTI | IN |
| 117 | DOR3 | OUT | 167 | CLKOUT | OUT |
| 118 | VDD | +POWER | 168 | VDD | +POWER |
| 119 | DOR2 | OUT | 169 | TINTREQN | OD |
| 120 | VDD | +POWER | 170 | VDD | +POWER |
| 121 | ALUFLTI | IN | 171 | BNK0 | TRI |
| 122 | VDD | +POWER | 172 | VDD | +POWER |
| 123 | DOUTENA | OUT | 173 | NFTSFPP1 | IN |
| 124 | VDD | +POWER | 174 | VSS | -POWER |
| 125 | READDATA21 | IN | 175 | BNK2 | TRI |
| 126 | VSS | -POWER | 176 | VSS | -POWER |
| 127 | READDATA16 | IN | 177 | HCLK | CLK |
| 128 | VSS | -POWER | 178 | VSS | -POWER |
| 129 | READDATA28 | IN | 179 | PIO | OUT |
| 130 | VSS | -POWER | 180 | VSS | -POWER |
| 131 | READDATA27 | IN | 181 | EXPMEM | IN |
| 132 | VSS | -POWER | 182 | MMUWRTI | IN |
| 133 | READDATA20 | IN | 183 | CPUADDR1 | TRI |
| 134 | READDATA12 | IN | 184 | NFTRN | IN |
| 135 | READDATA13 | IN | 185 | MODECPU1 | IN |
| 136 | READDATA15 | IN | 186 | READDATAP2 | IN |
| 137 | READDATA14 | IN | 187 | VCPACKN | OD |
| 138 | READDATA11 | IN | 188 | CONSOLEN | IN |
| 139 | READDATA10 | IN | 189 | CPUADDR5 | TRI |
| 140 | READDATA9 | IN | 190 | LACKN | IN |
| 141 | READDATA8 | IN | 191 | MEMTIMEN | OUT |
| 142 | PARFLTO | OUT | 192 | NFTSE | IN |
| 143 | READDATA0 | IN | 193 | SYSCLKD | OUT |
| 144 | READDATA7 | IN | 194 | BNK1 | TRI |
| 145 | READDATA2 | IN | 195 | LRMW | TRI |
| 146 | READDATA3 | IN | 196 | CPUADDR0 | TRI |
| 147 | READDATA5 | IN | 197 | CPUADDR2 | TRI |
| 148 | READDATA6 | IN | 198 | READDATAP1 | IN |
| 149 | FPPPRESN | IN | 199 | CPUADDR6 | TRI |
| 150 | READDATA1 | IN | 200 | NFTSCPU1 | IN |

1/ BI - Bidirectional (input/output)
IN - Input
OUT - Output
CLK - System clock
OD - Open drain
TRI - Three-state output

FIGURE 2. Terminal connections - continued.

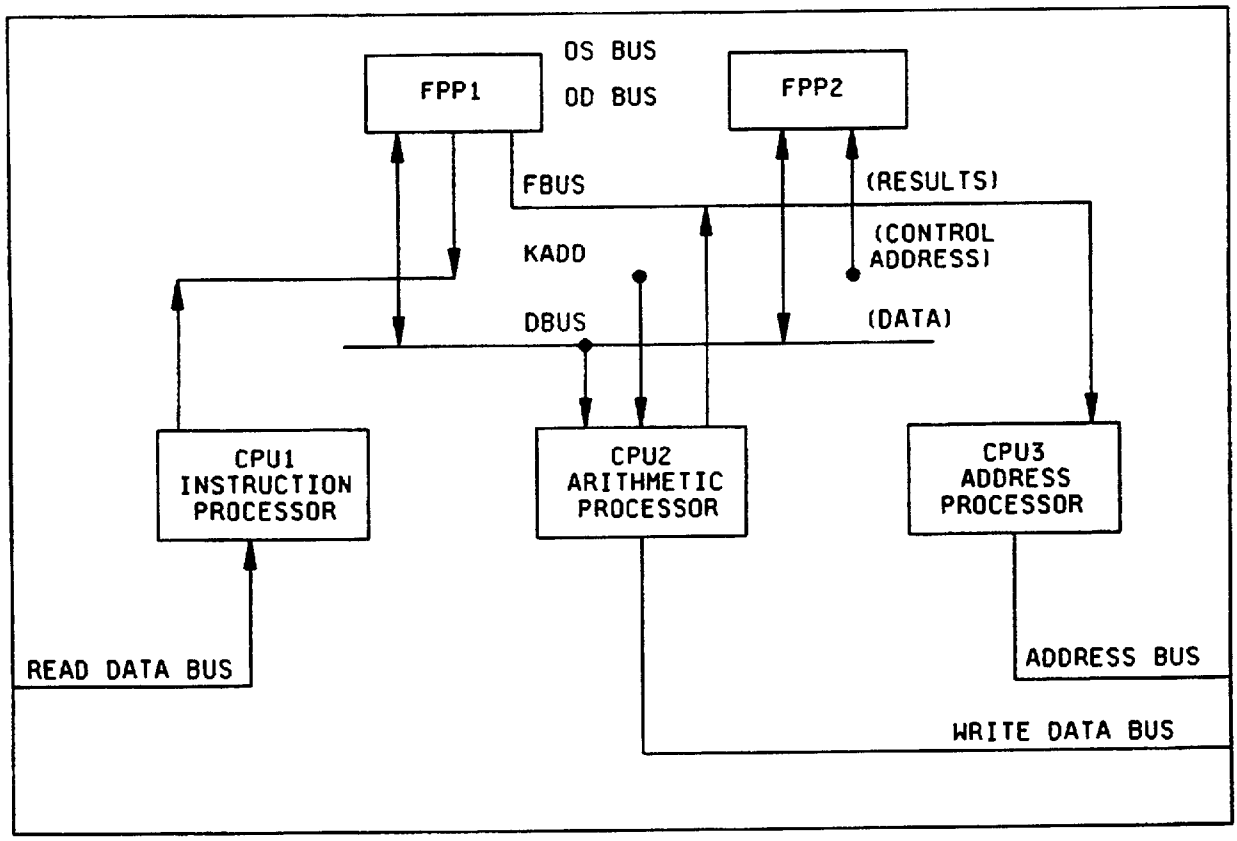
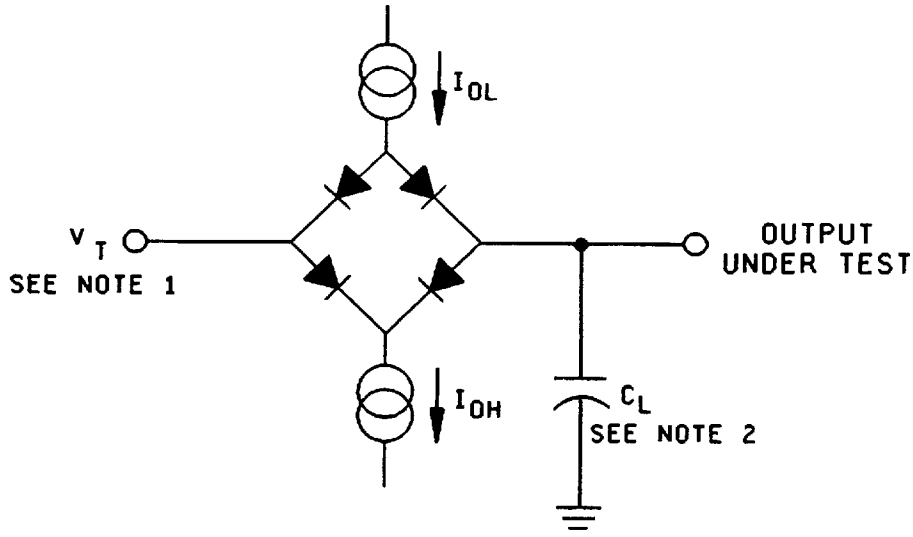



FIGURE 3. Block diagram.

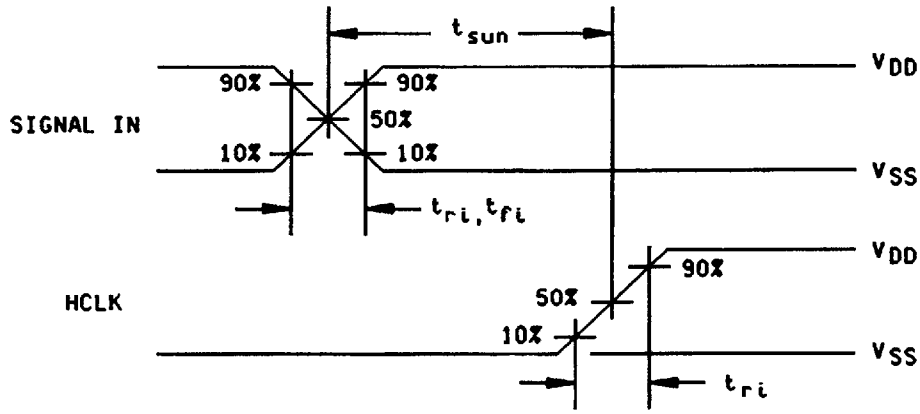



Notes:

1. VT is a variable dependant upon the test parameter.
2. Load capacitance ($C_L$) includes jig and probe capacitance. For bidirectional output pins, $C_L$ = 115 pF; for all other outputs, $C_L$ = 85 pF.

FIGURE 4. Switching test circuit and waveforms.

SETUP TIME FOR SIGNAL INPUT TO HCLK




HOLD TIME FOR SIGNAL INPUT TO HCLK

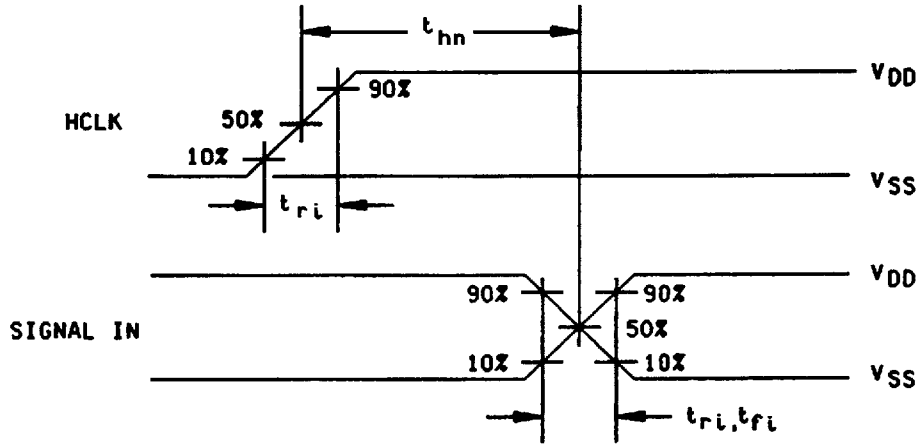
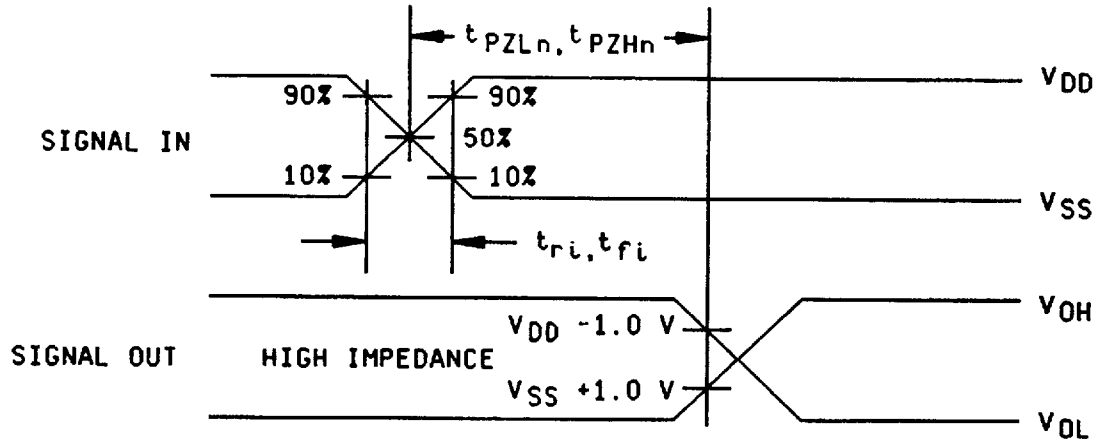



FIGURE 4. Switching test circuit and waveforms - continued.

SIGNAL INPUT TO THREE-STATE ENABLE DELAY




SIGNAL INPUT TO THREE-STATE DISABLE DELAY

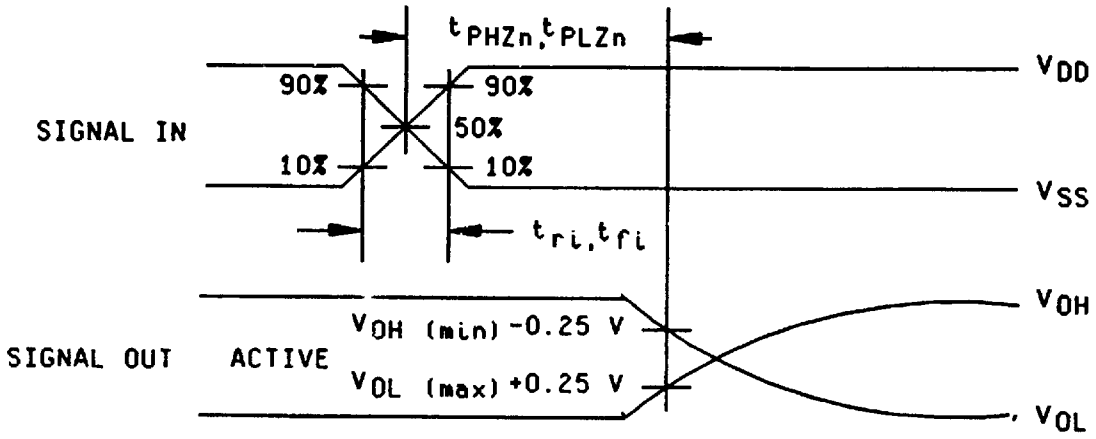



FIGURE 4. Switching test circuit and waveforms - continued.

OUTPUT RISE AND FALL TIMES

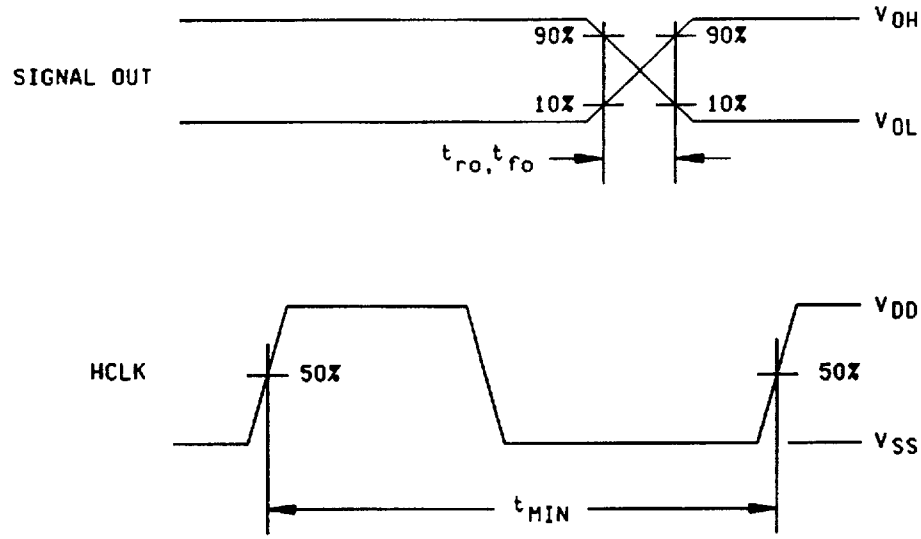
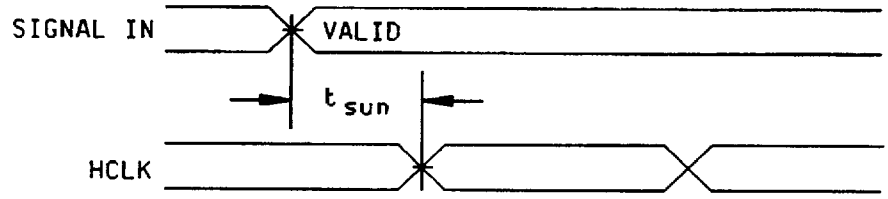
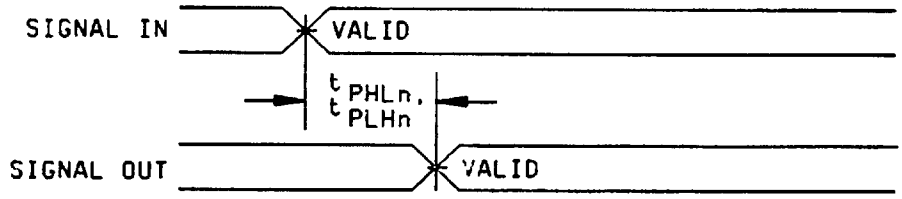



FIGURE 4. Switching test circuit and waveforms - continued.

SETUP TIME FOR SIGNAL INPUT TO HCLK




PROPAGATION DELAY OF SIGNAL FROM INPUT TO OUTPUT




PROPAGATION DELAY FROM HCLK TO SIGNAL OUTPUT

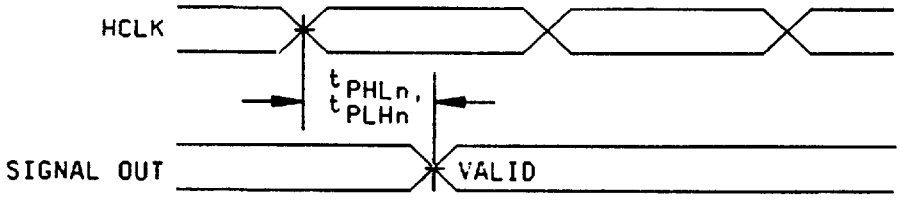
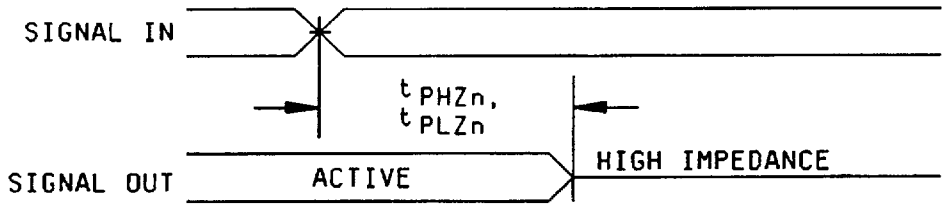
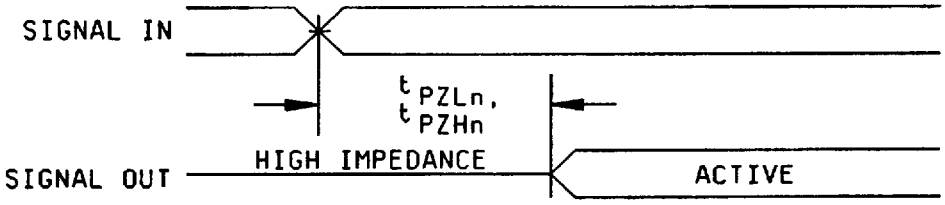



FIGURE 4. Switching test circuit and waveforms - continued.

SIGNAL INPUT TO OUTPUT DISABLE DELAY




SIGNAL INPUT TO OUTPUT ENABLE DELAY




HCLK TO OUTPUT DISABLE DELAY

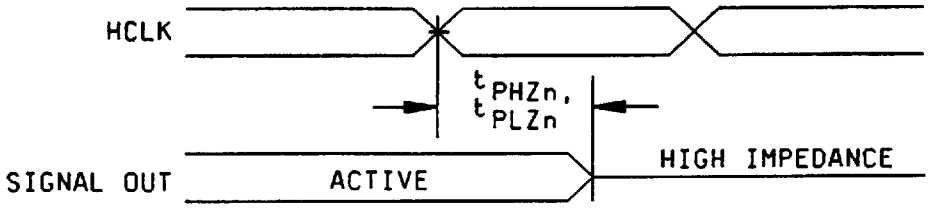
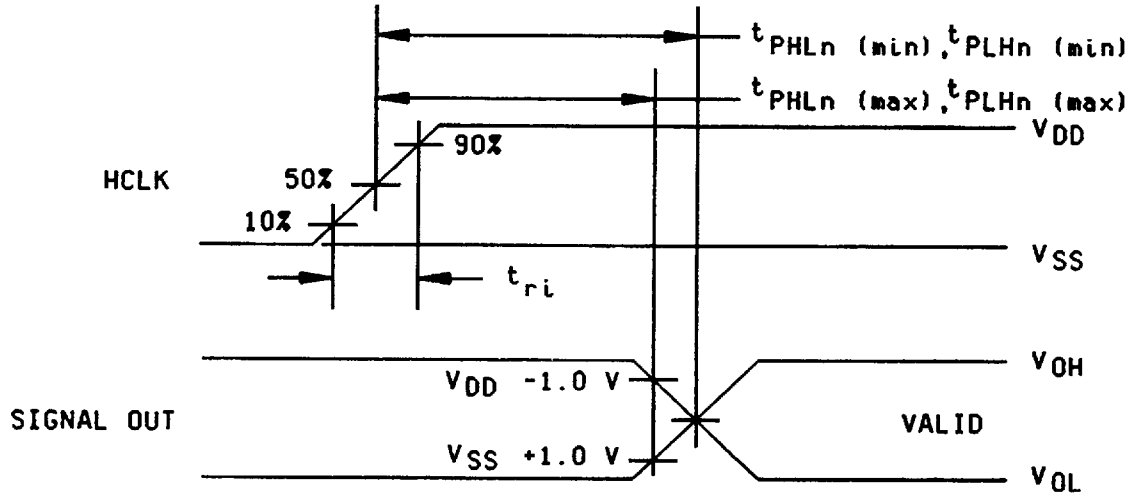



FIGURE 4. Switching test circuit and waveforms - continued.

PROPAGATION DELAY FROM HCLK TO SIGNAL OUTPUT




PROPAGATION DELAY OF SIGNAL FROM INPUT TO OUTPUT

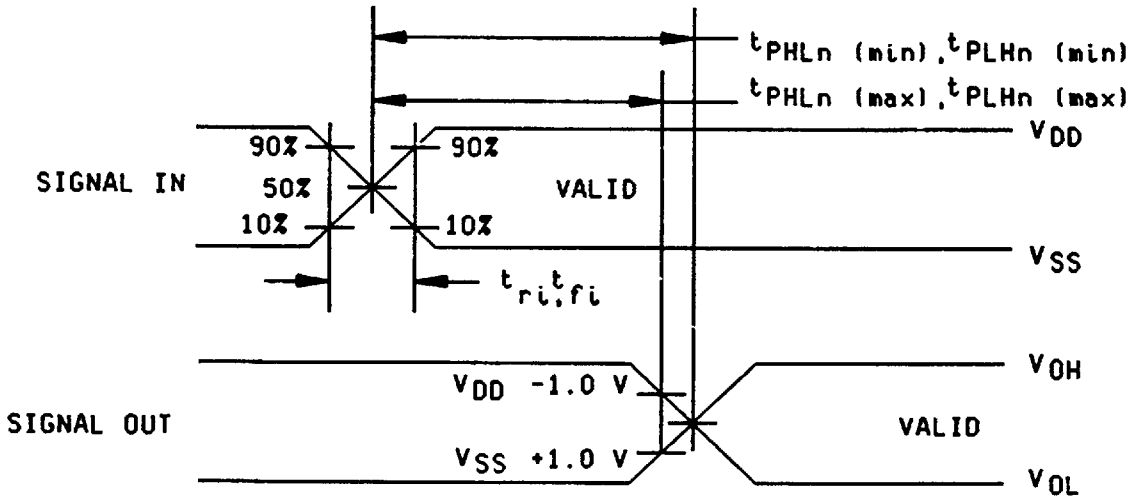
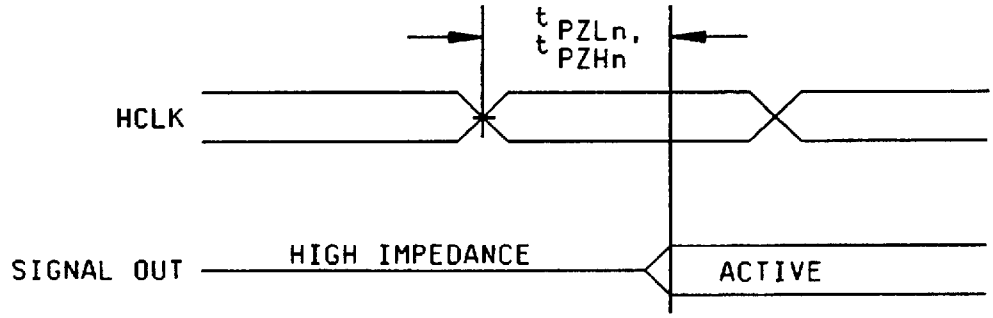



FIGURE 4. Switching test circuit and waveforms - continued.

HCLK TO OUTPUT ENABLE DELAY




HOLD TIME FOR SIGNAL INPUT FROM HCLK

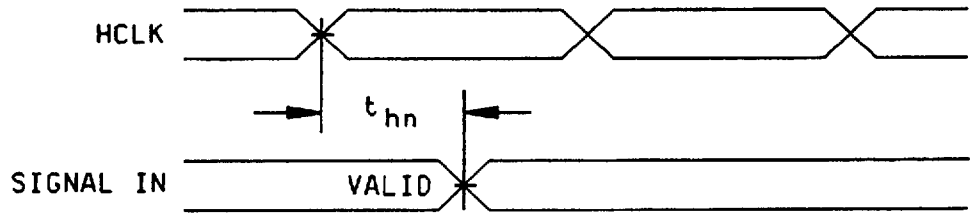
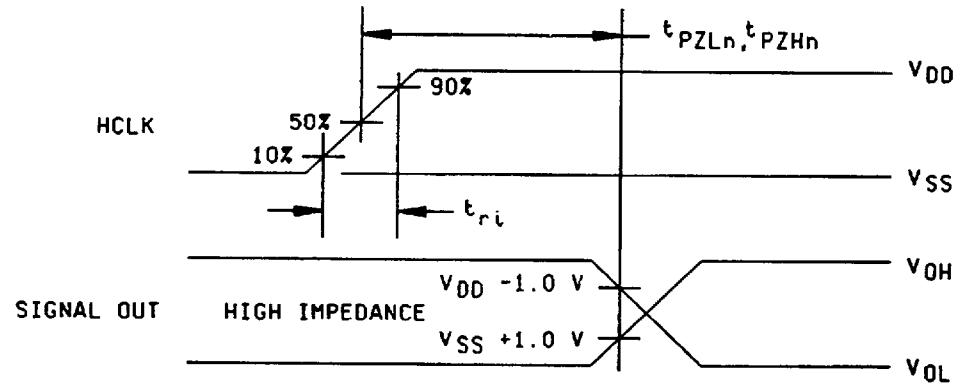



FIGURE 4. Switching test circuit and waveforms - continued.

HCLK TO OUTPUT ENABLE DELAY




HCLK TO OUTPUT DISABLE DELAY

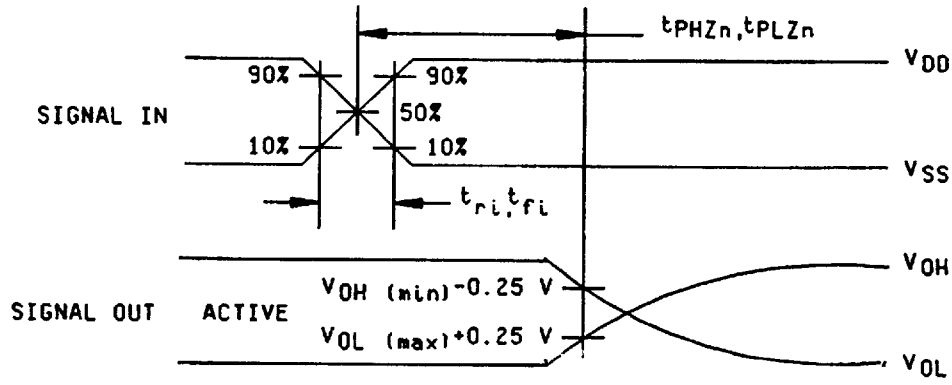



FIGURE 4. Switching test circuit and waveforms - continued.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-I-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

4.2 Element evaluation.

4.2.1 Microcircuit dice. Microcircuit dice shall be produced on a QML certified line and probed at wafer level according to the manufacturer's QM plan.

4.2.2 Capacitors. Capacitor element evaluation shall be performed according to the manufacturer's QM plan.

4.2.3 Package evaluation. Packages shall be electrically tested by the package manufacturer. Element evaluation shall be performed according to the manufacturer's QM plan.

4.3 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.3.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, D, or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) $T_A$ = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.3.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

d. Those devices whose measured characteristics, after burn-in, exceed the specified delta (Δ) limits or electrical parameter limits specified in table IIB, are defective and shall be removed from the lot. The verified failures divided by the total number of devices in the lot initially submitted to burn-in shall be used to determine the percent defective for the lot and the lot shall be accepted or rejected based on the PDA specified in the manufacturer's QM plan.

4.4 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.5.1 through 4.5.4).

TABLE IIA. Electrical test requirements.

| Test requirements | Subgroups (in accordance with MIL-STD-883, TM 5005, table I) | Subgroups (in accordance with MIL-I-38535, table III) | |
|---|---|---|---|
| | Device class M | Device class Q | Device class V |
| Pre seal electrical parameters (see 4.3) | | 1, 2, 3, 7, 8A 8B, 9, 10, 11 | 1, 2, 3, 7, 8A 8B, 9, 10, 11 |
| Initial (pre burn-in) electrical parameters (see 4.3) | | 1, 7, 9 | 1, 7, 9 |
| Dynamic burn-in (see 4.3) | | Required | Required |
| Interim (post dynamic burn-in) electrical parameters (see 4.3) | | 1, 2, 3, 7, 8A, 8B, 9, 10, 11 2/ 3/ | 1, 2, 3, 7, 8A, 8B, 9, 10, 11 2/ 3/ |
| Static burn-in (see 4.3) | Required | Required | Required |
| Final electrical parameters (see 4.3) | 1, 2, 3, 7, 8A, 8B, 9, 10, 11 1/ | 1, 2, 3, 7, 8A, 8B, 9, 10, 11 2/ 3/ | 1, 2, 3, 7, 8A, 8B, 9, 10, 11 2/ 3/ |
| Group A test requirements (see 4.5) | 1, 2, 3, 4, 5, 6, 7 8A, 8B, 9, 10, 11 4/ | 1, 2, 3, 4, 5, 6, 7 8A, 8B, 9, 10, 11 4/ | 1, 2, 3, 4, 5, 6, 7 8A, 8B, 9, 10, 11 4/ |
| Group C end-point electrical parameters (see 4.5) | 1, 7 | 1, 2, 3, 7, 8A, 8B, 9, 10, 11 3/ | 1, 2, 3, 7, 8A, 8B, 9, 10, 11 3/ |
| Group D end-point electrical parameters (see 4.5) | 1, 7 | 1, 7 | 1, 7 |
| Group E end-point electrical parameters (see 4.5) | 1, 7 | 1, 7 | 1, 7 |

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.
3/ After completion of life test, or burn-in, deltas shall be calculated and shall meet the requirements of table IIB herein.
4/ See 4.5.1c.

4.5 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.5.1 through 4.5.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

TABLE IIB. Delta limits at +25°C.

| Test 1/ | Delta limit (all device types) |
|---|---|
| $I_{DDSB}$ | ±20% of the initial measured value or ±200 µA, whichever magnitude is greater |
| $I_{IH}$, $I_{IL}$, $I_{OZH}$, $I_{OZL}$ | ±10% of the initial measured value or ±1.0 µA, whichever magnitude is greater |
| $V_{OH1}$, $V_{OH2}$, $V_{OL1}$, $V_{OL2}$ | ±10% of the initial measured value or ±50 mV, whichever magnitude is greater |

1/ The above parameters shall be tested in accordance with table IA and shall be recorded before and after the required burn-in and life tests to determine the delta.

4.5.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroups 4, 5, and 6 ($C_{IN}$ and $C_{OUT}$ measurements), if not tested, shall be guaranteed to the limits specified in table IA.

d. O/V (latchup) test shall be measured only for initial qualification or after any design or process changes which may affect the performance of the device. For classes Q and V the procedures and circuits shall be submitted to DESC-EC and will be under the control of the device manufacturer's technical review board (TRB). Testing shall be on all pins, on 5 devices with zero failures. Latchup test shall be considered destructive.

4.5.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.5.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, D, or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. $T_A$ = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

d. Those devices whose measured characteristics, after steady-state life test, exceed the specified delta (Δ) limits or electrical parameter limits specified in table IIB, are defective.

4.5.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

a. $T_A$ = +125°C, minimum.

b. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

c. Those devices whose measured characteristics, after steady-state life test, exceed the specified delta (Δ) limits or electrical parameter limits specified in table IIB, are defective.

4.5.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.5.4 Group E inspection. Group E inspection is required only for MCM's intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, L, R, F, G, and H and for device class M shall be M and D. Generic test data on individual elements may be used to satisfy the group E inspection requirements. MCM's are considered to meet a specific RHA level if all of the elements used in the manufacture of the MCM have previously passed conformance inspection to that RHA level, or a higher level. Generic test data is defined as test data from elements manufactured by means of the same production technique, materials, controls and design as the deliverable elements. Generic test data shall be maintained by the manufacturer and shall be made available to the preparing or acquiring activity upon request.

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at $T_A$ = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 and as specified herein.

4.5.4.1.1 Accelerated aging test. Accelerated aging tests shall be performed on all devices requiring a RHA level greater than 5K rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ± 5°C. The test shall be performed at initial qualification and after any design on process changes which may affect the radiation responses of the device.

4.5.4.2 Dose rate induced latchup testing. Dose rate induced latchup testing shall be performed in accordance with method 1020 of MIL-STD-883 and as specified herein. Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may effect the RHA capability of the process.

4.5.4.3 Dose rate upset testing. Dose rate upset testing shall be performed in accordance with test method 1021 of MIL-STD-883 and as specified herein.

a. Transient dose rate upset testing for class M devices shall be performed at initial qualification and after any design or process changes which may effect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-I-38535. Device parametric parameters that influence upset immunity shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-I-38535.

4.5.4.4 Single event phenomena (SEP). SEP testing shall be required on class V devices. SEP testing shall be performed on the SEC or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM standard F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be normal to the die surface and 60 degrees to the normal, inclusive (i.e., $0° \leq$ angle $\leq 60°$). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be greater than 100 errors or $\geq 10^7$ ions/cm$^2$.

c. The flux shall be between $10^2$ and $10^5$ ion/cm$^2$/s. The cross section shall be verified to be flux independent by measuring the cross section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be $\geq$ 20 microns in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be $V_{DD}$ = 4.5 V dc for the upset measurements and $V_{DD}$ = 5.5 V dc for the latchup measurements.

g. For SEP test limits, see table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535 and MIL-STD-1331.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

| Military documentation format | Example PIN under new system | Manufacturing source listing | Document listing |
|---|---|---|---|
| New MIL-H-38534 Standard Microcircuit Drawings | 5962-XXXXXZZ(H or K)YY | QML-38534 | MIL-BUL-103 |
| New MIL-I-38535 Standard Microcircuit Drawings | 5962-XXXXXZZ(Q or V)YY | QML-38535 | MIL-BUL-103 |
| New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings | 5962-XXXXXZZ(M)YY | MIL-BUL-103 | MIL-BUL-103 |

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

6.8 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied.

a. RHA upset levels.
b. Test conditions (SEP).
c. Number of upsets (SEP).
d. Number of transients (SEP).
e. Occurance of latchup (SEP).