Signetics

Military Logic Products

54LS240, 54LS241, 54S240, 54S241

Buffers

'240 Octal Inverter Buffer (3-State)
'241 Octal Buffer (3-State)
Product Specification

FUNCTION TABLE '240

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	$\overline{Y}_a$	$\overline{Y}_b$
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	(Z)	(Z)

H = High voltage level
L = Low voltage level
X = Don't care
(Z) = High impedance (off) state

FUNCTION TABLE '241

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	OE_b	I_b	Y_a	Y_b
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	(Z)	(Z)

H = High voltage level
L = Low voltage level
X = Don't care
(Z) = High impedance (off) state

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-Pin Ceramic DIP	54LS240/BRA 54S240/BRA 54LS241/BRA 54S241/BRA
20-Pin Ceramic FlatPack	54LS240/BSA 54S240/BSA 54LS241/BSA 54S241/BSA
20-Pin Ceramic LLCC	54LS240/B2A 54S240/B2A 54LS241/B2A 54LS241/B2A

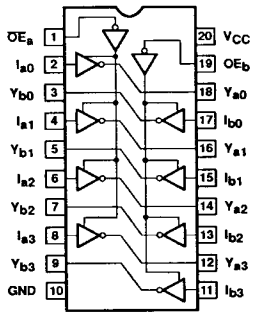
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54S	54LS
I_{a0} - I_{a3}, I_{b0} - I_{b3}	Inputs	1SUL	1LSUL
$\overline{OE}_a$, $\overline{OE}_b$, OE_b	Inputs	1SUL	1LSUL
All	Outputs	24SUL	32LSUL

NOTE: A 54S Unit Load (SUL) is 50μA I_{IH}, and -2.0mA I_{IL} and a 54LS Unit Load (LSUL) is 20μA I_{IH} and -0.4mA I_{IL}.

PIN CONFIGURATION

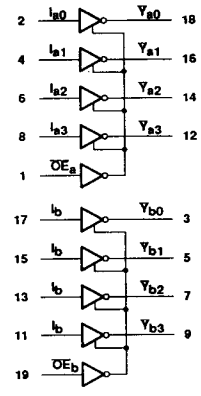
'240



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL

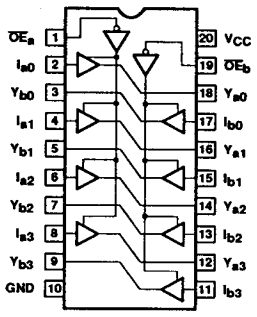
'240



For LLCC pin assignments, see JEDEC Standard No. 2

PIN CONFIGURATION

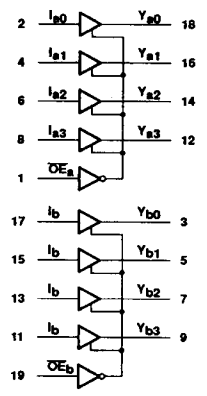
'241



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL

'241



For LLCC pin assignments, see JEDEC Standard No. 2

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	54LS	54S	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_I	Input voltage range	-0.5 to +7.0	-0.5 to +5.5	V
I_I	Input current range	-30 to +1	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54LS			54S			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			2.0			V
V_{IL}	Low-level input voltage			+0.7			+0.8	V
	+125°C			+0.7			+0.7	V
I_{IK}	Input clamp current			-18			-18	mA
I_{OH}	High-level output current			-12			-12	mA
I_{OL}	Low-level output current			12			48	mA
T_A	Operating free-air temperature range	-55		+125	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			54LS240, 241			54S240, 241			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)[6]	V_{CC} = Min			0.2	0.4		0.2	0.4		V
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max			2.0			2.0			V
		V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = -3mA			2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max					0.4			0.55	V
V_{IK}	Input clamp voltage	V_{CC} = Min, $I_I = I_{IK}$					-1.5			-1.2	V
I_{OZH}	Offstate output current, High-level voltage applied	V_{CC} = Max, V_{IH} = Min, V_{IL} = Max	V_O = 2.4V							50	µA
			V_O = 2.7V				20				µA
I_{OZL}	Offstate output current, Low-level voltage applied	V_{CC} = Max, V_{IH} = Min, V_{IL} = Max	V_O = 2.4V				-20				µA
			V_O = 0.5V							-50	µA
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max	V_I = 5.5V							1.0	mA
			V_I = 7.0V				0.1				mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V					20			50	µA
I_{IL}	Low-level input current	V_{CC} = Max	V_I = 0.4V				-0.2				mA
			V_I = 0.5V	$I_{a0} - I_{a3}$, $I_{b0} - I_{b3}$ inputs						-400	µA
				$\overline{OE}_a$, $\overline{OE}_b$, OE_b inputs						-2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max			-40		-130	-80		-180	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max	I_{CCH}	'LS240		17	27				mA
			I_{CCL}			26	44				mA
			I_{CCZ}			29	60				mA
			I_{CCH}	'LS241		17	27				mA
			I_{CCL}			27	46				mA
			I_{CCZ}			32	54				mA
			I_{CCH}	'S240					80	123	mA
			I_{CCL}						100	145	mA
			I_{CCZ}						100	145	mA
			I_{CCH}	'S241					95	147	mA
			I_{CCL}						120	170	mA
			I_{CCZ}						120	170	mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

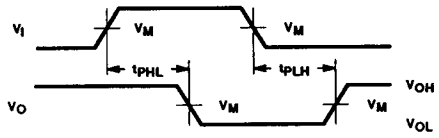
SYMBOL	PARAMETER	TEST CONDITIONS		54LS $C_L = 50pF$		54S $C_L = 50pF$		UNIT
				Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1, '240			14 18		7 7	ns ns
t_{PLH} t_{PHL}	Propagation delay	Waveform 2, '241			18 18		9 9	ns ns
t_{PZH}	Enable to High	Waveform 3	LS		30			ns
			'S240				10	ns
			'S241				12	ns
t_{PZL}	Enable to Low	Waveform 4			30		15	ns
t_{PHZ}	Disable from High	Waveform 3, $C_L = 5pF$[5]			18		9	ns
t_{PLZ}	Disable from Low	Waveform 4, $C_L = 5pF$[5]			25		15	ns
t_{PHZ}	Disable from High	Waveform 3, $C_L = 50pF$			34		14	ns
t_{PLZ}	Disable from Low	Waveform 4, $C_L = 50pF$			27		16.5	ns

AC ELECTRICAL CHARACTERISTICS $T_A = -55°C$ and $+125°C$, $V_{CC} = 5.0V$[6]

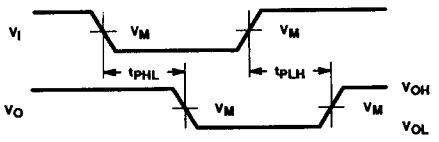
SYMBOL	PARAMETER	TEST CONDITIONS		54LS $C_L = 50pF$		54S $C_L = 50pF$		UNIT
				Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1, '240			18 23		9.0 9.0	ns ns
t_{PLH} t_{PHL}	Propagation delay	Waveform 2, '241			23 23		16 12	ns ns
t_{PZH}	Enable to High	Waveform 3	LS		39			ns
			'S240				13	ns
			'S241				20	ns
t_{PZL}	Enable to Low	Waveform 4			39		20	ns
t_{PHZ}	Disable from High	Waveform 3, $C_L = 5pF$[5]			23		12	ns
t_{PLZ}	Disable from Low	Waveform 4, $C_L = 5pF$[5]			33		20	ns
t_{PHZ}	Disable from High	Waveform 3, $C_L = 50pF$			44		18	ns
t_{PLZ}	Disable from Low	Waveform 4, $C_L = 50pF$			35		22	ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured with outputs open.
5. Guaranteed by 50pF limits, but not tested.
6. These parameters are guaranteed, but not tested.

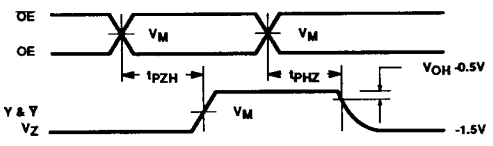
AC WAVEFORMS



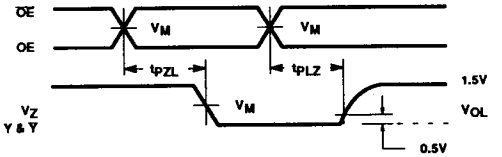
Waveform 1. Waveform for Inverting Outputs



Waveform 2. Waveform for Non-Inverting Outputs



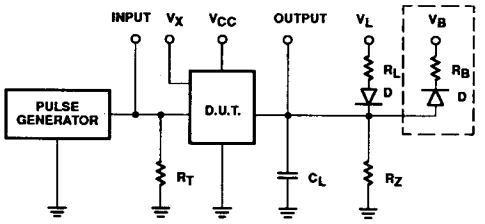
Waveform 3. 3-State Enable Time to High Level and Disable Time from High Level



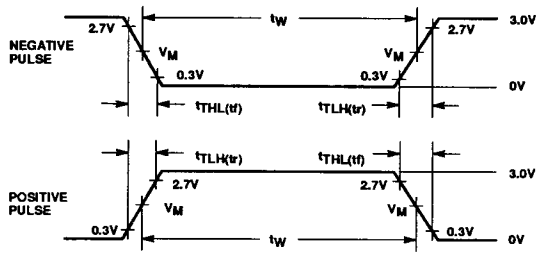
Waveform 4. 3-State Enable Time to Low Level and Disable Time from Low Level

FAMILY	V_M	V_{MZL}	V_{MZH}	V_Z
54LSXXX	1.3V	0.7V	1.9V	1.45V
54SXXX	1.5V	0.7V	2.0V	1.65V

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 3-State Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS							
	R_L	R_X	V_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	110Ω	2.4kΩ	2.1V	1.3V	1MHz	500ns	≤15ns	≤6ns
54SXXX	82Ω	560Ω	2.5V	1.5V	1MHz	500ns	≤2.5ns	≤2.5ns

Optional load for 54LSXXX only: R_B = 631Ω; V_B = 5.5V for all tests except T_{PHZ}; V_B = -0.6V for T_{PHZ} test.

DEFINITIONS:

C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.