

# W83194R-39/-39A



## 100MHZ 3-DIMM CLOCK

### W83194R-39/39A

#### Data Sheet Revision History

	Pages	Dates	Version	Version On Web	Main Contents
1	n.a.			n.a.	All of the versions before 0.50 are for internal use.
2	n.a.	02/Apr	1.0	1.0	Change version and version on web site to 1.0
3					
4					
5					
6					
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9					
10					

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## 1.0 GENERAL DESCRIPTION

The W83194R-39/-39A is a Clock Synthesizer, which provides all clocks required for high-speed RISC or CISC microprocessor such as Intel Pentium II. W83194R-39 provides eight different frequencies CPU and PCI clocks; W83194R-39A provides sixteen CPU/PCI frequencies, which are externally selectable with smooth transitions. W83194R-39/-39A also provides 13 SDRAM clocks controlled by the none-delay buffer\_in pin.

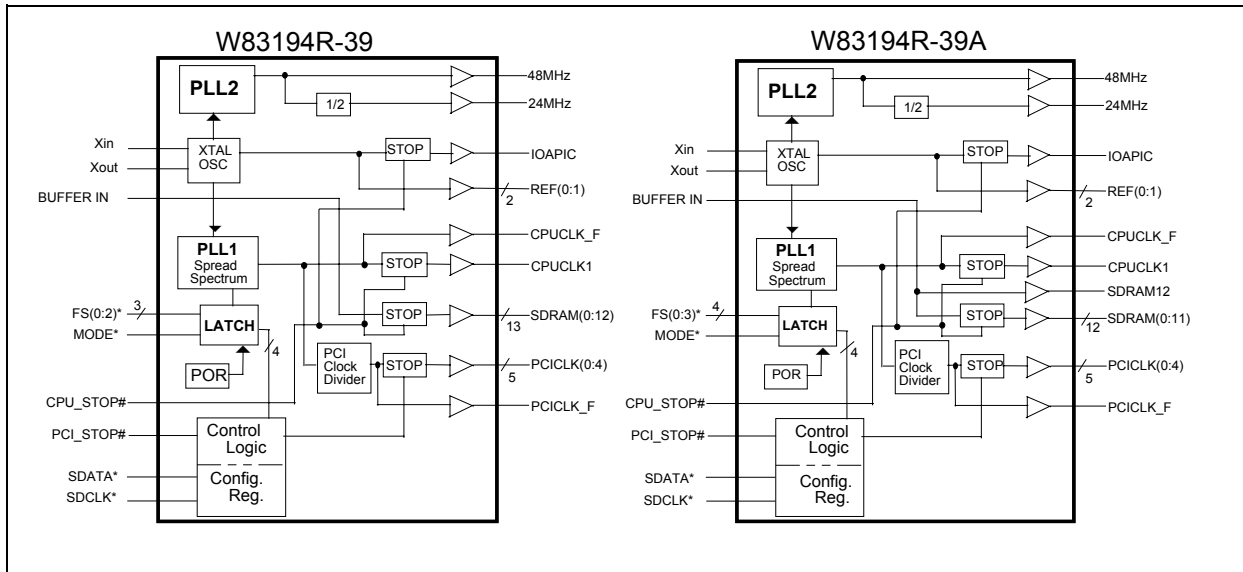
The W83194R-39/-39A accepts a 14.318 MHz reference crystal as its input and runs on a 3.3V supply. Spread spectrum built in at  $\pm 0.5\%$  or  $\pm 0.25\%$  to reduce EMI. Programmable stopping individual clock outputs and frequency selection through I<sup>2</sup>C interface. The device meets the Pentium power-up stabilization, which requires CPU and PCI clocks be stable within 2 ms after power-up. Using dual function pin for the slots (ISA, PCI, CPU, DIMM) is not recommend. The add on cards may have a pull up or pull down.

High drive six PCI and thirteen SDRAM CLOCK outputs typically provide greater than 1 V /ns slew rate into 30 pF loads. Two CPU CLOCK outputs typically provide better than 1 V /ns slew rate into 20 pF loads, when maintaining  $50 \pm 5\%$  duty cycle. The fixed frequency outputs, such as REF, 24MHz, and 48 MHz provide better than 0.5V /ns slew rate.

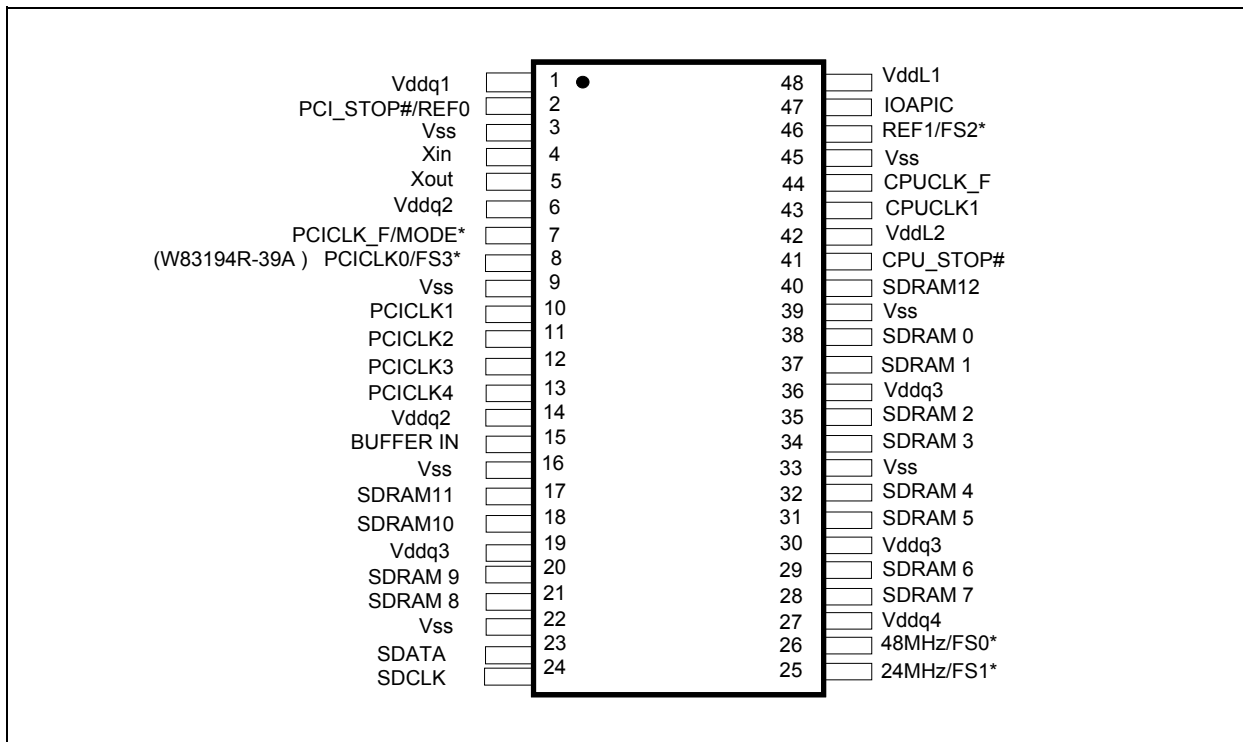
## 2.0 PRODUCT FEATURES

- Supports Pentium™ II CPU with I<sup>2</sup>C.
- 2 CPU clocks (one free-running CPU clock)
- 13 SDRAM clocks for 3 DIMs
- 6 PCI synchronous clocks
- One IOAPIC clock for multiprocessor support
- Optional single or mixed supply:  
(Vddq1=Vddq2 = Vddq3 = Vddq4 = VddL1 =VddL2= 3.3V) or (Vddq1= Vddq2 = Vddq3=Vddq4 = 3.3V, VddL1 = VddL2 = 2.5V)
- < 250ps skew among CPU and SDRAM clocks
- < 250ps skew among PCI clocks
- < 5ns propagation delay SDRAM from buffer input
- Skew from CPU (earlier) to PCI clock -1 to 4ns, center 2.6ns.
- Smooth frequency switch with selections from 50 MHz to 133 MHz CPU
- I<sup>2</sup>C 2-Wire serial interface and I<sup>2</sup>C read back
- $\pm 0.25\%$  or  $\pm 0.5\%$  spread spectrum function to reduce EMI
- Programmable registers to enable/stop each output and select modes  
(Mode as Tri-state or Normal)
- MODE pin for power Management
- One 48 MHz for USB & one 24 MHz for super I/O
- 48-pin SSOP package

## 3.0 BLOCK DIAGRAM



## 4.0 PIN CONFIGURATION





## 5.0 PIN DESCRIPTION

IN - Input

OUT - Output

I/O - Bi-directional Pin

# - Active Low

\* - Internal 250k $\Omega$  pull-up

### 5.1 Crystal I/O

SYMBOL	PIN	I/O	FUNCTION
Xin	4	IN	Crystal input with internal loading capacitors and feedback resistors.
Xout	5	OUT	Crystal output at 14.318MHz nominally.

### 5.2 CPU, SDRAM, PCI, IOAPIC Clock Outputs

SYMBOL	PIN	I/O	FUNCTION
CPUCLK_F	44	OUT	Free running CPU clock. Not affected by CPU_STOP#
CPUCLK1	43	OUT	Low skew (< 250ps) clock outputs for host frequencies such as CPU, Chipset and Cache. Powered by VddL2. Low if CPU_STOP# is low.
CPU_STOP#	41	IN	This asynchronous input halts CPUCLK1, IOAPIC & SDRAM (0:12) at logic "0" level when driven low.
IOAPIC	47	OUT	High drive buffered output of the crystal, and is powered by VddL1.
SDRAM [0:12]	17,18,20,21,28,29,31,32,34,35,37,38,40	OUT	SDRAM clock outputs. Fanout buffer outputs from BUFFER IN pin. (Controlled by chipset)
PCICLK_F/ *MODE	7	I/O	Free running PCI clock during normal operation. Latched Input. Mode=1, Pin 2 is REF0; Mode=0, Pin2 is PCI_STOP#
PCICLK0/*FS3 (W83194R-39A)	8	I/O	Low skew (< 250ps) PCI clock outputs. Latched input for FS3 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks.
PCICLK [0:4] (W83194R-39)	8,10,11,12,13	OUT	Low skew (< 250ps) PCI clock outputs. Synchronous to CPU clocks with 1-48ns skew (CPU early).
BUFFER IN	15	IN	Inputs to fanout for SDRAM outputs.
SDRAM [0: 11]	17,18,20,21,28,29,31,32,34,35,37,38	O	Synchronous DRAM DIMMs clocks which have the same frequency as CPU clocks

## 5.3 I2C Control Interface

SYMBOL	PIN	I/O	FUNCTION
*SDATA	23	I/O	Serial data of I <sup>2</sup> C 2-wire control interface with internal pull-up resistor.
*SDCLK	24	IN	Serial clock of I <sup>2</sup> C 2-wire control interface with internal pull-up resistor.

## 5.4 Fixed Frequency Outputs

SYMBOL	PIN	I/O	FUNCTION
REF0 / PCI_STOP#	2	I/O	14.318MHz reference clock. This REF output is the stronger buffer for ISA bus loads. Halt PCICLK (0:4) clocks at logic 0 level, when input low (In mobile mode. MODE=0)
REF1 / *FS2	46	I/O	14.318MHz reference clock. Latched input for FS2 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks.
24MHz / *FS1	25	I/O	24MHz output clock. Latched input for FS1 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks.
48MHz / *FS0	26	I/O	48MHz output for USB during normal operation. Latched input for FS0 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks.

## 5.5 Power Pins

SYMBOL	PIN	FUNCTION
Vddq1	1	Power supply for Ref [0:1] crystal and core logic.
VddL1	48	Power supply for IOAPIC output, either 2.5V or 3.3V.
VddL2	42	Power supply for CPUCLK [0:3], either 2.5V or 3.3V.
Vddq2	6, 14	Power supply for PCICLK_F, PCICLK [0:4], 3.3V.
Vddq3	19, 30, 36	Power supply for SDRAM [0:12], and CPU PLL core, nominal 3.3V.
Vddq4	27	Power for 24 & 48MHz output buffers and fixed PLL core.
Vss	3,9,16,22,33,39,45	Circuit Ground.

## 6.0 FREQUENCY SELECTION

### 6.1 Frequency table of W83194R-39

FS2	FS1	FS0	CPU, SDRAM (MHz)	PCI (MHz)	REF, IOAPIC (MHz)
0	0	0	50	25(CPU/2)	14.318
0	0	1	75	37.5(CPU/2)	14.318
0	1	0	83.3	41.65(CPU/2)	14.318
0	1	1	66.8	33.4(CPU/2)	14.318
1	0	0	103	34.3(CPU/3)	14.318
1	0	1	112	37.33(CPU/3)	14.318
1	1	0	133	33.25(CPU/4)	14.318
1	1	1	100.2	33.3(CPU/3)	14.318

### 6.2 Frequency table of W83194R-39A

FS3=0			CPU, SDRAM (MHz)	PCI (MHz)	REF, IOAPIC (MHz)
FS2	FS1	FS0			
0	0	0	124	41.33(CPU/3)	14.318
0	0	1	75	37.5(CPU/2)	14.318
0	1	0	83.3	41.65(CPU/2)	14.318
0	1	1	66.8	33.4(CPU/2)	14.318
1	0	0	103	34.3(CPU/3)	14.318
1	0	1	112	37.33(CPU/3)	14.318
1	1	0	133	44.33(CPU/3)	14.318
1	1	1	100.3	33.3(CPU/3)	14.318
FS3=1			CPU, SDRAM (MHz)	PCI (MHz)	REF, IOAPIC (MHz)
FS2	FS1	FS0			
0	0	0	120	40.00(CPU/3)	14.318
0	0	1	115	38.33(CPU/3)	14.318
0	1	0	110	36.67(CPU/3)	14.318
0	1	1	105	35.00(CPU/3)	14.318
1	0	0	140	35.00(CPU/4)	14.318
1	0	1	150	37.50(CPU/4)	14.318
1	1	0	124	31.00(CPU/4)	14.318
1	1	1	133	33.25(CPU/4)	14.318

## 7.0 MODE PIN -POWER MANAGEMENT INPUT CONTROL

MODE, Pin7 (Latched Input)	PIN 2
0	PCI_STOP# (Input)
1	REF0 (Output)

## 8.0 FUNTION DESCRIPTION

### 8.1 POWER MANAGEMENT FUNCTIONS

All clocks can be individually enabled or disabled via the 2-wire control interface. On power up, external circuitry should allow 3 ms for the VCO to stabilize prior to enabling clock outputs to assure correct pulse widths. When MODE=0, pins 15 and 46 are inputs (PCI\_STOP#), (CPU\_STOP#), when MODE=1, these functions are not available. A particular clock can be enabled as both the 2-wire serial control interface and one of these pins indicate that it should be enable.

The W83194R-39/-39A may be disabled in the low state according to the following table in order to reduce power consumption. All clocks are stopped in the low state, but maintain a valid high period on transitions from running to stop. The CPU and PCI clocks transform between running and stop by waiting for one positive edge on PCICLK\_F followed by negative edge on the clock of interest, after which high levels of the output are either enabled or disabled.

CPU_STOP#	PCI_STOP#	CPUCLK1, IOAPIC & SDRAM 0:12	PCI	OTHER CLKs	XTAL & VCOs
0	0	LOW	LOW	RUNNING	RUNNING
0	1	LOW	RUNNING	RUNNING	RUNNING
1	0	RUNNING	LOW	RUNNING	RUNNING
1	1	RUNNING	RUNNING	RUNNING	RUNNING



## 8.2 2-WIRE I<sup>2</sup>C CONTROL INTERFACE

The clock generator is a slave I<sup>2</sup>C component, which can be read back the data, stored in the latches for verification. All proceeding bytes must be sent to change one of the control bytes. The 2-wire control interface allows each clock output individually enabled or disabled. On power up, the W83194R-39/-39A initializes with default register settings. Use of the 2-wire control interface is then optional.

The SDATA signal only changes when the SDCLK signal is low, and is stable when SDCLK is high during normal data transfer. There are only two exceptions. One is a high-to-low transition on SDATA while SDCLK is high used to indicate the beginning of a data transfer cycle. The other is a low-to-high transition on SDATA while SDCLK is high used to indicate the end of a data transfer cycle. Data is always sent as complete 8-bit bytes followed by an acknowledge generated.

Byte writing starts with a start condition followed by 7-bit slave address and a write command bit [1101 0010], command code checking [0000 0000], and byte count checking. After successful reception of each byte, an acknowledge (low) on the SDATA wire will be generated by the clock chip. Controller can start to write to internal I<sup>2</sup>C registers after the string of data. The sequence order is as follows:

Bytes sequence order for I<sup>2</sup>C controller:

Clock Address A(6:0) & R/W	Ack	8 bits dummy Command code	Ack	8 bits dummy Byte count	Ack	Byte0,1,2... until Stop
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Set R/W to 1 when read back", the data sequence is as follows:

Clock Address A(6:0) & R/W	Ack	Byte 0	Ack	Byte 1	Ack	Byte2, 3, 4... until Stop
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## 8.3 SERIAL CONTROL REGISTERS

The Pin column lists the affected pin number and the @PowerUp column gives the default state at true power up. "Command Code" byte and "Byte Count" byte must be sent following the acknowledge of the Address Byte. Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledge. After that, the sequence described below (Register 0, Register 1, Register 2...) will be valid and acknowledged.

### 8.3.1 Register 0: CPU Frequency Select Register (default = 0)

Bit	@PowerUp	Pin	Description
7	0	-	0 = $\pm 0.25\%$ Spread Spectrum Modulation 1 = $\pm 0.5\%$ Spread Spectrum Modulation
6	0	-	SSEL2 (for frequency table selection by software via I <sup>2</sup> C)
5	0	-	SSEL1 (for frequency table selection by software via I <sup>2</sup> C)
4	0	-	SSEL0 (for frequency table selection by software via I <sup>2</sup> C)
3	0	-	0 = Selection by hardware 1 = Selection by software I <sup>2</sup> C - Bit 6:4
2	0	-	SSEL3 (for frequency table selection by software via I <sup>2</sup> C)
1	0	-	0 = Normal 1 = Spread Spectrum enabled
0	0	-	0 = Running 1 = Tristate all outputs

Note: The frequency table selected by software via I<sup>2</sup>C is the same as the hardware setting frequency table.

### 8.3.2 Register 1: CPU, 48/24 MHz Clock Register (1 = enable, 0 = Stopped)

Bit	@PowerUp	Pin	Description
7	X	-	Latched FS2#
6	1	-	Reserved
5	1	-	Reserved
4	1	-	Reserved
3	1	40	SDRAM12 (Active / Inactive)
2	1	-	Reserved
1	1	43	CPUCLK1 (Active / Inactive)
0	1	44	CPUCLK_F (Active / Inactive)

### 8.3.3 Register 2: PCI Clock Register (1 = enable, 0 = Stopped)

Bit	@PowerUp	Pin	Description
7	1	-	Reserved
6	1	7	PCICLK_F (Active / Inactive)
5	1	-	Reserved
4	1	14	PCICLK4 (Active / Inactive)
3	1	12	PCICLK3 (Active / Inactive)
2	1	11	PCICLK2 (Active / Inactive)
1	1	10	PCICLK1 (Active / Inactive)
0	1	8	PCICLK0 (Active / Inactive)

**8.3.4 Register 3: SDRAM Clock Register (1 = enable, 0 = Stopped)**

Bit	@PowerUp	Pin	Description
7	1	-	Reserved
6	X	-	Latched FS0#
5	1	26	48MHz (Active / Inactive)
4	1	25	24MHz (Active / Inactive)
3	1	-	Reserved
2	1	21,20,18,17	SDRAM (8:11) (Active / Inactive)
1	1	32,31,29,28	SDRAM (4:7) (Active / Inactive)
0	1	38,37,35,34	SDRAM (0:3) (Active / Inactive)

**8.3.5 Register 4: Reserved Register (1 = enable, 0 = Stopped)**

Bit	@PowerUp	Pin	Description
7	1	-	Reserved
6	1	-	Reserved
5	1	-	Reserved
4	1	-	Reserved
3	X	-	Latched FS1#
2	1	-	Reserved
1	X	-	Latched FS3#
0	1	-	Reserved

**8.3.6 Register 5: Peripheral Control (1 = enable, 0 = Stopped)**

Bit	@PowerUp	Pin	Description
7	1	-	Reserved
6	1	-	Reserved
5	1	-	Reserved
4	1	47	IOAPIC (Active / Inactive)
3	1	-	Reserved
2	1	-	Reserved
1	1	46	REF1 (Active / Inactive)
0	1	2	REF0 (Active / Inactive)

## 9.0 SPECIFICATIONS

### 9.1 ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in this table may cause permanent damage to the device. Precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. Subjection to maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level (Ground or Vdd).

Symbol	Parameter	Rating
Vdd , V <sub>IN</sub>	Voltage on any pin with respect to GND	- 0.5 V to + 7.0 V
T <sub>STG</sub>	Storage Temperature	- 65°C to + 150°C
T <sub>B</sub>	Ambient Temperature	- 55°C to + 125°C
T <sub>A</sub>	Operating Temperature	0°C to + 70°C

### 9.2 AC CHARACTERISTICS

Vdd = Vddq3 = 3.3V ± 5 %, Vddq2 = VddL1=VddL2 = 2.375V~2.9V, T <sub>A</sub> = 0°C to +70°C						
Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Output Duty Cycle		45	50	55	%	Measured at 1.5V
CPU/SDRAM to PCI Offset	t <sub>OFF</sub>	1		4	ns	15 pF Load Measured at 1.5V
Skew (CPU-CPU), (PCI-PCI), (SDRAM-SDRAM)	t <sub>SKEW</sub>			250	ps	15 pF Load Measured at 1.5V
CPU/SDRAM Cycle to Cycle Jitter	t <sub>CCJ</sub>			±250	ps	
CPU/SDRAM Absolute Jitter	t <sub>JA</sub>			500	ps	
Jitter Spectrum 20 dB Bandwidth from Center	BW <sub>J</sub>			500	KHz	
Output Rise (0.4V ~ 2.0V) & Fall (2.0V ~ 0.4V) Time	t <sub>TLH</sub> t <sub>THL</sub>	0.4		1.6	ns	15 pF Load on CPU and PCI outputs
Overshoot/Undershoot Beyond Power Rails	V <sub>over</sub>	0.7		1.5	V	22 Ω at source of 8 inch PCB run to 15 pF load
Ring Back Exclusion	V <sub>RBE</sub>	0.7		2.1	V	Ring Back must not enter this range.

### 9.3 DC CHARACTERISTICS

<b>Vdd = Vddq3 = 3.3V <math>\pm</math> 5 %, Vddq2 = VddL1=VddL2 = 2.375V~2.9V, T<sub>A</sub> = 0 °C to +70 °C</b>						
Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Input Low Voltage	V <sub>IL</sub>			0.8	V <sub>dc</sub>	
Input High Voltage	V <sub>IH</sub>	2.0			V <sub>dc</sub>	
Input Low Current	I <sub>IL</sub>			-66	μA	
Input High Current	I <sub>IH</sub>			5	μA	
Output Low Voltage I <sub>OL</sub> = 4 mA	V <sub>OL</sub>			0.4	V <sub>dc</sub>	All outputs
Output High Voltage I <sub>OH</sub> = 4mA	V <sub>OH</sub>	2.4			V <sub>dc</sub>	All outputs using 3.3V power
Tri-State leakage Current	I <sub>oz</sub>			10	μA	
Dynamic Supply Current for Vdd + Vddq3	I <sub>dd3</sub>				mA	CPU = 66.6 MHz PCI = 33.3 Mhz with load
Dynamic Supply Current for Vddq2 + Vddq2b	I <sub>dd2</sub>				mA	Same as above
CPU Stop Current for Vdd + Vddq3	I <sub>CPUS3</sub>				mA	Same as above
CPU Stop Current for Vddq2 + Vddq2b	I <sub>CPUS2</sub>				mA	Same as above
PCI Stop Current for Vdd + Vddq3	I <sub>PD3</sub>				mA	

### 9.4 BUFFER CHARACTERISTICS

#### 9.4.1 TYPE 1 BUFFER FOR CPU CLOCK

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Pull-Up Current Min	I <sub>OH(min)</sub>	-27			mA	V <sub>out</sub> = 1.0 V
Pull-Up Current Max	I <sub>OH(max)</sub>			-27	mA	V <sub>out</sub> = 2.0V
Pull-Down Current Min	I <sub>OL(min)</sub>				mA	V <sub>out</sub> = 1.2 V
Pull-Down Current Max	I <sub>OL(max)</sub>			27	mA	V <sub>out</sub> = 0.3 V
Rise/Fall Time Min Between 0.4 V and 2.0 V	T <sub>RF(min)</sub>	0.4			ns	10pF Load
Rise/Fall Time Max Between 0.4 V and 2.0 V	T <sub>RF(max)</sub>			1.6	ns	20pF Load

**9.4.2 TYPE 2 BUFFER FOR IOAPIC**

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Pull-Up Current Min	I <sub>OH(min)</sub>				mA	V <sub>out</sub> = 1.4 V
Pull-Up Current Max	I <sub>OH(max)</sub>			-29	mA	V <sub>out</sub> = 2.7 V
Pull-Down Current Min	I <sub>OL(min)</sub>				mA	V <sub>out</sub> = 1.0 V
Pull-Down Current Max	I <sub>OL(max)</sub>			28	mA	V <sub>out</sub> = 0.2 V
Rise/Fall Time Min Between 0.7 V and 1.7 V	T <sub>RF(min)</sub>	0.4			ns	10pF Load
Rise/Fall Time Max Between 0.7 V and 1.7 V	T <sub>RF(max)</sub>			1.8	ns	20pF Load

**9.4.3 TYPE 3 BUFFER FOR REF1, 24MHZ, 48MHZ**

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Pull-Up Current Min	I <sub>OH(min)</sub>	-29			mA	V <sub>out</sub> = 1.0 V
Pull-Up Current Max	I <sub>OH(max)</sub>			-23	mA	V <sub>out</sub> = 3.135V
Pull-Down Current Min	I <sub>OL(min)</sub>	29			mA	V <sub>out</sub> = 1.95 V
Pull-Down Current Max	I <sub>OL(max)</sub>				mA	V <sub>out</sub> = 0.4 V
Rise/Fall Time Min Between 0.8 V and 2.0 V	T <sub>RF(min)</sub>	1.0			ns	10pF Load
Rise/Fall Time Max Between 0.8 V and 2.0 V	T <sub>RF(max)</sub>			4.0	ns	20pF Load

**9.4.4 TYPE 4 BUFFER FOR SDRAM (0:12)**

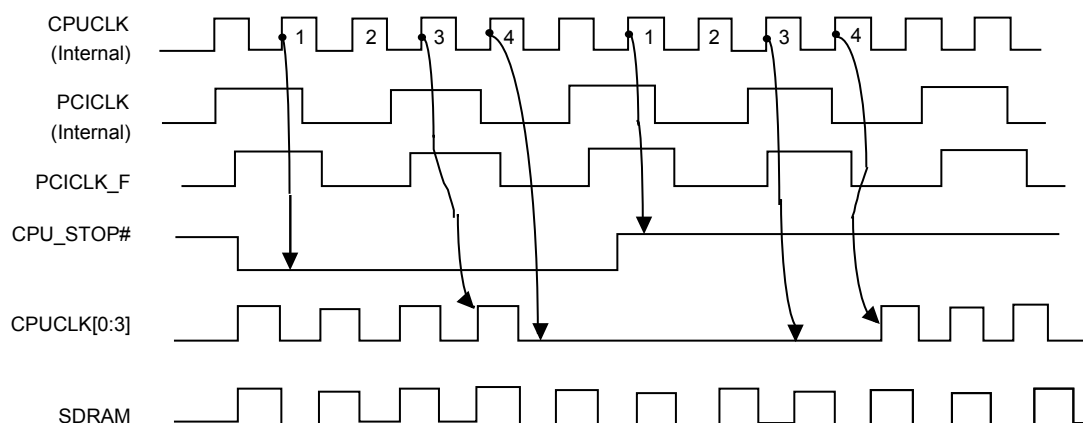
Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Pull-Up Current Min	I <sub>OH(min)</sub>				mA	V <sub>out</sub> = 1.65 V
Pull-Up Current Max	I <sub>OH(max)</sub>			-46	mA	V <sub>out</sub> = 3.135 V
Pull-Down Current Min	I <sub>OL(min)</sub>				mA	V <sub>out</sub> = 1.65 V
Pull-Down Current Max	I <sub>OL(max)</sub>			53	mA	V <sub>out</sub> = 0.4 V
Rise/Fall Time Min Between 0.8 V and 2.0 V	T <sub>RF(min)</sub>	0.5			ns	20pF Load
Rise/Fall Time Max Between 0.8 V and 2.0 V	T <sub>RF(max)</sub>			1.3	ns	30pF Load

### 9.4.5 TYPE 5 BUFFER FOR PCICLK (0:4,F)

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Pull-Up Current Min	$I_{OH(min)}$	-33			mA	$V_{out} = 1.0\text{ V}$
Pull-Up Current Max	$I_{OH(max)}$			-33	mA	$V_{out} = 3.135\text{ V}$
Pull-Down Current Min	$I_{OL(min)}$	30			mA	$V_{out} = 1.95\text{ V}$
Pull-Down Current Max	$I_{OL(max)}$			38	mA	$V_{out} = 0.4\text{ V}$
Rise/Fall Time Min Between 0.8 V and 2.0 V	$T_{RF(min)}$	0.5			ns	15pF Load
Rise/Fall Time Max Between 0.8 V and 2.0 V	$T_{RF(max)}$			2.0	ns	30pF Load

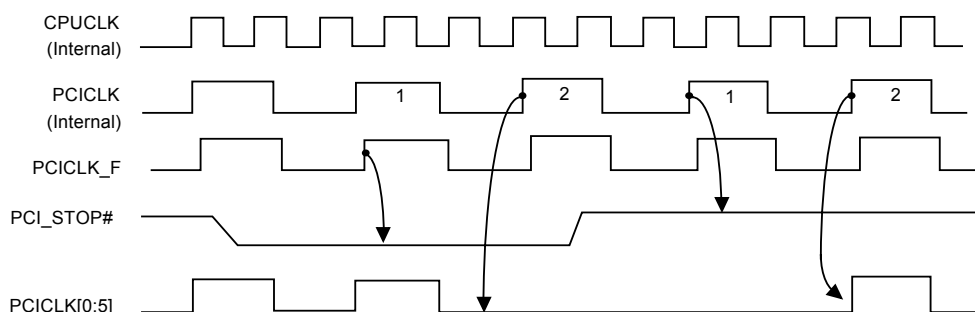
## 10.0 POWER MANAGEMENT TIMING

### 10.1 CPU\_STOP# Timing Diagram



For synchronous Chipset, CPU\_STOP# pin is an asynchronous “ active low ” input pin used to stop the CPU clocks for low power operation. This pin is asserted synchronously by the external control logic at the rising edge of free running PCI clock (PCICLK\_F). All other clocks will continue to run while the CPU clocks are stopped. The CPU clocks will always be stopped in a low state and resume output with full pulse width. In this case, CPU clocks on latency” is less than 4 CPU clocks and locks off latency” is less than 4 CPU clocks.

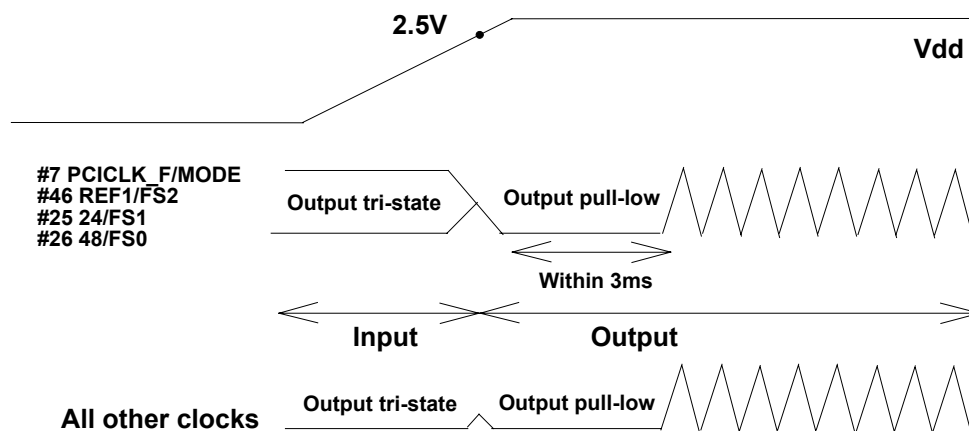
## 10.2 PCI\_STOP# Timing Diagram



For synchronous Chipset, PCI\_STOP# pin is an asynchronous "active low" input pin used to stop the PCICLK [0:4] for low power operation. This pin is asserted synchronously by the external control logic at the rising edge of free running PCI clock (PCICLK\_F). All other clocks will continue to run while the PCI clocks are stopped. The PCI clocks will always be stopped in a low state and resume output with full pulse width. In this case, PCI "locks on latency" is less than 2 PCI clocks and "locks off latency" is less than 2 PCI clocks.

## 11.0 OPERATION OF DUAL FUNCTION PINS

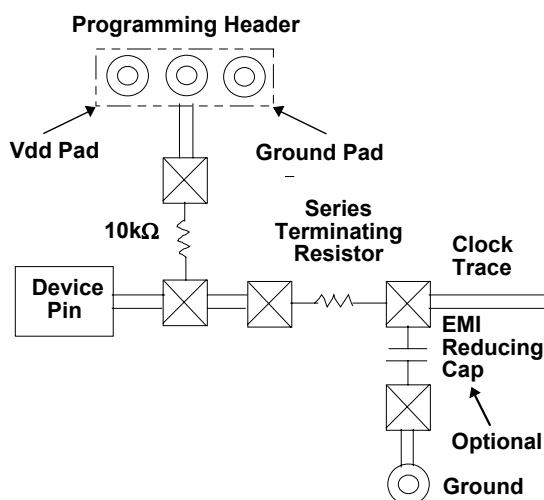
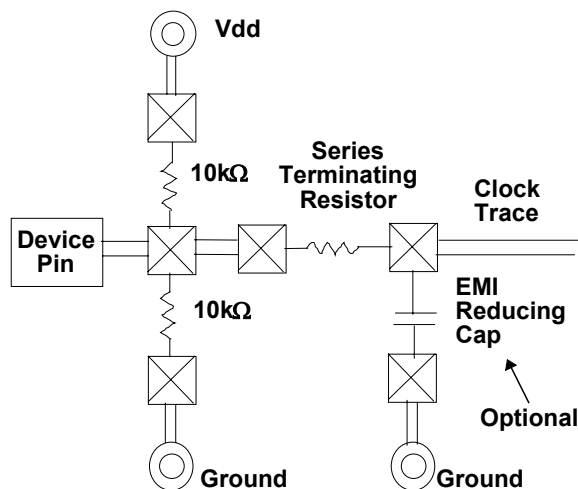
Pins 2, 7, 8, 25, and 26 are dual function pins and are used for selecting different functions in this device (see Pin description). During power up, these pins are in input mode (see Fig1), therefore, and are considered input select pins. When Vdd reaches 2.5V, the logic level that is present on these pins is latched into their appropriate internal registers. Once the correct information is properly latched, these pins will change into output pins and will be pulled low by default. At the end of the power up timer (within 3 ms) outputs starts to toggle at the specified frequency.



Each of these pins has a large pull-up resistor (250 kΩ @3.3V) inside. The default state will be logic 1, but the internal pull-up resistor may be too large when long traces or heavy load appear on these

dual function pins. Under these conditions, an external 10 k $\Omega$  resistor is recommended to be connected to Vdd if logic 1 is expected. Otherwise, there should be direct connection to ground if logic 0 is desired. The 10 k $\Omega$  resistor should be placed before the series terminating resistor. Note that this logic will only be latched at initial power on.

If optional EMI reducing capacitor is needed, they should be placed as close to the series terminating resistor as possible and after the series-terminating resistor. These capacitors have typical values ranging from 4.7pF to 22pF.



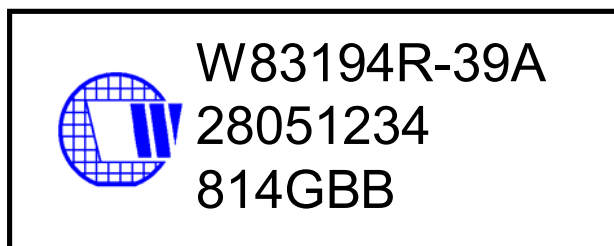
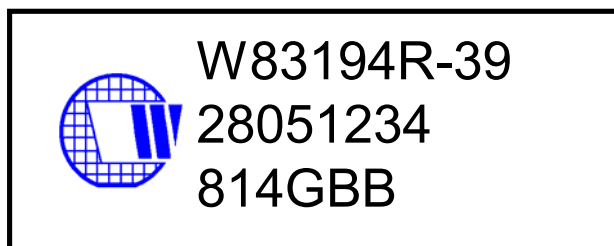
## 13.0 ORDERING INFORMATION

# W83194R-39/-39A



Part Number	Package Type	Production Flow
W83194R-39/-39A	48 PIN SSOP	Commercial, 0°C to +70°C

## 14.0 HOW TO READ THE TOP MARKING



1st line: Winbond logo and the type number: W83194R-39/-39A

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 814 G B B

814: packages made in '98, week 14

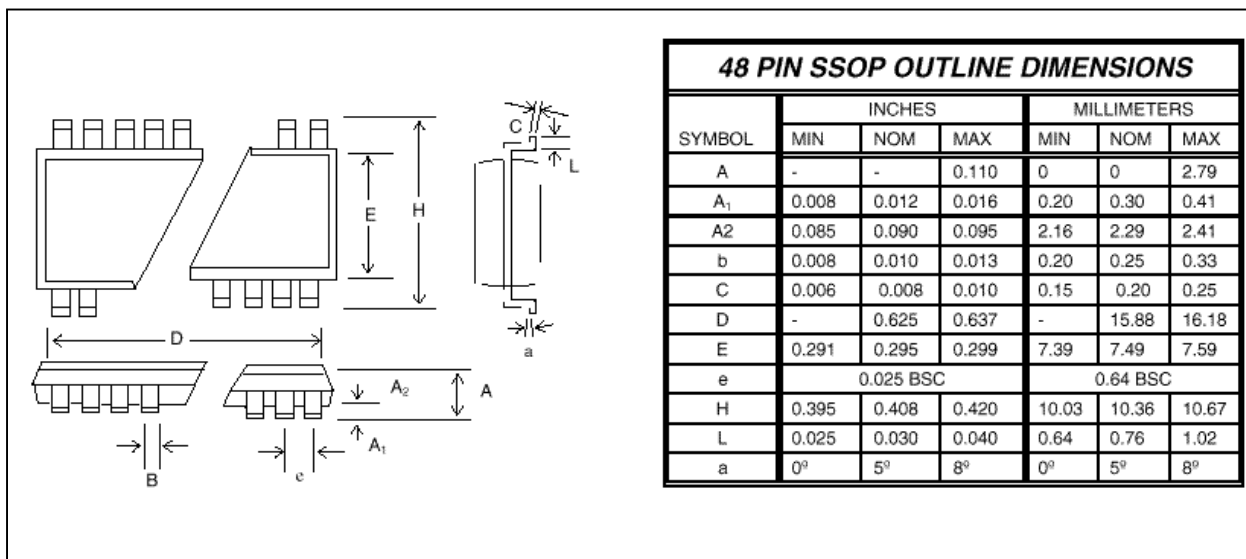
G: assembly house ID; A means ASE, S means SPIL, G means GR

BB: IC revision

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## 15.0 PACKAGE DRAWING AND DIMENSIONS

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Revision 1.0



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