QDS1F Device
QUAD DS1 Framer
TXC-03102

DATA SHEET
Preliminary

FEATURES

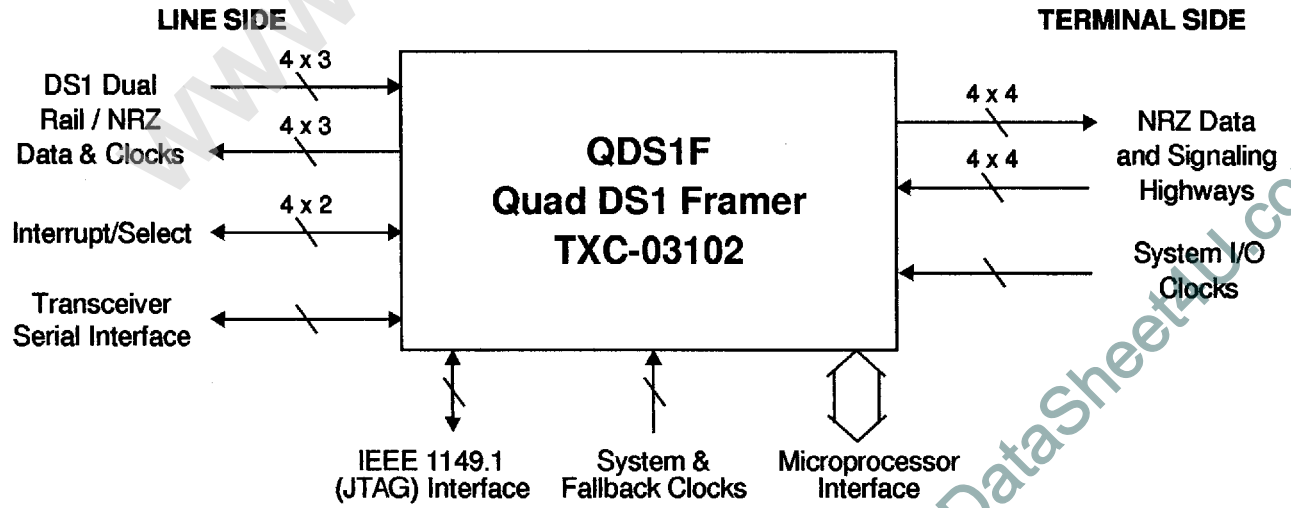
- D4 SF, ESF (including FDL support), and transparent framing modes
- Encodes/decodes AMI/B8ZS and forced ones density line codes
- Two frame slip buffers in both receive and transmit directions
- Supports channel-associated and robbed-bit signaling (enabled or processor forced on a per DS0 basis)
- Detects and forces yellow and AIS alarms; detects OOF, SEF, and change of frame alignment
- Detects, counts and forces line code errors (BPVs and excess zeros), CRC errors (ESF only), and frame bit errors
- Motorola/Intel compatible microprocessor interface
- One-second interrupt input latches counter values and line events into shadow registers
- Local, line remote, and payload remote loopback
- Processor forcing/monitoring of DS0s for maintenance purposes
- Boundary scan capability (IEEE 1149.1)
- 128-pin plastic quad flat package

DESCRIPTION

The QDS1F is a 4-channel DS1 (1.544 Mbit/s) framer designed for voice and data communications applications. AMI, B8ZS, and NRZ line codes are supported with full alarm detection and generation per ANSI T1M1.3. The transmit and receive sections of each of the four framers are independent, with individual slip buffers to allow operation in a wide range of switching and transmission products. D4 SF and ESF modes are provided per ANSI T1.403 - 1989 and AT&T PUB 62411, with per DS0 signaling and DS0 data access and control via a Motorola/Intel-compatible microprocessor. For ESF applications, each framer supplies a full duplex HDLC/bit-oriented message controller in addition to on-board latching of all required performance parameters; minimal software overhead is required to support either ANSI T1.403-1989 or AT&T PUB 54016 protocols. Diagnostic, test, and maintenance functions are provided, including loopbacks and boundary scan (IEEE 1149.1).

APPLICATIONS

- SONET/SDH terminal or add/drop multiplexers supporting DS1 byte synchronous operation
- DCS, digital central office or remote digital terminals
- T1 multiplexers
- T1 and fractional T1 CSUs
- ATM products with integrated DS1 interfaces
- LAN routers with integrated DS1 interfaces
- Multichannel DS1 test equipment



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QUAD DS1 FRAMER FEATURES

The Quad DS1 Framer (QDS1F) device is a highly-featured DS1 framer for use in a wide variety of interface, transmission and switching applications. Four independent DS1 framers are provided in a single monolithic VLSI device using sub-micron CMOS technology. Powered from a single +5.0 volt supply, the four framers dissipate less than half a watt typically. The QDS1F is provided in a rectangular 128-pin plastic quad flat package. Its operating temperature range extends from -40°C to +85°C.

The QDS1F device has been designed to meet the latest industry standards, namely:

- ANSI T1.403 and T1M1.3
- Bellcore TR-TSY 000499
- AT&T Pub. 62411 and Pub. 54016
- IEEE 1149.1

The following features are independently selectable for each of the four DS1 framers:

Framing Modes:

- D4 SF programmable for Fs, Ft or both frame bits
- ESF with or without CRC
- Unframed (bypass)
- SLC 96, T1DM and other SF modes with external logic

Line Codes:

- AMI
- B8ZS
- AMI with forced ones density
- NRZ (bypass)
- Selectable polarity (NRZ) and clock edges

Signaling:

- A, AB (SF)
- A, AB, ABCD (ESF)
- Per DS0 enable with microprocessor read and substitution in both receive and transmit directions
- Signaling freeze on LOS

Clock Management:

- Flexible receive and transmit clock selection, including local oscillator
- Two frame slip buffers for each of receive and transmit paths, with independent bypass
- System side and line side clocks on receive and transmit, each independent

Alarms and Errors:

- Detect and force yellow and blue (AIS) alarms
- Detect Out Of Frame, Loss Of Signal, Severely Errored Frame and Change of Frame Alignment
- Detect, count and force CRC errors (ESF only), frame bit errors and line code errors (bipolar violations, with or without excessive zeros)
- Detect and force frame slips

DS0 Control:

- Per DS0 enable (independent receive and transmit) with microprocessor read and substitution in both receive and transmit directions

Maintenance:

- Loopbacks - line remote, local and payload (ESF only)
- Detect and transmit SF loop-up and loop-down codes
- Full duplex HDLC controller with bit-oriented code support for facility data link and 16-byte receive and transmit FIFOs

Microprocessor Interface:

- Eight-bit status register with eight-bit mask register
- Latched event registers for each status bit
- CRC (ESF only), code violation and frame bit error counters
- Shadow registers and counters
- Full control of framing, alarm generation and propagation, codec features
- FDL control, signaling access/control, DS0 access/control
- Reset, resync, slip buffer and frame bit access

The following features are only selectable for the four framers as a group:

- Transmission mode ("off line" framing) or MVIP mode system interfaces
- Serial port to read/write control up to four line interface transceivers, or selection of one of four DS1 line interfaces (receive or transmit) to monitor clock and data
- Microprocessor global reset, masks, polling registers, interrupt polarity and latch edge control
- Two reference clock outputs at 8kHz or 1544 kHz with freeze on LOS
- IEEE 1149.1 boundary scan
- Motorola or Intel microprocessor access with separate address and data buses
- Ability to tri-state all outputs for in-circuit testing
- Ability to place line side transmit clock and data to logic low for protection switching
- Synchronization start position is programmable to any receive or transmit bit position on the system side
- External shadow register clock input
- Pseudo-Random Binary Sequence (PRBS) generator and analyzer

BLOCK DIAGRAM

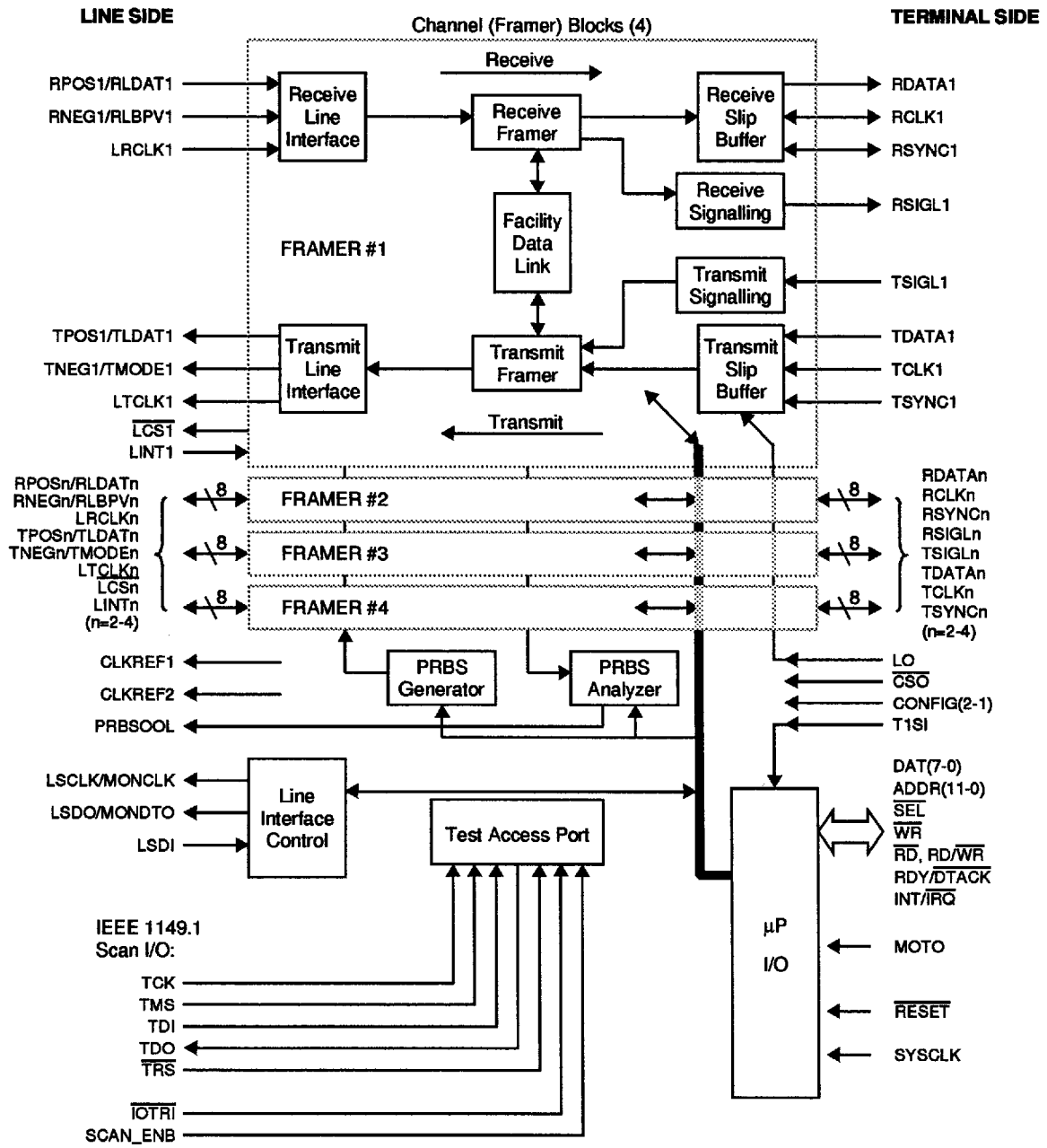


Figure 1. QDS1F TXC-03102 Block Diagram

BLOCK DIAGRAM DESCRIPTION

A simplified block diagram of the QDS1F device is shown in Figure 1. The major blocks are the Microprocessor Input/Output Interface (µP I/O), the Line Interface Control, the PRBS generator and the PRBS analyzer, four Channel (Framer) blocks and the Test Access Port. These blocks are described in detail below. For additional information, reference may be made to the Pin Descriptions, Timing Characteristics (Figures 14 - 28), Memory Map and Memory Map Descriptions sections of this Data Sheet.

MICROPROCESSOR INPUT/OUTPUT INTERFACE BLOCK

The Microprocessor Input/Output Interface allows access and control for each of the four DS1 framers. Alarm information detected by the framers can be read as current status and latched in event registers. Either the arrival or the departure of a condition can be individually enabled for setting the event register. To facilitate either interrupt or polled systems, global interrupt masks, per channel interrupt masks, global event and global polling registers are provided. To assist in the collection of performance parameters, shadow registers and counter latching are provided. The configuration of each framer is provided by this interface, as well as control of the Facility Data Link block for each framer. The Receive Line Interface and Transmit Line Interface blocks are also controlled by the Microprocessor Input/Output Interface. The microprocessor bus supports both Motorola and Intel style processors with a minimum amount of interface logic. An external pin (MOTO) configures the type of bus supported. The data bus DAT(7-0) is an 8-bit, bi-directional, tri-state port. The internal control and status registers are accessed through this port. When not accessed, this port is in a high impedance state. The address bus ADDR(11-0) is a 12-bit input port. These pins select individual control and status registers within the framer. $\overline{SEL}$ is the microprocessor port select signal. $\overline{WR}$ is the Intel microprocessor port write signal and $\overline{RD}$,RD/$\overline{WR}$ is the Intel read and Motorola read/write signal. RDY/ $\overline{DTACK}$ is used to delay microprocessor access if required to access internal registers. INT/$\overline{IRQ}$ is the microprocessor port interrupt line. $\overline{RESET}$ is the overall device reset line and SYSCLK is a high speed system clock used by all blocks.

Global controls for reset are provided at memory address 005H (the suffix H indicates a hexadecimal number throughout this Data Sheet)). Register 006H allows the interrupt to be turned off (GIM bit), the polarity and active edge for latching to be controlled (IPOL, RISE and FALL bits) and performance and fault monitoring functions, together with the hardware mask, to be turned on (ENPMFM and ENHWM bits).

For a view of all QDS1F framers and control the following registers are provided:

Register 00AH is an or-gated value of each framer's event register. Loss Of Signal, Alarm Indication Signal, Out Of Frame, Yellow Alarm, Severely Errored Frame, Change of Frame Alignment, Receive Slip and Transmit Slip are all provided.

Register 00BH provides a mask for each condition covering all four framers (per-framer masks are also provided at register X09H).

Register 00CH contains channel activity indicating interrupts from alarms.

Register 00EH provides activity information, but only for facility data link (FDL) interrupts. This allows software to control line status and FDL status separately.

LINE INTERFACE CONTROL AND DS1 MONITOR

The Line Interface Control block is a serial interface that is used to control and manage the external analog line transceivers operating in the host mode. This allows the system processor to have complete control of the line transceiver through the QDS1F Microprocessor Input/Output Interface. The interface consists of a data input pin (LSDI), data output pin (LSDO), and serial clock (LSCLK) that are shared among all the transceivers. In addition, there is an individual chip select ($\overline{LCS}$) for each transceiver, and an individual input from each transceiver that may be used to generate an interrupt (LINT) that is part of the Line Interface block. Figure 2 below shows the serial interface operation. Note that control bit ESP initiates and terminates the sequence.

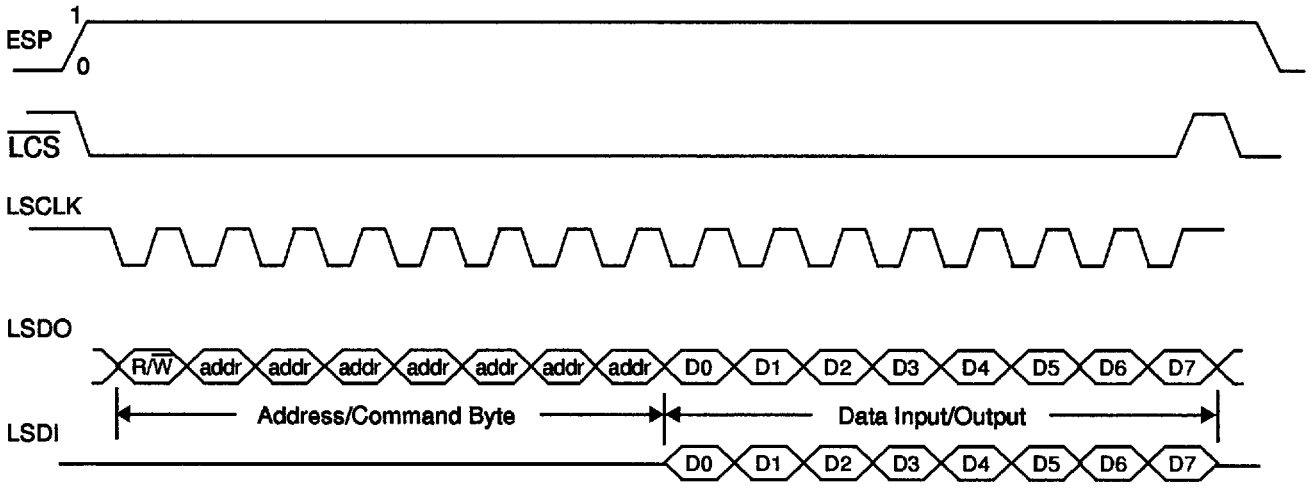


Figure 2. Serial Interface Operation

When the serial interface to the line transceivers is not used with the QDS1F (e.g., in an application using the TranSwitch M13E device), access to the DS1 transmit or receive clock and data is provided by microprocessor selection of the channel and direction. The signals are available on pins MONDTO and MONCLK. These pins are tri-stated when not selected, to allow multiple framers to share a DSX-1 line driver if desired. The monitored signals are selected after the decoding and before the encoding. This mode is mutually exclusive with the serial interface.

Control of the serial port or DS1 monitor function is provided by Microprocessor Input/Output Interface registers. "Command Byte" and "Line Interface Serial Data Output" (address 010H and 011H), "Line Interface Serial Data Output" (address 012H) and control bits for DS1 channel number, RXTX, ESP/EMON and BDCST (address 013H).

Reference Clock Outputs

To support system clock reference needs, the QDS1F device can provide two recovered receive clocks, LRCLK, from any of the four lines, as outputs on pins CLKREF1 and CLKREF2. The microprocessor interface can select the output frequency (1544 kHz or 8 kHz), the specific lines, and whether or not to tri-state both CLKREF1 and CLKREF2 to permit multiple QDS1F devices to share a common reference clock line. To facilitate clock holdover requirements, LOS (or LINT if enabled as LOS) will cause the specific CLKREF(1, 2) output to be tri-stated. A register at address 019H provides two pairs of bits that control which DS1 provides CLKREF1 and which DS1 provides CLKREF2. Individual enable bits, ENREF1 and ENREF2, are provided as well as a frequency selection bit, 1544KHZ, covering both reference outputs.

PSEUDO-RANDOM BINARY SEQUENCE (PRBS) GENERATOR AND ANALYZER

The PRBS Generator and Analyzer blocks provide the ability to test each channel (framer) using the local loopback feature provided. The output of the analyzer is brought out to a pin (PRBSOOL). The pattern is 2^{15}-1 bit pseudo- random sequence that follows the ITU-T 'O' recommendations (except that it is inverted).

Control bits PRBSFR, PRBSEN and DS1 channel number in a Microprocessor Input/Output Interface register (address 013H) provide control. Per channel bit INSPRBS (address X06H, where X=1 - 4, identifies the channel) controls per-framer insertion, which substitutes the PRBS pattern for the data from TDATAn. The analyzer is connected to the selected RDATAn output.

OVERVIEW OF THE RECEIVE AND TRANSMIT PATHS

The Receive and Transmit Line Interface Signals

The Receive Line Interface and Transmit Line Interface blocks of each of the four Channel (Framer) blocks consist of clock and data pins to the external Line Transceiver for each channel. These pins can be configured to operate in two modes, dual unipolar and NRZ. In the dual unipolar mode the individual positive and negative line pulses are converted to CMOS level signals (RPOS, RNEG) by an external Line Transceiver. Similarly, each CMOS output (TPOS, TNEG) is converted to positive and negative line pulses by an external Line Transceiver. In NRZ mode the external Line Transceiver performs the code conversion to/from AMI or B8ZS; here the input (RLDAT) contains a pulse for each line pulse regardless of polarity and the output (TLDAT) contains a pulse for each line pulse regardless of polarity. The Line Interface can be programmed in NRZ mode to handle these signals with either a pulse or lack of pulse as a valid "1" or a rising or falling clock edge as valid for sampling/outputting. Clock extraction (LRCLK) is also handled by the external Line Transceiver and this clock is used by the Line Interface block to clock either NRZ or dual unipolar signals to the Receive Line Interface of the Channel block. Clock from the Transmit Line Interface of the Channel block (LTCLK) is used to clock out the data, programmable on the rising or falling edge. Remote line loopback for each channel is handled in the Line Interface. In the NRZ mode the negative polarity input and output pins are used for other purposes; RLBPV input is used to count bipolar violations from an external Line Transceiver; TMODE is used as a spare output (e.g., to control an external Line Transceiver for AMI/B8ZS selection).

System Interface Signals

The system interface interconnects each of the framers with the rest of the system. For each framer there is a separate transmit and receive highway. Each highway consists of a data bus, a signaling bus, a clock, and a synchronization signal. Each data highway is connected to a two-frame slip buffer, and each signaling highway is connected to a 96-bit signaling buffer. There are two modes of operation for the system interface; the transmission mode and the MVIP mode. In the transmission mode, the system interface operates at approximately the same speed as the line, with signaling and alarms on the signaling highway; a 3 millisecond multiframe pulse is used to synchronize the interface, and use of the slip buffers is optional. In MVIP mode, the system interface operates at 2.048 MHz with DS0s on the data highway and signaling on the signaling highway; a 125-microsecond frame pulse is used to synchronize the interface, and use of the slip buffers is mandatory.

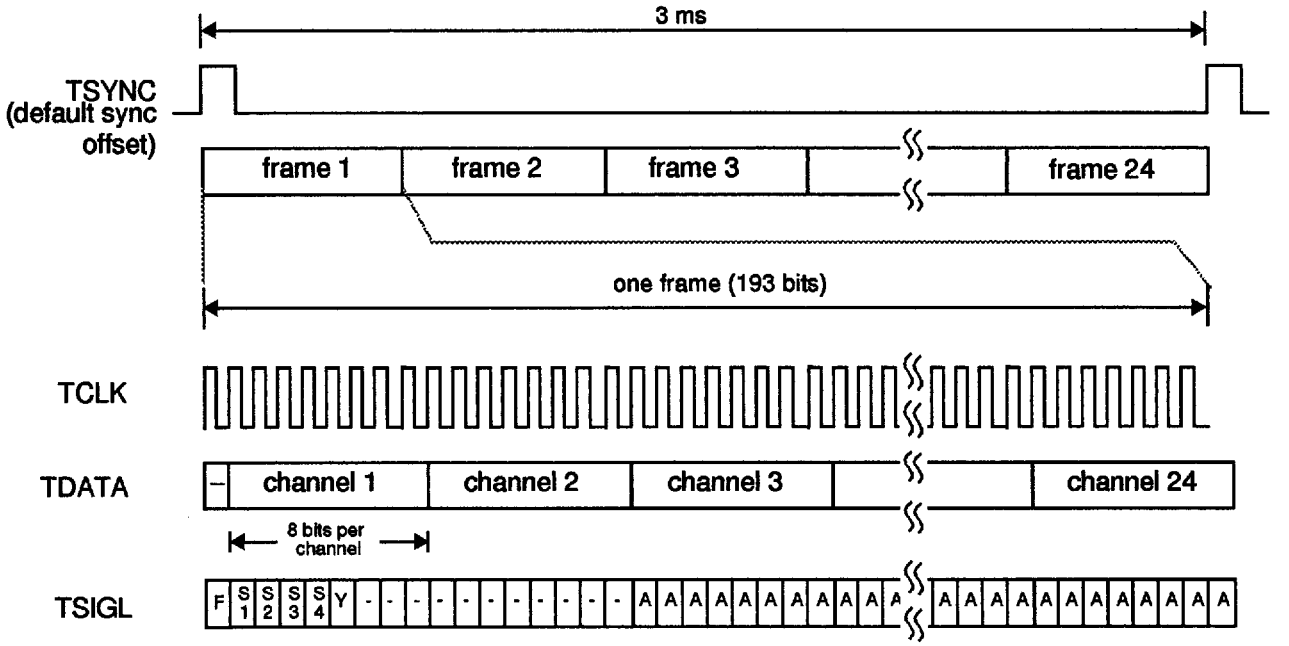
Transmission Mode ("Off Line" Framer Operation)

In transmission mode the transmit highway carries information from the system to the framer. The highway is sub-divided into two time division multiplexed buses, one for the data (TDATA), and one for signaling, frame bit and alarms (TSIGL). These two buses are synchronous with the signal TCLK, a 1.544 MHz clock, driven from the system. The transmit framing (data) format and signaling format are shown in the timing diagrams below, Figures 3 and 4.

The data highway is a single bit-serial bus organized into 193-bit groups called frames. Each frame consists of a spare bit position followed by twenty-four 8-bit data samples representing the 24 DS0s. There are 24 frames that form a multiframe, the beginning of which is identified by a synchronization pulse, TSYNC. TSYNC is programmable for the device to any bit position in the frame; the default position occurs one bit time before the first frame of the multiframe and every 24 frames after that. A register at address 017H provides TSYNC control (TSD7-TSD0).

The signaling highway, TSIGL, is also divided into 193-bit frames. Each frame consists of a frame bit followed by 192 bits of signaling and alarm information for the 24 data channels on the data highway. The frame bit pattern tracks the signaling bit pattern received from the system and may be used to send ESF FDL bits or SLC-96 control bits. The alarm bits in the signaling highway follow the signaling bits. In each frame of 193 bits, four signaling bits are transmitted followed by a yellow alarm bit position. The bit positions coincident with DS0 #3 through DS0 #24 are all used for the AIS alarm bit. Signaling bits A1 through A4 occur in frame number one, followed by A5 through A8 in frame number two, ending with D21 through D24 in frame number 24, corresponding to the ESF mode with 16-state signaling. For two- or four-state signaling the B, C and D bits or the C and D bits are replaced by A bits, or A and B bits, respectively. Two control bits in a register at address X00H, ENSYEL and ENSAIS, control the receipt of yellow alarm and AIS over the signaling highway. DS1 yellow will be transmitted if the yellow bit is set on the signaling highway and ENSYEL is set to one. Similarly, if ENSAIS is set to one, DS1 AIS will be transmitted on the line if the AIS bit is set on the signaling highway (TSIGL).

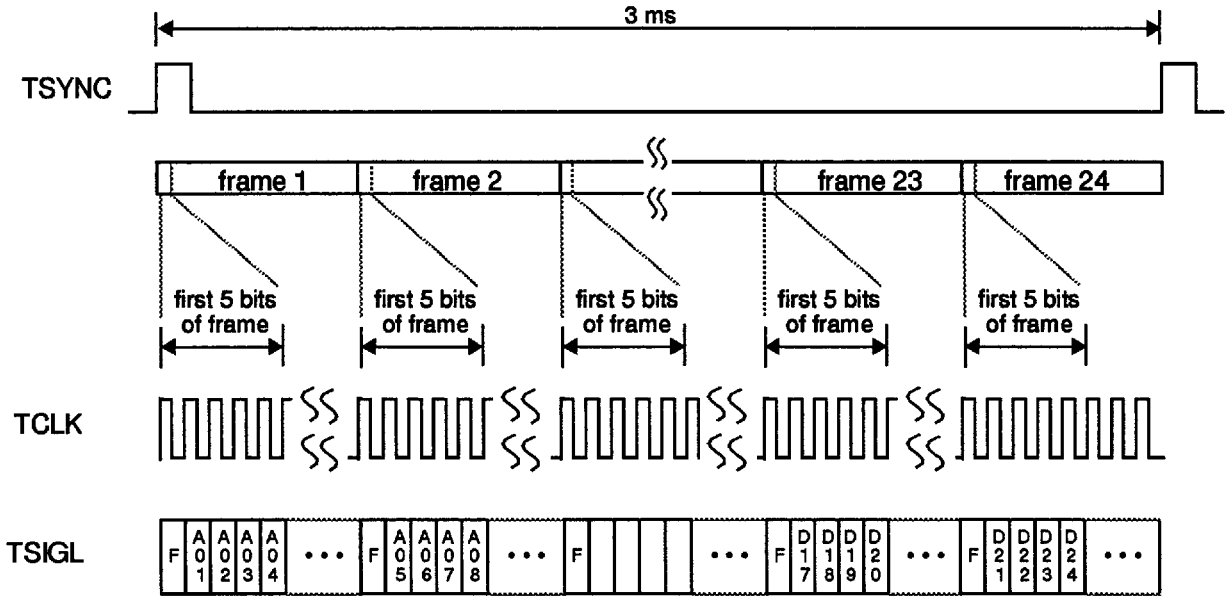
Figure 3. System Interface Transmit Framing Format for Transmission Mode



F = frame bit; A = AIS; Y = Yellow alarm; S1, S2, S3, S4 = signalling bits; - = not assigned

Signaling bit positions on TSIGL and RSIGL

Frame	SF/ESF	16-St. TSIGL; S_1-S_4	RSIGL; S_1-S_4	4-State; S_1-S_4	2-State; S_1-S_4
1	Ft/DI	A1, A2, A3, A4	A1, A2, A3, A4	A1, A2, A3, A4	A1, A2, A3, A4
2	Fs/CRC	A5, A6, A7, A8	A5, A6, A7, A8	A5, A6, A7, A8	A5, A6, A7, A8
3	Ft/DI	A9, A10, A11, A12	A9, A10, A11, A12	A9, A10, A11, A12	A9, A10, A11, A12
4	Fs/Ft	A13, A14, A15, A16	A13, A14, A15, A16	A13, A14, A15, A16	A13, A14, A15, A16
5	Ft/DI	A17, A18, A19, A20	A17, A18, A19, A20	A17, A18, A19, A20	A17, A18, A19, A20
6	Fs/CRC	A21, A22, A23, A24	A21, A22, A23, A24	A21, A22, A23, A24	A21, A22, A23, A24
7	Ft/DI	B1, B2, B3, B4	B1, B2, B3, B4	B1, B2, B3, B4	A1, A2, A3, A4
8	Fs/Ft	B5, B6, B7, B8	B5, B6, B7, B8	B5, B6, B7, B8	A5, A6, A7, A8
9	Ft/DI	B9, B10, B11, B12	B9, B10, B11, B12	B9, B10, B11, B12	A9, A10, A11, A12
10	Fs/CRC	B13, B14, B15, B16	B13, B14, B15, B16	B13, B14, B15, B16	A13, A14, A15, A16
11	Ft/DI	B17, B18, B19, B20	B17, B18, B19, B20	B17, B18, B19, B20	A17, A18, A19, A20
12	Fs/Ft	B21, B22, B23, B24	B21, B22, B23, B24	B21, B22, B23, B24	A21, A22, A23, A24
13	Ft/DI	C1, C2, C3, C4	C1, C2, C3, C4	A1, A2, A3, A4	A1, A2, A3, A4
14	Fs/CRC	C5, C6, C7, C8	C5, C6, C7, C8	A5, A6, A7, A8	A5, A6, A7, A8
15	Ft/DI	C9, C10, C11, C12	C9, C10, C11, C12	A9, A10, A11, A12	A9, A10, A11, A12
16	Fs/Ft	C13, C14, C15, C16	C13, C14, C15, C16	A13, A14, A15, A16	A13, A14, A15, A16
17	Ft/DI	C17, C18, C19, C20	C17, C18, C19, C20	A17, A18, A19, A20	A17, A18, A19, A20
18	Fs/CRC	C21, C22, C23, C24	C21, C22, C23, C24	A21, A22, A23, A24	A21, A22, A23, A24
19	Ft/DI	D1, D2, D3, D4	D1, D2, D3, D4	B1, B2, B3, B4	A1, A2, A3, A4
20	Fs/Ft	D5, D6, D7, D8	D5, D6, D7, D8	B5, B6, B7, B8	A5, A6, A7, A8
21	Ft/DI	D9, D10, D11, D12	D9, D10, D11, D12	B9, B10, B11, B12	A9, A10, A11, A12
22	Fs/CRC	D13, D14, D15, D16	D13, D14, D15, D16	B13, B14, B15, B16	A13, A14, A15, A16
23	Ft/DI	D17, D18, D19, D20	D17, D18, D19, D20	B17, B18, B19, B20	A17, A18, A19, A20
24	Fs/Ft	D21, D22, D23, D24	D21, D22, D23, D24	B21, B22, B23, B24	A21, A22, A23, A24



See table in Figure 3 for signaling bit assignment.

Figure 4. System Interface Transmit Signaling Format for Transmission Mode

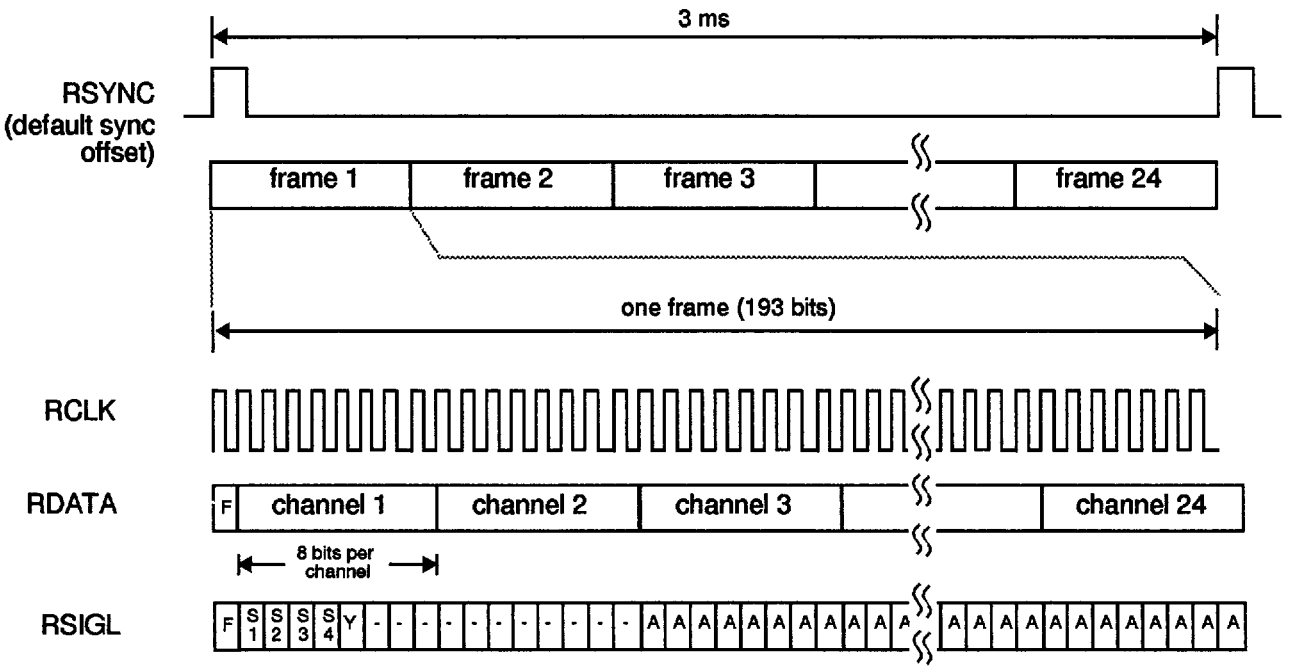
In transmission mode the receive highway carries information from the framer to the system. The highway is sub-divided into two time division multiplexed buses, one for the data (RDATA) and one for signaling, frame bits and alarms (RSIGL). These two buses are synchronous with the signal RCLK, a 1.544 MHz clock that is driven either from the system or the framer. The system interface receive framing (data) format and signaling format are shown in the timing diagrams below, Figures 5 and 6. The system will source the clock when the receive side slip buffer is enabled, and the framer will source the clock when the receive side slip buffer is bypassed.

The data highway is a single bit-serial bus that is organized into 193-bit groups called frames. Each frame consists of a frame bit followed by twenty-four 8-bit data samples. Each of the 8-bit data samples represents a single DS0 on the receive highway. The 193-bit frames are grouped into a 24-frame multiframe. In order to help locate the beginning of a frame and extract signaling information, the system or the framer sources a synchronization signal, RSYNC. RSYNC is programmable to any bit position in the frame; the default value occurs one bit time before the first frame in the multiframe and every 24 frames after that. A register at address 018H provides RSYNC control (RSD7-RSD0).

The signaling highway, RSIGL, is also divided into 193-bit frames and is organized in an identical fashion to TSIGL. AIS or Yellow alarms detected by the framer are sent out in the same positions as for TSIGL. The frame bits received from the line are available on RSIGL; they track the signaling bits and may be used for FDL extraction or SLC-96 control channel extraction.

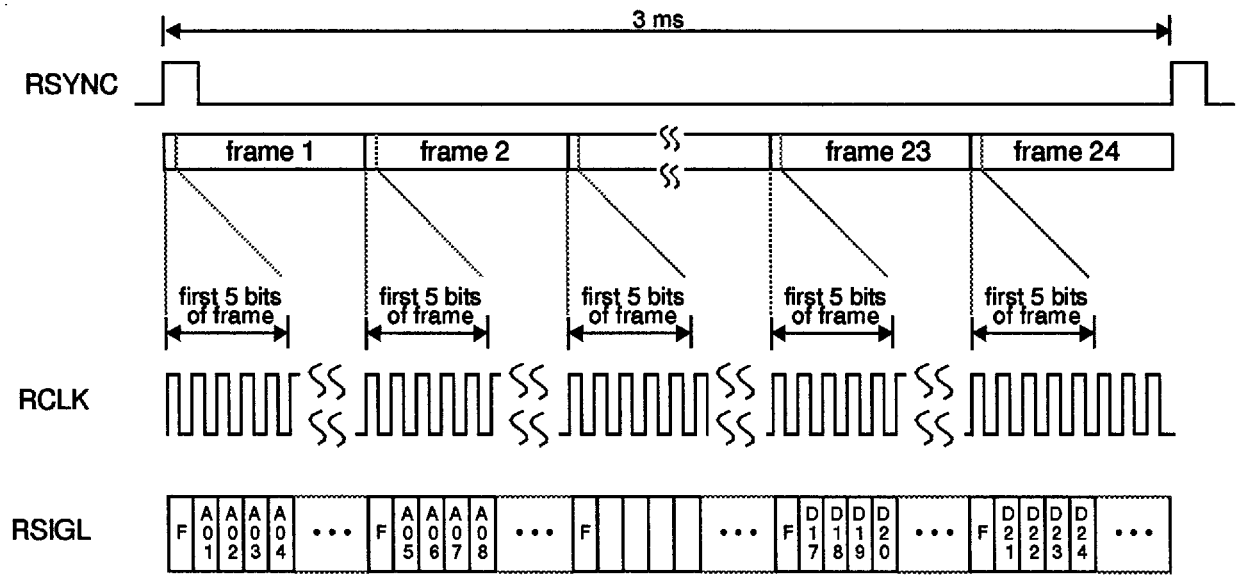
Several controls are provided for alarms sent on the alarm bit position of the signal highway. Bits ENAIS, ELOS and ENOOF allow AIS, LOS and OOF, respectively to set the AIS bit to 1 on the signaling highway (address X03H). Control bits SYSVTAIS and SYSALL1 (address X07H) allow a DS1 AIS to be generated to the system on receipt of an AIS condition or when forced by the Microprocessor Input/Output Interface.

Figure 5. System Interface Receive Framing Format for Transmission Mode



F = frame bit; A = AIS; Y = Yellow alarm; S1, S2, S3, S4 = signalling bits; - = not assigned

Figure 6. System Interface Receive Signaling Format for Transmission Mode



See table in Figure 3 for signaling bit assignment.

MVIP Mode

In MVIP mode the transmit highway carries information from the system to the framer. The highway is subdivided into two time division multiplexed buses, one for the data (TDATA), and one for signaling, TSIGL. These two buses are synchronous with the signal TCLK, a 2.048 MHz clock, driven from the system. The data highway is a single bit-serial bus organized into 256-bit groups called frames. Each frame consists of thirty two 8-bit data samples representing 32 DS0s. The 24 DS0s to be transmitted on the line are mapped to the 32 DS0s of the transmit data highway as follows:

Tran. Hwy Channel No.	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DS1 DS0 No.	X	1	2	3	X	4	5	6	X	7	8	9	X	10	11	12	X	13	14	15	X	16	17	18	X	19	20	21	X	22	23	24

The frame start is identified by a synchronization pulse, TSYNC, which occurs once per frame (125 microseconds). TSYNC is programmable for the device to any bit position in the frame; the default position occurs coincident with the first bit of transmit highway channel 0 (see control bits TSD7-TSD0 at address 017H). The signaling highway, TSIGL, is also divided into 256-bit frames. Each frame consists of 32 DS0 positions, 24 of which carry the ABCD signaling bits associated with the DS0s on the data highway. The same positions used for the DS0s are used for the signaling bits. The signaling bits occupy the last four bits of the DS0 on the signaling highway. The QDS1F updates its signaling buffer every other frame. The QDS1F can only update the line once every six frames for signaling. The transmit framing format and signaling format are shown in Figure 7.

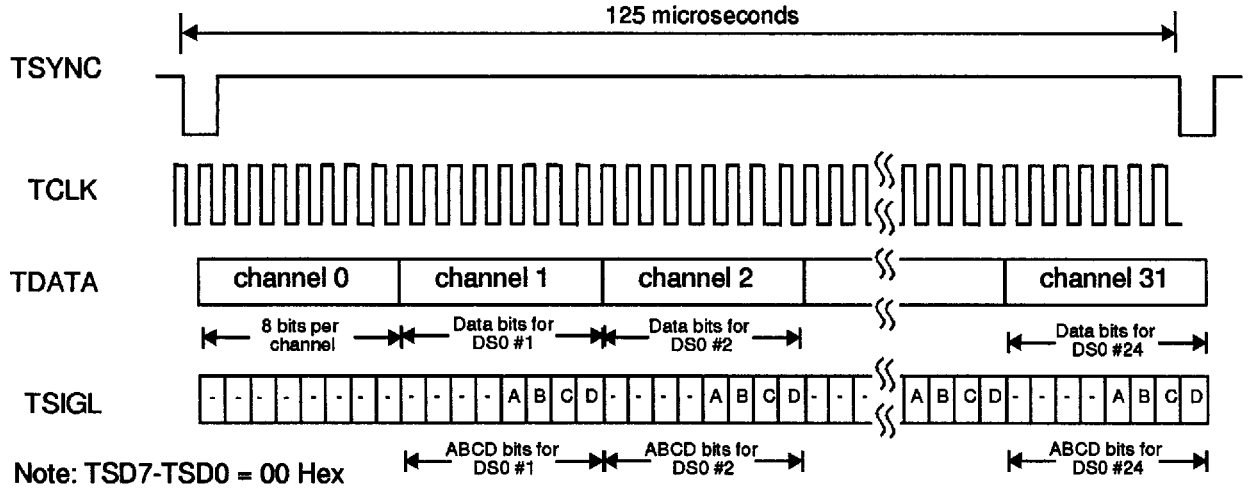
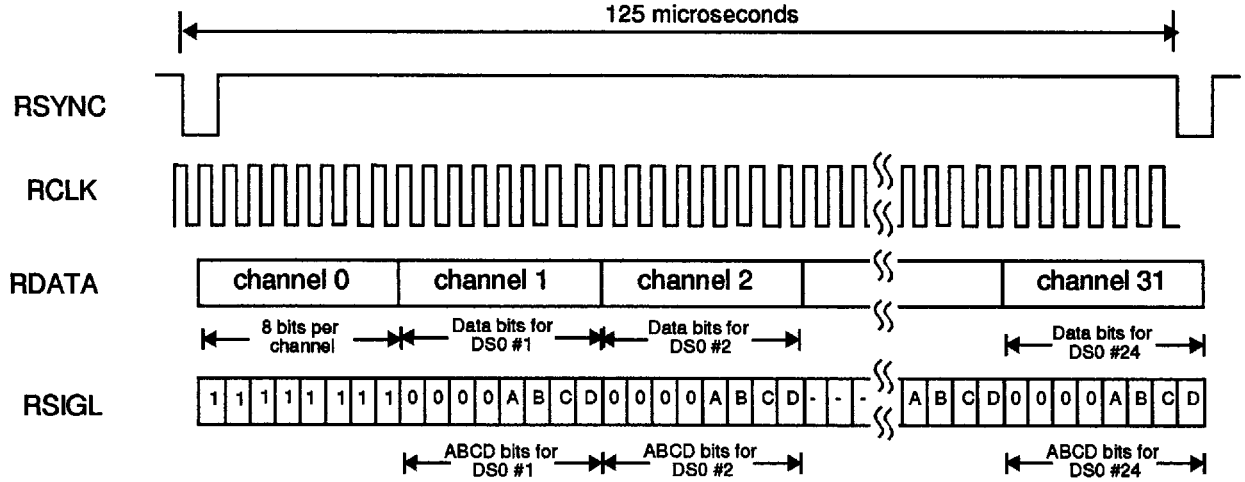


Figure 7. System Interface Transmit Format for MVIP Mode

In MVIP mode the receive highway carries information from the framer to the system. The highway is subdivided into two time division multiplexed buses, one for the data (RDATA), and one for signaling, RSIGL. These two buses are synchronous with the signal RCLK, a 2.048 MHz clock, driven from the system. The data highway is a single bit-serial bus organized into 256-bit groups called frames. Each frame consists of thirty two 8-bit data samples representing 32 DS0s. The 24 DS0s received from the line are mapped to the 32 DS0s of the receive data highway as follows:

Rec. Hwy Channel No.	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DS1 DS0 No.	X	1	2	3	X	4	5	6	X	7	8	9	X	10	11	12	X	13	14	15	X	16	17	18	X	19	20	21	X	22	23	24

The frame start is identified by a synchronization pulse, RSYNC, which occurs once per frame (125 microseconds) and is supplied by the system. RSYNC is programmable for the device to any bit position in the frame; the default position occurs coincident with the first bit of receive highway channel 0 (see control bits RSD7-RSD0 at address 017H). The signaling highway, RSIGL, is also divided into 256-bit frames. Each frame consists of 32 DS0 positions 24 of which carry the ABCD signaling bits associated with the DS0s on the data highway. The same positions used for the DS0s are used for the signaling bits. The signaling bits occupy the last four bits of the DS0 on the signaling highway. The QDS1F updates the signaling highway from its signaling buffer every frame. The QDS1F receive signaling buffer is only updated by the line once every six frames for signaling. The receive framing format and signaling format are shown in Figure 8.



Note: RSYNC and RCLK are inputs
Note: RSD7-RSD0 = 00 Hex

Figure 8. System Interface Receive Format for MVIP Mode

In MVIP mode only, the frame sync pulses, RSYNC and TSYNC, may be delayed up to four clock pulses in integral numbers of clock periods (RCLK or TCLK). This allows the system side to run an overspeed clock. The effect is to always restart the data and signaling highways during transmit or receive highway channel number 0 (if an offset is programmed, the change is delayed by the value of the offset); in effect channel 0 can become 9, 10, 11 or 12 bits long. Since the framer does not process or supply data in channel 0 there is no effect on framer performance.

The System Interface provides payload loopbacks for each of the individual framers. The System Interface also accepts a single local oscillator input (LO) for use in the Framer blocks for Transmit Slip Buffer operation or AIS generation without TCLK present. T1SI is a one second clock used to operate shadow registers and freeze counter values, allowing polled service of the framers for performance and fault monitoring. The two mode select pins, CONFIG(2-1), are used to select transmission or MVIP modes and serial interface or DS1 monitor modes. Pin $\overline{CSO}$ is used to force the line interface output pins (LTCLK, TPOS/TLDAT and TNEG/TMODE) low for redundancy configurations.

PER CHANNEL (FRAMER) BLOCK OPERATION

Each Framer block consists of a Receive Line Interface, a Receive Framer, a Receive Slip Buffer and a Receive Signaling block for the line to terminal direction. In the terminal to line direction each Framer block consists of a Transmit Slip Buffer, a Transmit Signaling block, a Transmit Framer and a Transmit Line Interface. Each Framer block also has a Facility Data Link block and it provides three forms of loopback. All of these blocks, and the loopback features, framing structure and miscellaneous functions of the Framer blocks, are described in the following subsections.

Receive Line Interface Operation

The Receive Line Interface provides the AMI or B8ZS decoder. In addition, bipolar violations are detected and counted. Excessive zeros (8 or more consecutive zeros in B8ZS, or 16 or more consecutive zeros in AMI) are also detected and can optionally be added into the bipolar violation counts by setting the per channel control bit ENZC to 1. Loss of signal (LOS) is detected per ANSI T1M1.3. When LOS is detected, the local oscillator (LO) input is selected as a receive clock. For NRZ mode of operation, the decoder is bypassed and LOS cannot be detected, but bipolar violations can be counted if supplied by an external Line Transceiver via pin RLBPV. This block also can accept the output of the Transmit Line Interface block to provide local loopbacks. AIS is detected in this block per ANSI T1M1.3. In addition to providing error conditions and counts to the Microprocessor Input/Output Interface, this block can combine a signal from pin LINT to form LOS and can send AIS optionally to the System Interface via RSIGL (transmission mode only). Data from this block is sent to the Receive Framer and pertinent status information is forwarded to both the Receive Framer and the Facility Data Link block.

The receive line interface has many controls and status bits. Control bits MODE, BE, ENZC, LIE and LPOL (at address X00H) provide the enabling of the B8ZS/AMI decoder versus NRZ, control of B8ZS or AMI decoding, control of the inclusion of excessive zeros in the code violation counts, if the LINTn pin is or-gated with LOS status and LINTn's active polarity. RXNRZP and RXCP (at address X01H) determine the clock edge used to sample the line data and the polarity of NRZ data. Status, interrupt masking, latched values, PM values and FM values for Loss Of Signal (LOS) and Alarm Indication Signal (AIS) are provided (at addresses X10H, X09H, X11H, X12H and X13H). A line code error counter with overflow is provided, CV15-CV0 and BPVO (at addresses XF7H, XF8H and XF9H). Latched values are provided also, LCV15-LCV0 and LBPVO (at addresses XF4H, XF5H and XF6H) if ENPMFM is set to one. Status bit LINT is provided (at address X15H) to indicate the status of the input pin LINTn.

Receive Framer Operation

The Receive Framer performs two basic functions. One, it operates an off line synchronizer that finds the start of frame in either SF or ESF mode; just the terminal framing bit or both the terminal framing and signaling identification bits (CRC6 in ESF) can be used to validate frame start. The synchronizer meets ANSI T1.403 and AT & T PUB 62411 requirements. Two, it uses the frame position information to extract signaling bits which are sent to the Receive Signaling block, to extract the Facility Data Link information and to extract the DS0 information which is sent to the Receive Slip Buffer. The synchronizer continuously monitors the framing information and declares an Out Of Frame (OOF) on start-up and when 2 of 4, 5 or 6 (programmable) frame bits are in error with or without the signaling identification (SF mode). For performance monitoring, the Severely Error Frame (SEF) defined by ANSI T1M1.3 is also detected. When the framer regains frame alignment that causes a new start of frame position a Change of Frame Alignment alarm is generated (CFA). Frame bit errors are counted as well as CRC6 errors in ESF mode. The Receive Framer detects SF yellow alarm and SF loop-up and loop-down codes. A non-framing mode is also provided which bypasses this block as well as the Receive Slip Buffer in transmission mode.

The receive framer is controlled by the framer control register (at address X04H). The OOF1 and OOF0 control bits determine the out of frame window (4, 5 or 6 frame bits). Control bits FMD1 and FMD0 select SF, ESF or transparent modes. The SYCI and SYCO control bits determine what bits are used to frame a a 0. Control bit RSYC is used to force a re-frame operation. The ALT control bit selects the standard or Japanese versions of the yellow alarm.

From a status, mask, event, PM and FM viewpoint, five registers are provided (at addresses X10H, X09H, X11H, X12H and X13H). Out Of Frame (OOF), Yellow (YEL), Change of Frame Alignment (CFA) and Severely Errored Frame (SEF) are monitored. In addition, frame bit errors are counted with overflow in bits FBE7-FBE0 and FBOF (at addresses XFCH and XFDH). A latched value of this counter is also available in bits LFBE7-LFBE0 and LFBOF (at addresses XFAH and XFBH) if ENPMFM is set. For ESF, a CRC counter is provided in bits CRC8-CRC0 with CRCO for overflow (at addresses XF2H and XF3H). A latched value is also available in bits LCRC8-LCRC0 and LCRCO (at addresses XF0H and XF1H) if ENPMFM is set.

Receive Slip Buffer Operation

The Receive Slip Buffer controls the DS0 access and re-timing, providing a two-frame buffer that is optionally bypassable in transmission mode only. When enabled, DS0s received from the line via recovered receive clock (LRCLK) are written into the slip buffer and read out by system clock (RCLK). A phase shift between the two clocks is detected in this block, and a deletion or repetition of one frame of data (24 DS0s) is provided if the buffer reaches an almost full or almost empty condition, respectively. Alarm information is provided to the Microprocessor Input/Output Interface also. Individual DS0s can be accessed by the Microprocessor Input/Output Interface as well as written by the Microprocessor Input/Output Interface, in place of data from the Receive Framer, to allow idle or out of service codes to be sent to the system.

The receive slip buffer has several controls and status bits associated with it. The actual data bytes (DS0s) are also readable and writable through the Microprocessor Input/Output Interface. The receive slip buffer is controlled by bits RSE and RSR (at address X02H). RSE selects whether the receive slip buffer is bypassed or used. RSR, when toggled, causes the slip buffer to be re-centered, choosing a minimum delay. Status, mask, event, PM and FM information is available, together with other framer events, in bits CRXSLIP, MRXSLIP, LRXSLIP, P_RXSLIP and F_RXSLIP (at addresses X10H, X09H, X11H, X12H and X13H). In addition, the detailed status of the receive slip buffer is available with status bits RXSI and RXSO (at address X14H). The read and write pointers can also be read with bits RWP7-RWP0, RWPF4-RWPF0, RRP7-RRP0 and RWSBS (at addresses X24H, X25H and X26H). RWPF4-RWPF0 indicate the current frame of a superframe.

DS0 read/write access and control is provided. Each DS0 position appears twice in the slip buffer (current and next frame) at addresses X40H-X57H and X58H-X6FH. To disable the writing of the received data by the framer into the slip buffer (hence microprocessor write becomes the repeated value), control bits RDE1 through RDE24 are provided (at addresses XE0H, XE1H and XE2H).

The receive frame bits are also held in a FIFO, which can be read by via the Microprocessor Input/Output Interface. These bits are available at addresses X30H to X36H.

Receive clock can be either recovered receive clock (LRCLKn pin) or RCLKn if RSE is set. Control bit RXC (at address X02H) selects the clock. On LOS, local clock from pin LO is substituted for LRCLKn.

Receive Signaling Operation

The Receive Signaling block stores the 96 signaling bits extracted by the Receive Framer and the Frame bits (Fs or Facility Data Link) and outputs them on the signaling highway along with the AIS and yellow alarms via the System Interface in transmission mode; only signaling bits are sent to the output in the MVIP mode. Microprocessor Input/Output Interface control of which DS0s have signaling, and the ability to read or write the signaling bits by the Microprocessor Input/Output Interface, is provided. Signaling freeze is implemented on line failure conditions (LOS and OOF), as well as under Microprocessor Input/Output Interface control to allow writing of signaling bits.

Robbed-bit signaling type for both receive and transmit is selected by control bits TYP1 and TYP0 (at address X03H). Clear channel (no signaling) and 2- or 4-state signaling are available for SF mode. In ESF mode, clear channel and 2-, 4- or 16-state signaling are provided. Robbed-bit signaling can be enabled per DS0, allowing a mixture of clear and signaling DS0s. Control bits SE1 through SE24 (at addresses XE8H, XE9H and XEAH) provide signaling enable control for both receive and transmit.

The signaling bits received are available for reading and over-writing by the Microprocessor Input/Output Interface. The receive signaling bits (A1-A24, B1-B24, C1-C24 and D1-D24) are available at addresses X80H, X81H, X82H, X84H, X85H, X86H, X88H, X89H, X8AH, X8CH, X8DH and X8EH. For the Microprocessor Input/Output Interface to over-write the receive signaling bits or to continue to send to the system the current signaling bits repeatedly, control bit RXF (at address X03H) is provided, which freezes the signaling. This signaling freeze function is also automatically invoked under LOS and OOF conditions. This signaling freeze status is also readable with status bit RXSF (at address X15H). For SONET byte-synchronous applications, control bit OSE (at address X03H) is provided that replaces all extracted signaling bits with ones.

Transmit Slip Buffer Operation

The Transmit Slip Buffer controls the DS0 access and re-timing, providing a two-frame buffer that is optionally bypassable in transmission mode. When enabled, DS0s received from the system under system clock (TCLK) are written into the slip buffer and read out by recovered receive clock (LRCLK) or local oscillator (LO). A phase shift between the two clocks is detected in this block, and a deletion or repetition of one frame of data (24 DS0s) is provided if the buffer reaches an almost full or almost empty condition, respectively. Alarm information is provided to the Processor Interface also. Individual DS0s can be accessed by the Microprocessor Input/Output Interface as well as written by the Microprocessor Input/Output Interface, in place of data from the System Interface, permitting idle or out of service codes to be sent to the line.

The transmit slip buffer has several controls and status bits associated with it. The actual data bytes (DS0s) are also readable and writable through the Microprocessor Input/Output Interface. The transmit slip buffer is controlled by bits TSE and TSR (in address X02H). TSE selects whether the transmit slip buffer is bypassed or used. TSR, when toggled, causes the transmit slip buffer to be re-adjusted for minimum delay (approximately 16 DS0s) but with tolerance for jitter. Status, mask, event, PM and FM information is available, together with the other framer events, in bits CTXSLIP, MTXSLIP, LTXSLIP, P_TXSLIP and F_TXSLIP (at addresses X10H, X09H, X11H, X12H and X13H). In addition, the detailed status of the transmit slip buffer is available with status bits TXS1 and TXS0 (at address X14H). The read and write pointers can also be read with bits TWP7-TWP0, TRP7-TRP0, TWPF4-TWPF0 and TWSBS (at addresses X20H, X21H and X22H). TWPF4-TWPF0 indicate the current frame of a superframe being generated.

DS0 read/write access and control is provided. Each DS0 position appears twice in the transmit slip buffer (current and next frame) at addresses X90H-XA7H and XA8H-XBFH. To disable the writing of system data by the framer into the transmit slip buffer (hence microprocessor write becomes the repeated value), control bits TDE1 through TDE24 (at addresses XE4H, XE5H and XE6H) are provided. This feature allows DS0 codes (e.g., idle, out of service) to be sent in specific DS0s.

Transmit Signaling Operation

The Transmit Signaling block stores the 96 signaling bits, the Frame bits (Fs or Facility Data Link) and the AIS and yellow alarms received by the signaling highway in transmission mode and outputs them to the Transmit Framer; in MVIP mode only signaling bits are supplied. Microprocessor Input/Output Interface control of which DS0s have signaling, and the ability to read or write the signaling bits by the Microprocessor Input/Output Interface, is provided. Signaling freeze is implemented on system failure conditions (AIS on the signaling highway), as well as under Microprocessor Input/Output Interface control to allow writing of signaling bits.

Transmit robbed-bit signaling is controlled by control bits TYP1, TYP0 and SE1 through SE24, as described above for receive robbed-bit signaling.

The signaling bits received over the signaling highway are merged into the SF or ESF superframe after being buffered. This buffer is available for Microprocessor Input/Output Interface read or over-write. The signaling bits (A1-A24, B1-B24, C1-C24 and D1-D24 are available at addresses XD0H, XD1H, XD2H, XD4H, XD5H, XD6H, XD8H, XD9H, XDAH, XDCH, XDDH and XDEH. For the Microprocessor Input/Output Interface to over-write the signaling bits received from the signaling highway, or to allow the current signaling bits stored in the buffer to be transmitted to the line repeatedly, control bit TXF (at address X03H) is provided. This signaling freeze function is useful for microprocessor control of a DS1 interface to support per-DS0 signaling/dialing, trunk conditioning, etc. This signaling freeze function is also invoked automatically if AIS is received from the system interface. The signaling freeze status is also readable with status bit TXSF (at address X15H).

Transmit Framer Operation

The Transmit Framer forms an ESF or SF frame from the data received from the Transmit Slip Buffer and the signaling and alarm information (transmission mode only) received from the Transmit Signaling block. Facility Data Link information can either be incorporated from the Facility Data Link block or the Transmit Signaling block (transmission mode only); an external Fs pattern can also be incorporated if the Transmit Signaling block is chosen in SF mode (transmission mode only). CRC6 is calculated in the ESF mode and inserted. SF yellow and loop-up or loop-down codes can be inserted if selected. Yellow alarm (SF) is supplied by this block if selected by the Microprocessor Input/Output Interface or if received on the signaling highway (TSIGL) in transmission mode. A single frame bit, or CRC6 errors for test purposes, can also be supplied. The Transmit Framer and Transmit Slip Buffer can be bypassed if unframed operation is desired in transmission mode.

The transmit framer is controlled by the framer control register (at address X04H). Control bits FMD1 and FMD0 select the mode: SF, ESF or transparent. The F_s bit can be generated by the framer or bypassed (using control bit BDFL at address X01H) to support special ESF or SF modes. The transmit framer can force alarms as needed for operation or test. CRC forces a CRC error on one frame. FRME causes a bad frame bit to be sent. AIS sends all ones continuously and YEL sends ESF, SF or Japanese yellow alarm (all at address X07H). Yellow alarm can also come from the system interface as described above in the Transmission Mode subsection.

Transmit Line Interface Operation

The Transmit Line Interface provides an AMI/B8ZS encoder. In AMI mode forced ones density can be enabled to guarantee ANSI T1.403 compliance. NRZ mode bypasses the encoder. This block provides AIS generation either from Microprocessor Input/Output Interface control or from the alarm bit set on the signaling highway (TSIGL) in transmission mode. A single BPV can be generated for test purposes. A 'transmit all zeros' capability is provided to conserve power in an external Line Transceiver when AIS is not required.

The transmit line interface has many controls. Control bits MODE and BE (at address X00H) control the transmit coder as well as the receive decoder. TXCP and TXNRZP control the clock edge to send data to the line as well as the NRZ polarity (at address 01H). PWRD, FDAT and FPOL control power-down of the individual framers as well as an enable for forced data and a polarity for forced data (at address X01H). Control bit BPV (at address X07H) forces a single bipolar violation for test purposes.

Facility Data Link Operation

The Facility Data Link block provides a full duplex LAPD and bit-oriented message interface supporting the ANSI FDL protocol (T1.403) and the AT&T TABS protocol (Pub 54016). From the Microprocessor Input/Output Interface this block can be configured to send or receive either bit-oriented priority messages (one of which is ESF yellow) or message-oriented protocol (e.g. performance reports). A 16-byte FIFO is provided in each direction for each channel to permit ANSI and many TABS messages to be sent or received without additional processor intervention part way through the message. For long messages, interrupt and status support is provided to facilitate FIFO servicing. Separate global polling registers are provided for line events and FDL events so that the FDL can be run interrupt driven while the rest of the QDS1F is operated in a polled mode (see Global Register at address 00EH).

Facility Data Link Controller

The Facility Data Link Controller handles the following functions:

- Data parallel to/from serial conversion
- Zero bit stuffing/destuffing
- CRC - ITU-T generation/checking
- Flag generation/detection
- Abort generation/detection
- Start of frame detection
- End of frame detection
- Receiver overflow
- Transmitter underflow

HDLC message frames are composed of four sections: the opening flag, the body of the frame, the frame check sequence, and the closing flag. The opening and closing flags are represented by a single, unique 8-bit character (01111110). To avoid the occurrence of false flag characters in the data stream, a zero is inserted (stuffed) after each string of five contiguous ones. Reception of more than five contiguous ones is interpreted as a frame abort sequence. When an abort sequence is received, the remainder of the current frame is ignored and the received portion is discarded as an invalid frame.

A 16-bit frame check sequence is computed across the contents of the frame and appended to the end of the frame. Time between frames is filled with one or more flag characters. When two or more flag characters occur in sequence, they may share the zero between them, resulting in the following 15-bit sequence: 0111111<u>0</u>1111110. Note that the underlined zero is shared between the two flag characters.

The HDLC receiver is enabled with the EHR bit in the FDL Control Register (address X08H). When enabled, it will receive a serial data stream and remove the stuffed zero bits. It will then search for flag characters to find byte alignment. Flag characters are discarded. Non-flag characters following a valid flag character are received and placed into the receive FIFO (address X17H). A CRC is computed across the received characters until the trailing flag is detected. The last two bytes received are the transmitted CRC, and they are compared against the calculated CRC. The FDL Status and Event Registers (addresses X16H and X0EH) will be set if a CRC error is detected. The CRC bytes are not stored in the FIFO. The receiver has a maskable interrupt (address X0FH) that may be generated by a FIFO service request, a FIFO overflow, or a receive abort. These events are indicated by the RHIS2 - RHIS0 status bits in the FDL Status and Event Registers. These bits are or-gated together with TX status bits to generate an interrupt and set a bit for the channel in the FDL polling register. The Event Register must be cleared to enable receipt of another message.

The HDLC transmitter is enabled with the EHT bit in the FDL Control Register (address X08H). When enabled, it will transmit flag characters until data is placed in the transmit FIFO (address X0AH). Up to 16 bytes may be placed in the FIFO. The transmit bytes will be read from the FIFO and a CRC will be computed until the end of

message is received. The transmit bytes will be stuffed with zeros after they have been used for the CRC calculation. When the last byte of the transmit message is written into the FIFO, the end of message (EOM) bit (address X08H) should be set. When the transmitter empties the FIFO, if the EOM bit is not set, the underrun status will be set in the FDL Status and Event Registers (addresses X16H and X0EH) and an abort character will be transmitted. If the EOM bit is set, the computed CRC will be appended to the end of the message, followed by at least one flag character. When the transmitter completes a either normal or abnormal message, an interrupt will be generated.

The transmitter has a maskable interrupt (address X0FH) that may be generated by a FIFO service request or a FIFO underflow. These events are indicated by the THIS status bit and the TXFS1 - TXFS0 bits in the FDL Status and Event Registers (addresses X16H and X0EH). These bits are or-gated together with the RX status to generate an interrupt and set a bit for the channel in the FDL polling register.

HDLC FIFO service interrupts may be programmed to occur at various thresholds by the FDL Control Register (address X08H). In the transmit direction, interrupts may be set when the transmit FIFO is half empty or when the last character has been sent using the THIE bit in the FDL Control Register. For short messages, the entire contents may be placed in the FIFO and the controller will interrupt when the message has been sent. For long messages (longer than the maximum FIFO depth) the controller will interrupt when the FIFO is ready to accept more data (half empty). In the receive direction, interrupts may be set at the end of a received message or on FIFO half full, using the RHIE bit in the FDL Control Register. When messages are always expected to be shorter than the maximum FIFO depth, the controller will interrupt on the completion of the HDLC frame. When messages are expected to exceed the maximum FIFO depth, the controller will interrupt when the FIFO is half full. The Receive HDLC FIFO Depth Register (address X18H) will indicate the number of bytes to be read when the interrupt is received.

HDLC Application

There are four general types of message transfers possible; transmitting long and short messages and receiving long and short messages. The difference between the long and short messages is primarily in how the FIFO buffer is serviced. With short messages, the entire message will fit into the FIFO, and interrupts are generated when the end of the message is received. With long messages, the message will not fit into the FIFO and will have to be transmitted or received in several segments. Since a long and short message are similar, the receive short message type is described with the long message.

To transmit data five registers are used; the FDL Control Register (address X08H), the FDL Status Register (address X16H), the FDL Mask Register (address X0FH), the FDL Event Register (address X0EH) and the Transmit HDLC Data Register (address X0AH). To receive data six registers are used; the FDL Control Register, the FDL Status Register, the FDL Mask Register, the FDL Event Register, the Receive HDLC Data Register (address X17H), and the Receive FIFO Depth Register (address X18H). A separate Polling Register is used to distinguish FDL from loop events (address 00EH).

Transmit Short Message:

To transmit short messages, the transmitter is first configured to interrupt at the end of a message by clearing the THIE bit in the FDL Control Register. The transmitter is then enabled by setting the EHT bit in the FDL Control Register. The transmitter will begin sending flag characters until data is written to the Transmit HDLC Data Register.

The next step is to write the message into the transmit FIFO and then set the EOM bit in the FDL Control Register. The transmitter will begin sending characters until the FIFO is empty. When the last character is taken from the FIFO, the EOM bit is sampled and cleared. Since the EOM bit will always be set (the whole message is in the FIFO) the THIS bit in the FDL Status and Event Registers is set, and an interrupt is generated if not masked by the FDL Mask Register. This indicates that the FIFO is available for another message. Software should clear the FDL Event Register to clear the interrupt and send the next message. To prevent missing a receive interrupt, the FDL Status Register should be checked for a message in progress at this time.

Transmit Long Message:

To transmit long messages, the transmitter is first configured to interrupt when the FIFO is half full by setting the THIE bit in the FDL Control Register. The transmitter is then enabled by setting the EHT bit in the FDL Control Register. The transmitter will begin sending flag characters until data is written to the Transmit HDLC Data Register.

The next step is to begin writing the message into the transmit FIFO until 16 bytes have been loaded in. The transmitter will begin sending characters. When half of the FIFO has been sent, the THIS bit in the FDL Status and Event Registers is set, and an interrupt is generated (the FDL Mask Register must be properly programmed). The FIFO is then half empty and is available for more characters. The software will write the next set of 8 bytes to the FIFO. If the end of message is reached, software should also set the EOM bit. When the last character is taken from the FIFO, the EOM bit is sampled and cleared. If the EOM bit was not set, the TXFS1 - TXFS0 bits in the FDL Status Register are set, indicating an underrun, and an interrupt is generated. If the EOM bit is set, the THIS bit in the FDL Status and Event Registers is set, and an interrupt is generated. This indicates that the FIFO is available for another message. Software should clear the FDL Event Register to clear the interrupt and send the next message. The same precaution above applies to a receive message in progress.

Receive Message:

To receive messages, the receiver is first configured to interrupt when the FIFO is half full by setting the RHIE bit in the FDL Control Register. For ANSI/Bellcore maintenance data link protocol, RHIE may be cleared to reduce the number of interrupts, since all messages will fit in the FIFO. The receiver is then enabled by setting the EHR bit in the FDL Control Register.

The receiver will now generate an interrupt (if not masked) when it has received enough characters to fill the FIFO half full, or when it has received the end of a message. When the receive interrupt is asserted, the RHIS2 - RHIS0 bits are set in the FDL Status and Event Registers. Software should read the Receive FIFO Depth Register to determine the number of bytes to be read, and then read those bytes from the Receive HDLC Data Register. If an end of message is detected, the RHIS bits in the FDL Event Register will also be set to indicate the end of the message. Note that the FIFO depth count is updated when an interrupt is generated and will not be modified until read by software. The HDLC receiver cannot accept a new message until after the FDL Event register is cleared, so reading the designated number of bytes gets the entire message. During the reception of a long message the count is allowed to change after the half-full interrupt to permit software to extract the most data possible. If software fails to read out the FIFO in time, a second interrupt will be generated after clearing the FDL Event Register; this condition can be determined by again reading the FDL Status and Event Registers. This procedure is also useful in detecting a completion of a transmit message which could occur after reading the FDL Event Register for the receive interrupt but before clearing it, which must occur after reading out the FDL receive FIFO.

Bit-Oriented Code Controller

Bit-oriented codes are transmitted and received on the FDL as 16-bit sequences. The sequence consists of 8 ones, followed by 1 zero, followed by 6 code bits, followed by 1 zero (111111110xxxxxx0). There are 63 possible codes that may be transmitted or received. The 64th code of all ones is the same as the HDLC flag, and is not used.

To transmit a bit-oriented code, the 6-bit code value is written into the code register (address X0BH) and the transmit enable bit, EBT in the FDL Control Register (address X08H), is set. The concatenated 16-bit code word is sent continuously.

The bit-oriented code receiver is enabled with the EBRI bit in the FDL Control Register. It will detect the 63 possible codes and store the significant 6-bit value in the receive register (address X19H) if the same code has been received 8 out of 10 times. When a valid bit code has been detected, the RHIS bits in the FDL Status Register will be set and an interrupt will be generated. It should be noted that ESF yellow alarm overrides this function and only the line event, status events and interrupts will be generated.

Loopbacks

Figure 9 below shows the three loopbacks available in the QDS1F device and indicates where the DS1 monitor is connected.

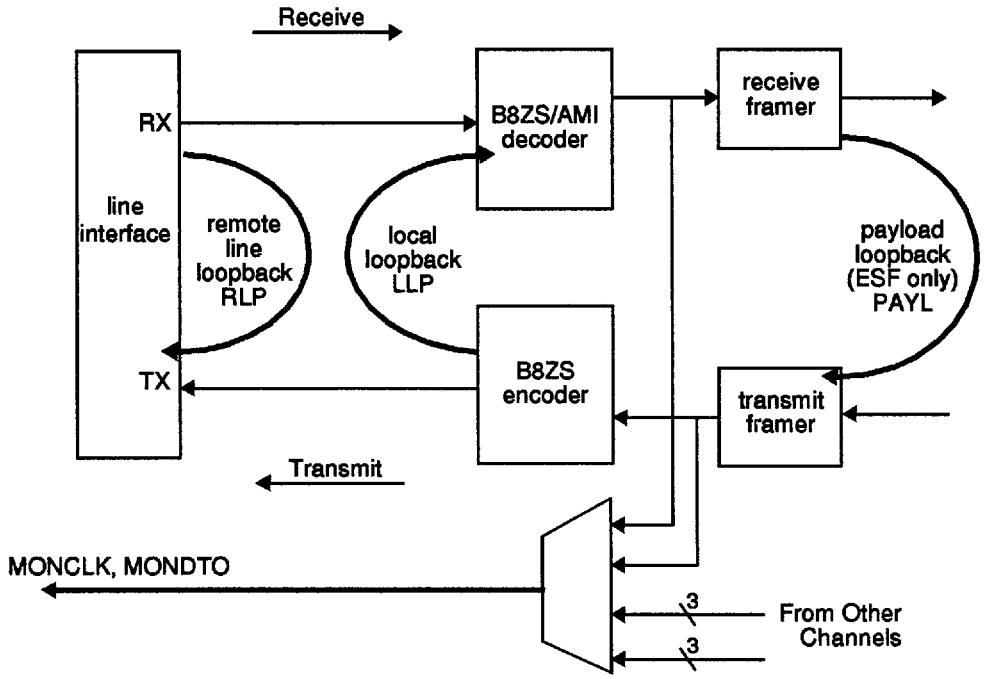


Figure 9. Loopbacks per Channel in QDS1F Device

Loopbacks for SF are automatically handled by the QDS1F. Loopbacks for ESF are handled using the Microprocessor Input/Output Interface. Loopbacks are detected by the QDS1F (see Facility Data Link section) and the microprocessor sets and clears the loopbacks. Several loopback controls are provided. Control bits RLP, PAYL and LLP (at address X05H) control the remote, payload and local loopbacks respectively, as shown in Figure 9.

SF loop-up and loop-down operation is supported also. To send the codes, control bits TXUP and TXDN (at address X05H) are used. To set a framer up to receive the loop-up and loop-down codes control bit ALUP is provided (at address X05H). A 16-bit counter is provided that can be used by the Microprocessor Input/Output Interface to indicate matches to the loop-up and loop-down codes in bits LBCC15-LBCC0 (at addresses X39H and X38H). The codes are programmable on a per-device basis. The transmit (and receive) loop-up pattern is set by control bits TLU6-TLU0 (at address 014H). The transmit (and receive) loop-down pattern is set by control bits TLD6-TLD0 (at address 015H). The pattern length (4 to 7 bits) is set by ULEN1 and ULEN0, and DLEN1 and DLEN0, control bits (at address 016H). When ALUP is set, the loop-up and loop-down codes are automatically detected over a 5-second period and invoked. loop-up and loop-down status are presented in a status register as UP and DOWN (at address X15H).

Framing Structures

The two tables in Figures 10 and 11 below show the D4 SF and ESF framing structure. In ESF mode 2, 4 or 16 state signaling is supported. When no signaling is supported in a DS0, the signaling frames support 8-bit data. 'Fe' is the framing bit, 'D1' is the facility data link bit and 'CRC' is the CRC6 bit. For framing, the CRC6 check may optionally be included to determine frame alignment. This is recommended since automatic clearing of mimic patterns is provided. In D4 SF mode 2- or 4-state signaling is supported. When no signaling is supported in a DS0 the signaling frames support 8-bit data. 'Ft' is the terminal framing bit and 'Fs' is the multi-frame alignment bit. 'YA' is the yellow alarm bit; it is bit 2 = 0 of every DS0, or Fs =1 for frame 12 for Japanese standards.

Frame #	1st Bit in frame	F-Bit		Bit Use for each time-slot			Signaling Options		
		Fs	Ft	Data	YA	Signaling	None	2-state	4-state
1	0	-	1	Bits 1-8	Bit 2	None	-	-	-
2	193	0	-	Bits 1-8	Bit 2	None	-	-	-
3	386	-	0	Bits 1-8	Bit 2	None	-	-	-
4	579	0	-	Bits 1-8	Bit 2	None	-	-	-
5	772	-	1	Bits 1-8	Bit 2	None	-	-	-
6	965	1	-	Bits 1-7	Bit 2	Bit 8	-	A	A
7	1158	-	0	Bits 1-8	Bit 2	None	-	-	-
8	1351	1	-	Bits 1-8	Bit 2	None	-	-	-
9	1544	-	1	Bits 1-8	Bit 2	None	-	-	-
10	1737	1	-	Bits 1-8	Bit 2	None	-	-	-
11	1930	-	0	Bits 1-8	Bit 2	None	-	-	-
12	2123	0 or YA	-	Bits 1-7	Bit 2	Bit 8	-	A	B

Figure 10. D4 SF Framing Structure

Frame #	1st Bit in frame	F-Bit			Bit Use for each time-slot		Robbed bit Signaling Options			
		Fe	DI	CRC	Data	Signaling	None	2-state	4-state	16-state
1	0	-	D	-	Bits 1-8	None	-	-		
2	193	-		1	Bits 1-8	None	-	-		
3	386	-	D	-	Bits 1-8	None	-	-		
4	579	0		-	Bits 1-8	None	-	-		
5	772	-	D	-	Bits 1-8	None	-	-		
6	965	-		2	Bits 1-7	Bit 8		A	A	A
7	1158	-	D	-	Bits 1-8	None	-	-		
8	1351	0		-	Bits 1-8	None	-	-	-	
9	1544	-	D	-	Bits 1-8	None	-	-	-	
10	1737	-		3	Bits 1-8	None	-	-	-	
11	1930	-	D	-	Bits 1-8	None	-	-	-	
12	2123	1		-	Bits 1-7	Bit 8	-	A	B	B
13	2316	-	D	-	Bits 1-8	None	-	-	-	
14	2509	-		4	Bits 1-8	None	-	-	-	
15	2702	-	D	-	Bits 1-8	None	-	-	-	
16	2895	0		-	Bits 1-8	None	-	-		
17	3088	-	D	-	Bits 1-8	None	-	-	-	
18	3281	-		5	Bits 1-7	Bit 8	-	A	A	C
19	3474	-	D	-	Bits 1-8	None	-	-	-	
20	3667	1		-	Bits 1-8	None	-	-	-	
21	3860	-	D	-	Bits 1-8	None	-	-	-	
22	4053	-		6	Bits 1-8	None	-	-	-	
23	4246	-	D	-	Bits 1-8	None	-	-	-	
24	4439	1		-	Bits 1-7	Bit 8	-	A	B	D

Figure 11. ESF Framing Structure

Miscellaneous Functions

Each framer can be reset by control bit SRST (at address X05H). As long as this bit is set, the selected framer is held in a reset state. This control bit resets all performance counters and latched/shadow registers as well as all internal state machines. It does not affect configuration registers.

To assist in debugging software, control bit SFZ is provided (at address X06H). When it is set, SFZ holds the internal registers, RAMs, etc. in their current state by shutting off the four framer clocks. All counters, pointers, etc. can be read by the Microprocessor Input/Output Interface without influence by external data and clocks.

Receive and Transmit fast synchronization functions are provided via control bits TXFS and RXFS (at address X06H). TXFS re-uses pin TNEGn in NRZ mode to generate a synchronization pulse every 3 milliseconds. If RXFS is set, a pulse received on RNEGn in NRZ mode will force the receive framer to start a new superframe.

The AIS and YELLOW status bits received over the signaling highway can be read by the Microprocessor Input/Output Interface as bits VTAIS and VTRDI (at address X14H).

For local loopback operation, an AIS signal can be sent while LLP is set, allowing test data to be looped back to the system while a blue alarm is sent to the far end. Control bit TX1S (at address X05H) performs this function. It should be noted that, if both LLP and RLP bits are set, TX1S is disregarded.

A register at address X04H allows general purpose read and write; it may be used for device testing.

TEST ACCESS PORT

The Test Access Port interface includes a five-pin test access port (TAP) that conforms to the IEEE 1149.1 standard. This standard provides external boundary scan functions to read and write the external I/O pins from the TAP for board and component test. In addition to the TAP, a pin ($\overline{IOTRI}$) is provided to place the output buffers in a high impedance state for applications that do not support the IEEE 1149.1 standard. TCK is the test clock input signal. TMS is the test mode select signal. TDI is the test data input signal. TDO is the test data output signal. $\overline{TRS}$ is the test reset signal. Pin SCAN_ENB is used for manufacturing tests and must be tied low for normal operation.

Boundary Scan

Introduction

The IEEE 1149.1 standard defines the requirements of a boundary scan architecture that has been specified by the IEEE Joint Test Action Group (JTAG). Boundary scan is a specialized scan architecture that provides observability and controllability for the interface pins of the device. As shown in Figure 12, one cell of a boundary scan register is assigned to each input or output pin to be observed or tested (bidirectional pins may have two cells). The boundary scan capability is based on a Test Access Port (TAP) controller, instruction and bypass registers, and a boundary scan register bordering the input and output pins. The boundary scan test bus interface consists of four input signals (Test Clock (TCK), Test Mode Select (TMS), Test Data Input (TDI) and Test Reset ($\overline{TRS}$)) and a Test Data Output (TDO) output signal. Boundary scan signal timing is shown in Figure 27.

The TAP controller receives external control information via a Test Clock (TCK) signal and a Test Mode Select (TMS) signal, and sends control signals to the internal scan paths. Detailed information on the operation of this state machine can be found in the IEEE 1149.1 standard. The serial scan path architecture consists of an instruction register, a boundary scan register and a bypass register. These three serial registers are connected in parallel between the Test Data Input (TDI) and Test Data Output (TDO) signals, as shown in Figure 12.

The boundary scan function can be reset and disabled by holding pin $\overline{TRS}$ low. When boundary scan testing is not being performed the boundary scan register is transparent, allowing the input and output signals to pass to and from the QDS1F device's internal logic. During boundary scan testing, the boundary scan register may disable the normal flow of input and output signals to allow the device to be controlled and observed via scan operations. For applications that use an on-board microprocessor to operate the Boundary Scan function it should be noted that pin RDY/$\overline{DTACK}$ must be ignored during Boundary Scan tests.

Boundary Scan Operation

The maximum frequency the QDS1F device will support for boundary scan is 10 MHz. The timing diagrams for the boundary scan interface leads are shown in Figure 27.

The instruction register contains three bits. The QDS1F device performs the following three boundary scan test instructions:

The EXTEST test instruction (000) provides the ability to test the connectivity of the QDS1F device to external circuitry.

The SAMPLE test instruction (010) provides the ability to examine the boundary scan register contents without interfering with device operation.

The BYPASS test instruction (111) provides the ability to bypass the QDS1F boundary scan and instruction registers.

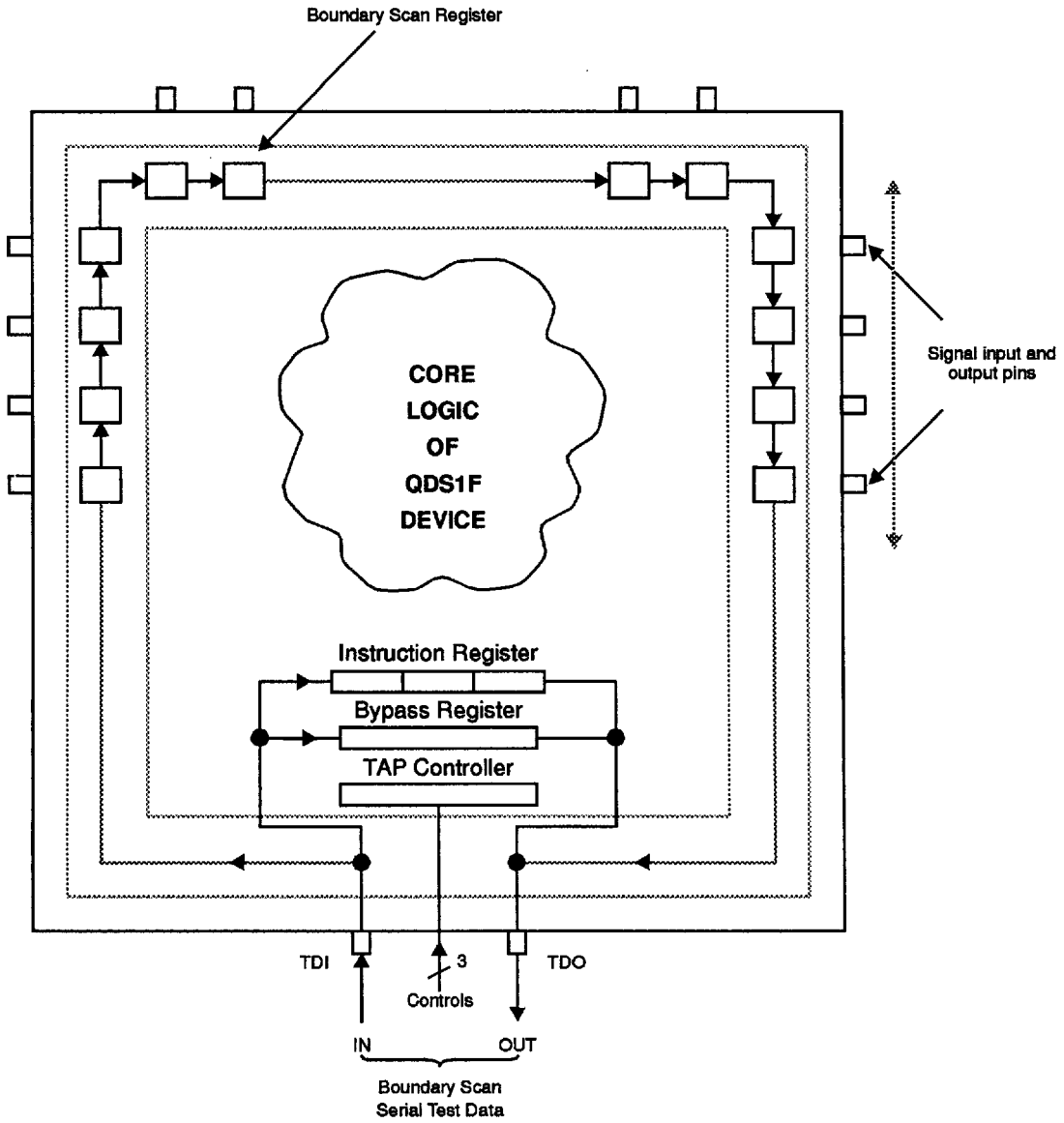


Figure 12. Boundary Scan Schematic

Boundary Scan Chain

There are (TBD) scan cells in the QDS1F boundary scan chain. Bidirectional signals require two scan cells. Additional scan cells are used for direction control as needed. The following table shows the listed order of the scan cells and their function. (Note: The detailed contents of this table are yet To Be Determined, TBD.)

PIN DIAGRAM

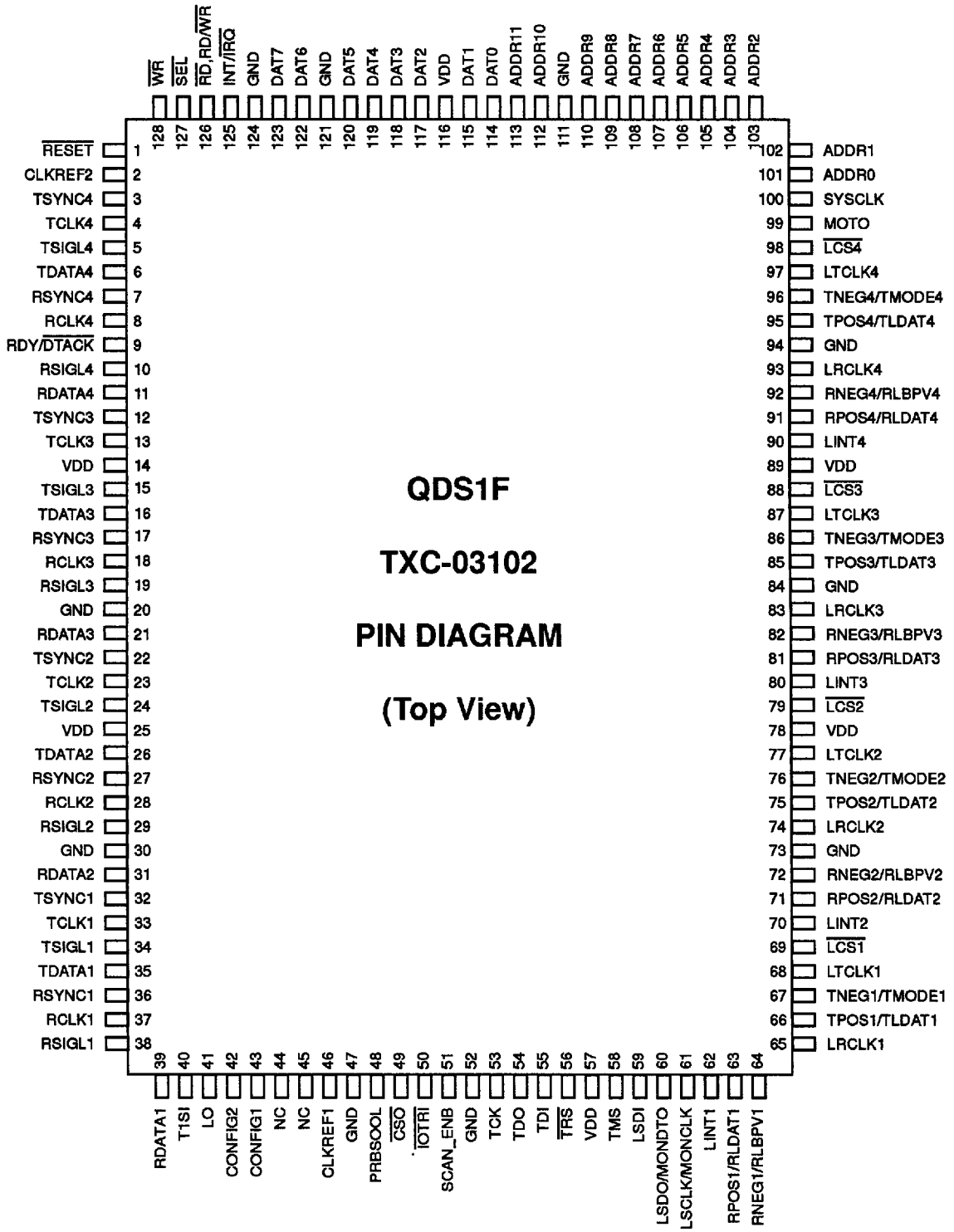


Figure 13. QDS1F TXC-03102 Pin Diagram

PIN DESCRIPTIONS

Power Supply and Ground

Symbol	Pin No.	I/O/P*	Type	Name/Function
VDD	14, 25, 57, 78, 89, 116	P		**Power Supply:** +5 volt supply voltage, +/-5%.
GND	20, 30, 47, 52, 73, 84, 94, 111, 121, 124	P		**Ground:** 0 volts reference.
NC	44, 45			**No Connect:** NC pins are not to be connected, not even to another NC pin, but must be left floating. Connection of these pins may impair performance or cause damage to the device.

* Note: I = Input; O = Output; P = Power; T=Tri-state.

Line Interface Port Signals

Symbol	Pin No.	I/O/P	Type *	Name/Function
RPOS(4-1)/ RLDAT(4-1)	91 81 71 63	I	CMOS	**Receive Positive Recovered Data Input:** When dual unipolar mode is selected, RPOS carries the received positive rail data. RPOS is a one whenever a positive pulse is received by the line interface transceiver. This signal is sampled on the active edge of LRCLK, defined by control bit RXCP. **Receive Recovered Data Input:** When NRZ mode is selected, RLDAT carries the received NRZ data. RLDAT is a one when a positive or negative pulse is received on the line interface transceiver. This signal is sampled on the active edge of LRCLK, defined by control bit RXCP.
RNEG(4-1)/ RLBPV(4-1)	92 82 72 64	I	CMOS	**Receive Negative Recovered Data Input:** When dual unipolar mode is selected, RNEG carries the received negative rail data. RNEG is a one whenever a negative pulse is received by the line interface transceiver. This signal is sampled on the active edge of LRCLK, defined by control bit RXCP. **Receive Bipolar Violation Indication:** When NRZ mode is selected and not Fast Sync, RLBPV carries the bipolar violation indication from the line interface transceiver. RLBPV is driven high by the line interface transceiver when a bipolar violation is received. This input is used to increment the internal BPV counter. This signal is sampled on the active edge of LRCLK, defined by bit RXCP. When in Fast Sync Mode and NRZ, RNEG will force sync if a one is received for bit period 193 of the last frame of a superframe. See bit RXFS (Address X06H).

* Note: See Input, Output and I/O Parameters section for Type definitions.

Symbol	Pin No.	I/O/P	Type	Name/Function
LRCLK(4-1)	93, 83 74, 65	I	CMOS	**Receive Line Clock:** Receive data is sampled on the active edge of the 1.544 MHz clock LRCLK, defined by control bit RXCP.
TPOS(4-1)/ TLDAT(4-1)	95 85 75 66	O	CMOS 2mA	**Transmit Positive Data Output:** When dual unipolar mode is selected, TPOS carries the transmit positive rail data. TPOS is a one whenever a positive pulse is to be transmitted by the line interface transceiver. This signal is updated on the active edge of LTCLK, defined by control bit TXCP. **Transmit Data Output:** When NRZ mode is selected, TLDAT carries the transmit NRZ data. When TLDAT is a one, the line interface transceiver will transmit a positive or negative pulse. This signal is updated on the active edge of LTCLK, defined by control bit TXCP.
TNEG(4-1)/ TMODE (4-1)	96 86 76 67	O	CMOS 2mA	**Transmit Negative Data Output:** When dual unipolar mode is selected, TNEG carries the transmit negative rail data. When TNEG is a one, the line interface transceiver will transmit a negative pulse. This signal is updated on the active edge of LTCLK, defined by control bit TXCP. **Transmit Mode General Purpose Output:** When NRZ mode is selected and not Fast Sync, TMODE becomes a general purpose output. This bit may be modified at any time by software but the output will be synchronized with LTCLK. It may be used to enable/disable the B8ZS encoder in the line interface transceiver. This signal is updated on the active edge of LTCLK, defined by bit TXCP. When in Fast Sync Mode and NRZ, TNEG is a one for bit period 193 of frame 24 (ESF) or every other frame 12 (SF). See bit TXFS (Address X06H).
LTCLK(4-1)	97, 87 77, 68	O	CMOS 2mA	**Transmit Line Clock:** Transmit data is updated on the active edge of the 1.544 MHz clock LTCLK, defined by TXCP.
LINT(4-1)	90 80 70 62	I	CMOS	**General Purpose Interrupt Input Port:** This input may be used to receive an interrupt from an external source. The active edge is programmable and the interrupt is maskable. When asserted, an interrupt to the controlling processor will be generated. This input may be used to generate an interrupt when the external transceiver detects an LOS or LOC. (See control bits LIE, LPOL.)
$\overline{\text{LCS(4-1)}}$	98 88 79 69	O	CMOS 2mA	**Line Interface Serial Port Chip Select:** This active low signal enables the serial port on the external line interface transceiver. When asserted, data can be written to, or read from, the line interface.

Symbol	Pin No.	I/O/P	Type	Name/Function
LSCLK/ MONCLK	61	O(T)	CMOS 2mA	**Line Interface Serial Port Clock:** This signal is used to shift data to and from the line interface serial port. Data out, LSDO, is updated on the falling edge of LSCK. Data in, LSDI, is sampled on the falling edge of LSCK. CONFIG2 = 0 for this mode. LSCLK is derived from the signal at pin LO. **Monitor Clock:** For DS1 Monitor mode (CONFIG2 = 1) this signal is the selected DS1 clock and is used to shift MONDTO data out on its rising edge.
LSDO/ MONDTO	60	O(T)	CMOS 2mA	**Line Interface Serial Port Data Out:** This is the serial data output to the line interface transceiver. This output is shared among the four transceivers. This output is updated on the falling edge of LSCLK. CONFIG2 = 0 for this mode. Typically, the first bit is Read/$\overline{\text{Write}}$ followed by seven address bits. The second byte is data. **Monitor Data:** For DS1 Monitor mode (CONFIG2 = 1) this signal is the selected DS1 NRZ data. This data is updated on the rising edge of MONCLK.
LSDI	59	I	CMOS	**Line Interface Serial Port Data In:** This is the serial data input from the line interface transceiver. This input is shared among the four transceivers. This input is sampled on the rising edge of LSCLK. One byte is shifted in from the selected device.
CLKREF1	46	O(T)	CMOS 2mA	**Clock Reference 1:** This output can be tri-stated or set to one of LRCLKn as selected via the microprocessor port. The output is either 1544KHz or 8KHz as selected by the microprocessor port. The pulse high time follows LRCLKn at 1544 kHz and is 648 nsec at 8 kHz.
CLKREF2	2	O(T)	CMOS 2mA	**Clock Reference 2:** This output can be tri-stated or set to one of LRCLKn as selected via the microprocessor port. The output is either 1544KHz or 8KHz as selected by the microprocessor port. The pulse high time follows LRCLKn at 1544 kHz and is 648 nsec at 8 kHz.

Test Access Port Signals

Symbol	Pin No.	I/O/P	Type	Name/Function
TCK	53	I	CMOS	**IEEE 1149.1 Test Port Serial Scan Clock:** This signal is used to shift data into TDI on the rising edge, and out of TDO on the falling edge.
TMS	58	I	CMOSp	**IEEE 1149.1 Test Port Mode Select:** TMS is sampled on the rising edge of TCLK, and is used to place the test access port controller into various states as defined in IEEE 1149.1. This pin must be set high for normal framer operation.

Symbol	Pin No.	I/O/P	Type	Name/Function
TDI	55	I	CMOSp	**IEEE 1149.1 Test Port Serial Scan Data In:** Serial test instructions and data are clocked into this pin on the rising edge of TCK. This input has an internal pull-up to VDD.
TDO	54	O	TTL 4mA	**IEEE 1149.1 Test Port Serial Scan Data Out:** Serial test instructions and data are clocked out of this pin on the falling edge of TCLK. When inactive, this 3-state output will be put into its high impedance state.
$\overline{TRS}$	56	I	CMOSp	**IEEE 1149.1 Test Port Reset Pin:** This pin will asynchronously reset the test access port (TAP) controller. This input has an internal pull-up to VDD. This pin must be set high for normal framer operation.
$\overline{IOTRI}$	50	I	TTL	**I/O 3-State:** This asynchronous input pin, when driven low, will place all of the output pins in a high impedance state. This will not affect the internal state of the framer.
SCAN_ENB	51	I	CMOS	**Scan Enable:** This pin is for manufacturing tests and must be tied low for device operation.

Microprocessor Bus Interface

Symbol	Pin No.	I/O/P	Type	Name/Function
DAT(7-0)	123, 122 120-117 115, 114	I/O	TTL8mA	**Data:** Bidirectional, 3-state data bus.
ADDR(11-0)	113, 112 110-101	I	TTL	**Address:** Address bus to access internal registers.
MOTO	99	I	TTL	**Motorola/Intel Processor Select:** This pin defines the operating mode of the microprocessor port. When set low, MODE 0 (Intel style) is selected. If it is high, MODE 1 (Motorola style) is selected.
$\overline{SEL}$	127	I	TTLp	**Select:** This signal enables the microprocessor interface and allows the transfer of information between the framer and the microprocessor.
$\overline{WR}$	128	I	TTL	**Write:** In MODE 0, this active low signal, in conjunction with $\overline{SEL}$, controls microprocessor write cycles. In MODE 1, this pin has no function and should be pulled to a logic one.
$\overline{RD}$,RD/$\overline{WR}$	126	I	TTL	**Read:** In MODE 0, this active low signal, in conjunction with $\overline{SEL}$, controls microprocessor read cycles. **Read/Write:** In MODE 1, this signal, in conjunction with $\overline{SEL}$, controls microprocessor read and write cycles.
RDY/$\overline{DTACK}$	9	O(T)	TTL8mA	**Ready:** In MODE 0, this signal acknowledges that the data transfer will be completed. **Data Transfer Acknowledge:** In MODE 1, this signal indicates the completion of the bus cycle.

Symbol	Pin No.	I/O/P	Type	Name/Function
INT/$\overline{IRQ}$	125	O	TTL4mA	**Interrupt:** In MODE 0, this active high signal indicates an interrupt is pending. This interrupt can be disabled.
$\overline{RESET}$	1	I	TTLp	**Reset:** This active low signal will reset the four framers. $\overline{RESET}$ must be asserted for a minimum of 10 cycles of SYSCLK after power is applied to the QDS1F. $\overline{RESET}$ will cause all writable registers in the memory map to be set to 00H. Both performance/event registers and mode control registers are affected.
SYSCLK	100	I	TTL	**System Clock:** This clock is used by the device to run internal state machines. Nominal frequency 16 MHz (16.0 MHz min. to 20.0 MHz max.), duty cycle 50 ± 10%.

System Interface

Symbol	Pin No.	I/O/P	Type	Name/Function
TSYNC(4-1)	3 12 22 32	I	CMOS	**Transmit Sync:** This signal is used to synchronize both the frame sync and multiframe sync counters and is sourced by the system; sample on rising edge of TCLK.
TCLK(4-1)	4 13 23 33	I	CMOS	**Transmit Clock:** This 1.544 / 2.048 MHz clock is the primary transmit clock, and is sourced by the system.
TDATA(4-1)	6 16 26 35	I	CMOS	**NRZ Transmit Data Input:** TDATA is the transmit data from the system interface, and is sampled on the rising edge of TCLK (Transmission mode); sampled on the falling edge of TCLK (MVIP mode).
TSIGL(4-1)	5 15 24 34	I	CMOS	**Transmit Signaling Highway:** This input carries the signaling and alarm information from the mapper to the framer. TSIGL is sampled on the rising edge of TCLK (Transmission mode); sampled on the falling edge of TCLK (MVIP mode).
RSYNC(4-1)	7 17 27 36	I/O	CMOS 2mA	**Receive Sync:** This signal is used to synchronize both the frame sync and multiframe sync counters and is sourced or input by the framer. This signal is valid on the falling edge of RCLK. In MVIP mode it is input on the rising edge of RCLK
RCLK(4-1)	8 18 28 37	I/O	CMOS 2mA	**Receive Clock:** This 1.544 MHz clock is the primary receive clock, and is sourced or input by the framer in transmission mode. In MVIP mode it is a 2.048 MHz input.
RDATA(4-1)	11 21 31 39	O	CMOS 2mA	**NRZ Receive Data Output:** RDATA is the receive data to the system interface, and is updated on the falling edge of RCLK (Transmission mode); updated on the rising edge of RCLK (MVIP mode).

Symbol	Pin No.	I/O/P	Type	Name/Function
RSIGL(4-1)	10 19 29 38	O	CMOS 2mA	**Receive Signaling Highway:** This output carries the signaling and alarm information from the framer to the mapper. RSIGL is updated on the falling edge of RCLK (Trans. mode); updated on the rising edge of RCLK (MVIP mode).
LO	41	I	CMOS	**Local Oscillator Input:** This 1.544 MHz input is an alternate clock source for the transmit line clock, LTCLK. When selected, the falling edge of LO is used to clock data from the transmit slip buffer to the line interface. LO is required to operate LSCLK.
T1SI	40	I	CMOS	**One-Second Interrupt (Shadow Register Latch):** This input operates the latched counters and shadow registers; min. high time 0.25 msec.; min. low time 3.0 msec.; max. low time 1.5 sec. When using the SF loop code detection feature, this input should be 1.0 Hz. See control bits ALUP, UP and DOWN.
CONFIG(2-1)	42 43	I	CMOS	**Configuration:** These pins are used for device mode selection. CONFIG1 tied to ground provides Transmission mode 1.544 MHz system side operation; CONFIG1 tied high (VDD) provides MVIP mode 2.048 MHz system side operation. CONFIG2 tied to ground selects the Serial Port. CONFIG2 tied high (VDD) selects the DS1 Monitor mode.
$\overline{CSO}$	49	I	CMOS	**Card Switch Off:** This active low input when driven causes LTCLK(4-1), TPOS(4-1) and TNEG(4-1) to be driven to a logic low for protection switching purposes.
PRBSOOL	48	O	CMOS 2mA	**PRBS Out of Lock:** This output indicates when the PRBS analyzer is in lock. If high the PRBS analyzer is out of lock. If the PRBS analyzer is not selected this output remains low at all times. PRBS operates in transmission mode only.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min*	Max*	Unit
Supply voltage	V_{DD}	-0.3	+7.0	V
DC input voltage	V_{IN}	-0.5	V_{DD} + 0.5	V
Ambient operating temperature	T_A	-40	85	°C
Operating junction temperature	T_J		150	°C
Storage temperature range	T_S	-55	150	°C

*Note: Operating conditions exceeding those listed in Absolute Maximum Ratings may cause permanent failure. Exposure to absolute maximum ratings for extended periods may impair device reliability.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal Resistance: junction to ambient			43	°C/W	
Thermal Resistance: junction to case		TBD		°C/W	
Normal operating junction temperature		TBD		°C	

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	4.75	5.0	5.25	V	
I_{DD}		97[1]	115[2]	mA	1. All channels operating. 2. All channels operating, SYSCLK at maximum frequency
P_{DD}		485[1]	600[2]	mW	

INPUT, OUTPUT AND I/O PARAMETERS

Input Parameters For TTL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	V_{DD} =5.25
Input capacitance		5.0		pF	

Input Parameters For TTLp

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current		0.10	0.24	mA	V_{DD} =5.25; Input = 0 volts
Input capacitance		5.5		pF	

Note: Input has a 47 kilohm (nominal) internal pull-up resistor.

Input Parameters For CMOS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	3.15			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			1.65	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	V_{DD} =5.25
Input capacitance		5.0		pF	

Input Parameters For CMOSp

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	3.15			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			1.65	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current		0.10	0.24	mA	V_{DD} =5.25; Input = 0 volts
Input capacitance		5.5		pF	

Note: Input has a 47 kilohm (nominal) internal pull-up resistor.

Output Parameters For TTL4mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 4.75; I_{OH} = -2.0
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 4.0
I_{OL}			4.0	mA	
I_{OH}			-2.0	mA	
t_{RISE}		8		ns	C_{LOAD} = 15 pF
t_{FALL}		5		ns	C_{LOAD} = 15 pF

Output Parameters For TTL8mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 4.75; I_{OH} = -4.0
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 8.0
I_{OL}			8.0	mA	
I_{OH}			-4.0	mA	
t_{RISE}			10	ns	C_{LOAD} = 25 pF
t_{FALL}			5	ns	C_{LOAD} = 25 pF

Output Parameters For CMOS2mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 4.75; I_{OH} = -2.0
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 2.0
I_{OL}			2.0	mA	
I_{OH}			-2.0	mA	
t_{RISE}			10	ns	C_{LOAD} = 15 pF
t_{FALL}			10	ns	C_{LOAD} = 15 pF
Leakage Tri-state			+/-10	µA	0 to 5.25 V input

Input/Output Parameters For TTL8mA (slew rate controlled)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	$V_{DD} = 5.25$
Input capacitance		7.0		pF	
V_{OH}	V_{DD} - 0.5			V	$V_{DD} = 4.75$; $I_{OH} = -4.0$
V_{OL}			0.4	V	$V_{DD} = 4.75$; $I_{OL} = 8.0$
I_{OL}			8.0	mA	
I_{OH}			-4.0	mA	
t_{RISE}			10	ns	$C_{LOAD} = 25$ pF
t_{FALL}			5	ns	$C_{LOAD} = 25$ pF

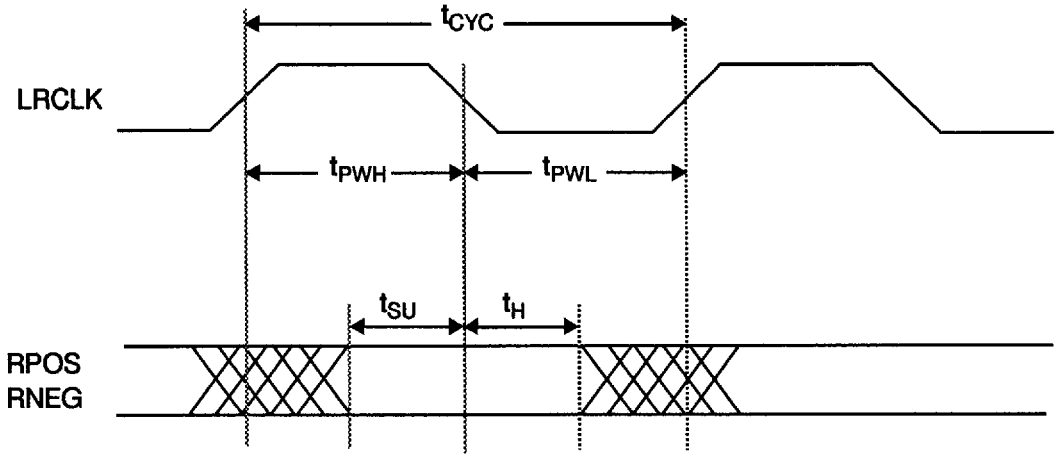
Input/Output Parameters For CMOS2mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	3.15			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			1.65	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	$V_{DD} = 5.25$
Input capacitance		7.0		pF	
V_{OH}	V_{DD} - 0.5			V	$V_{DD} = 4.75$; $I_{OH} = -2.0$
V_{OL}			0.4	V	$V_{DD} = 4.75$; $I_{OL} = 2.0$
I_{OL}			2.0	mA	
I_{OH}			-2.0	mA	
t_{RISE}			10	ns	$C_{LOAD} = 15$ pF
t_{FALL}			10	ns	$C_{LOAD} = 15$ pF
Leakage Tri-state			+/-10	µA	0 to 5.25 V input

TIMING CHARACTERISTICS

Detailed timing diagrams for the QDS1F are illustrated in Figures 14 through 28, with values of the timing intervals following each figure. All output times are measured with a maximum 25 pF load capacitance. Timing parameters are measured at $(V_{OH} + V_{OL})/2$ or $(V_{IH} + V_{IL})/2$ as applicable.

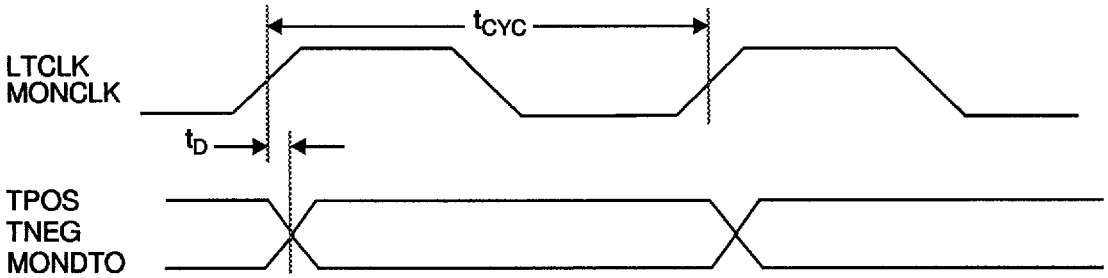
Figure 14. Recovered Clock and Switching Characteristics



Parameter	Symbol	Min	Typ	Max	Unit
LRCLK clock period	t_{CYC}	560	648		ns
LRCLK high time	t_{PWH}	240			ns
LRCLK low time	t_{PWL}	240			ns
RPOS/RNEG set-up time to LRCLK ↓*	t_{SU}	50			ns
RPOS/RNEG hold time after LRCLK ↓*	t_H	50			ns

*LRCLK may be inverted per RXCP; as shown RXCP = 0.

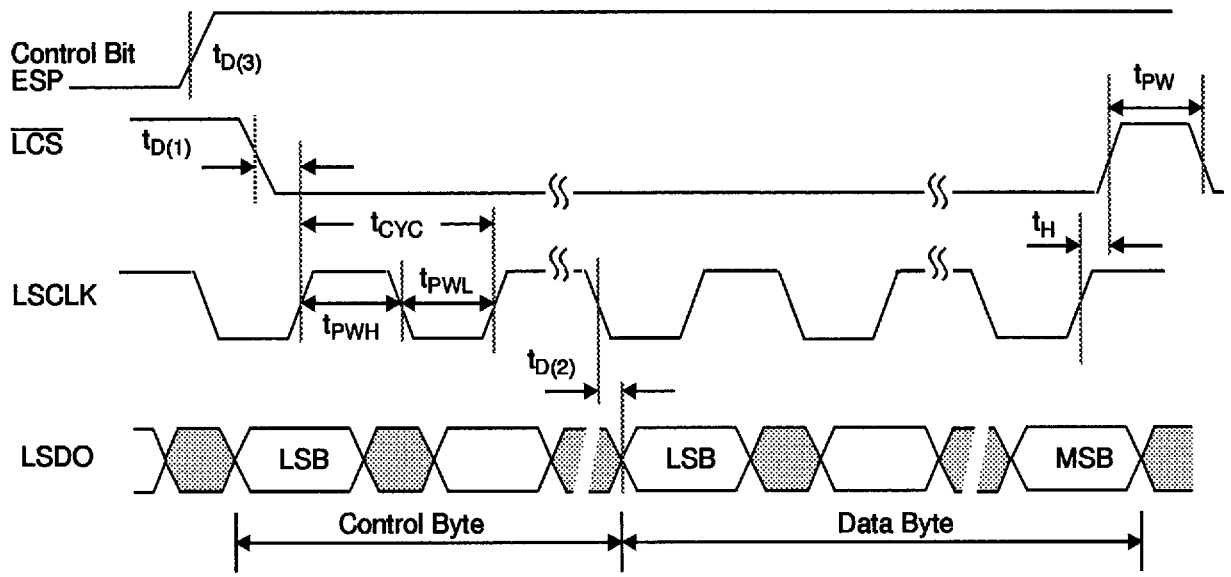
Figure 15. Transmit Clock and Data Switching Characteristics



Parameter	Symbol	Min	Typ	Max	Unit
LTCLK clock period	t_{CYC}	637	648	656	ns
LTCLK duty cycle (t_{PWH}/t_{CYC})	--	45		55	%
TPOS/TNEG delay after LTCLK↑*	t_D	-5		50	ns

*LTCLK may be inverted per TXCP; as shown TXCP = 1.

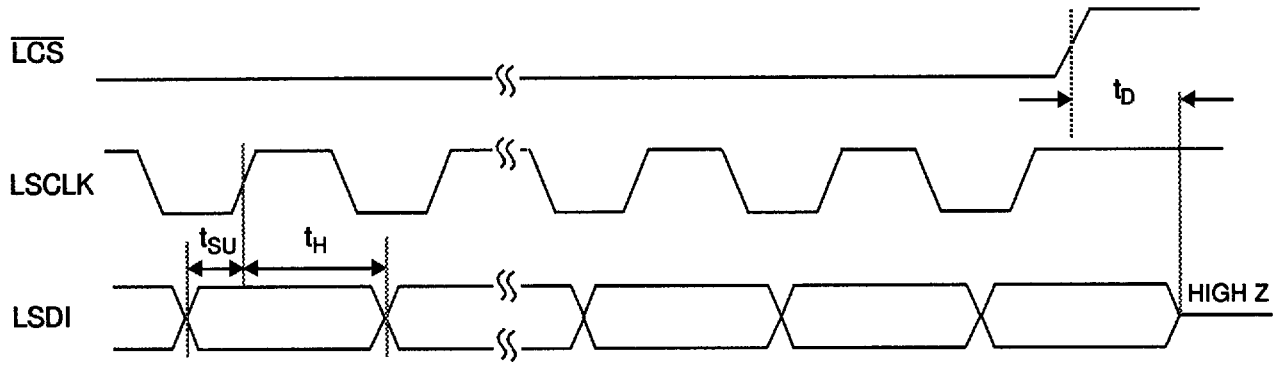
Figure 16. Serial Port Write Timing



Parameter	Symbol	Min	Typ	Max	Unit
$\overline{LCS}$ pulse width	t_{PW}	300			ns
$\overline{LCS}$ hold time after LSCLK↑	t_H	100			ns
LSCLK clock period *	t_{CYC}	560	648		ns
LSCLK high time	t_{PWH}	280			ns
LSCLK low time	t_{PWL}	280			ns
LSCLK delay after $\overline{LCS}$ active	$t_{D(1)}$	100			ns
LSDO valid delay after LSCLK↓	$t_{D(2)}$			100	ns
$\overline{LCS}$ delay after ESP control bit set	$t_{D(3)}$			2 cycles of clock LO	ns

* LSCLK frequency is locked to the frequency of input clock LO.

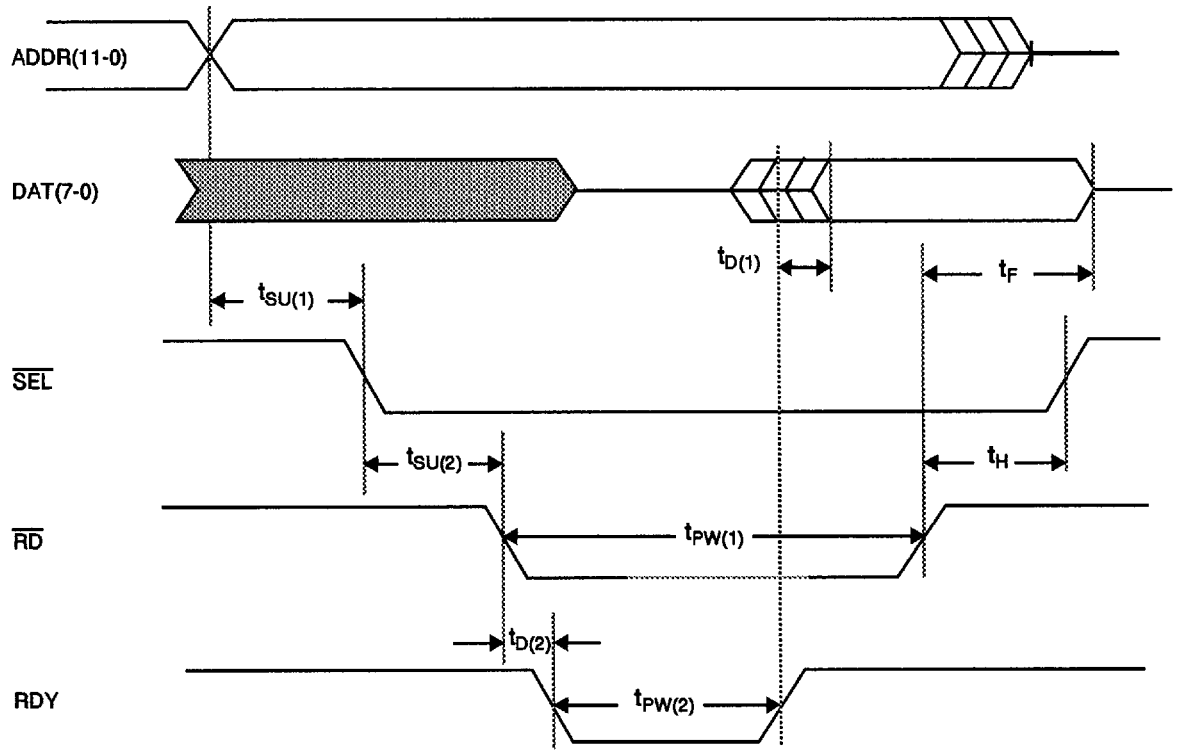
Figure 17. Serial Port Read Timing



Parameter*	Symbol	Min	Typ	Max	Unit
LSDI High Z delay after $\overline{LCS}$ inactive	t_D			100	ns
LSDI set-up time to LSCLK↑	t_{SU}	50			ns
LSDI hold time after LSCLK↑	t_H	50			ns

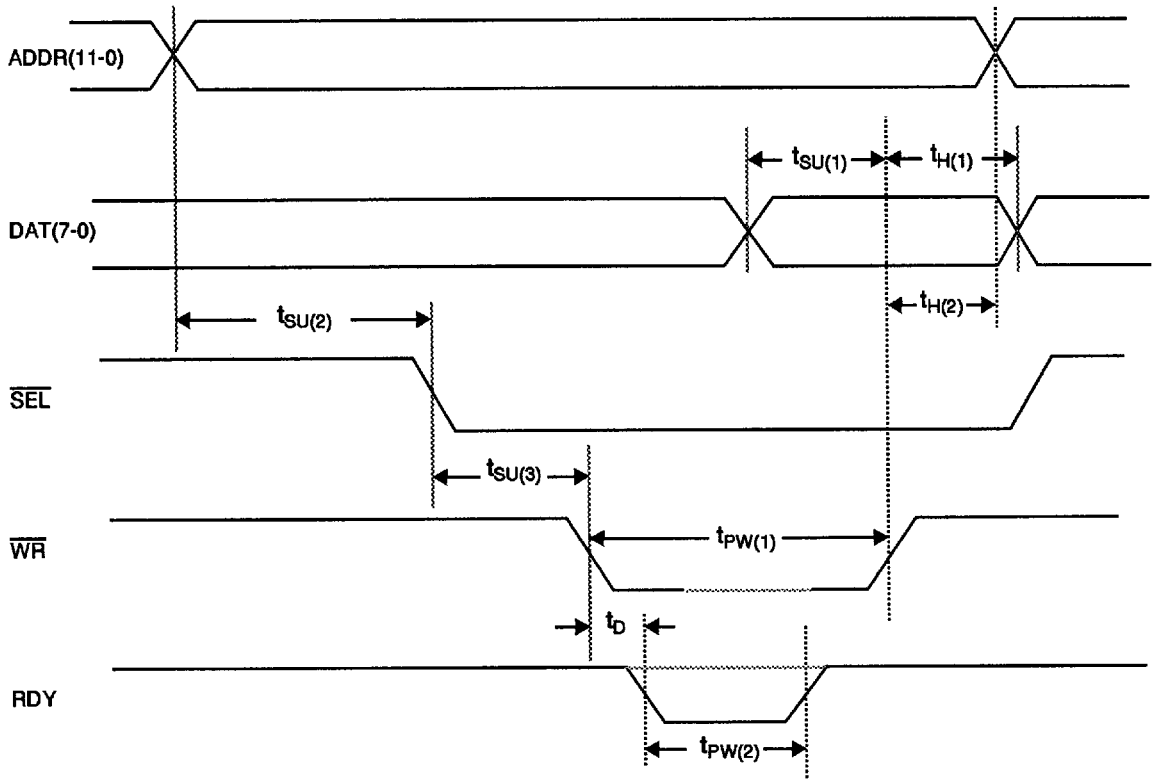
*Note: Timing diagrams and parameter values refer to conditions which prevail when control bit ESP is set to 1.

Figure 18. Intel Microprocessor Read Cycle Timing



Parameter	Symbol	Min	Typ	Max	Unit
ADDR set-up time to $\overline{SEL}\downarrow$	$t_{SU(1)}$			0	ns
DAT valid delay after RDY↑	$t_{D(1)}$		-1/2 cycle of SYSCLK	-10	ns
DAT float time after $\overline{RD}\uparrow$	t_F	1.0	3.0	5.0	ns
$\overline{SEL}$ set-up time to $\overline{RD}\downarrow$	$t_{SU(2)}$	0			ns
$\overline{SEL}$ hold time after $\overline{RD}\uparrow$	t_H	0			ns
$\overline{RD}$ pulse width	$t_{PW(1)}$	50			ns
RDY delay after $\overline{RD}\downarrow$	$t_{D(2)}$	0		12	ns
RDY pulse width	$t_{PW(2)}$	2 cycles of SYSCLK		10 cycles of SYSCLK	ns

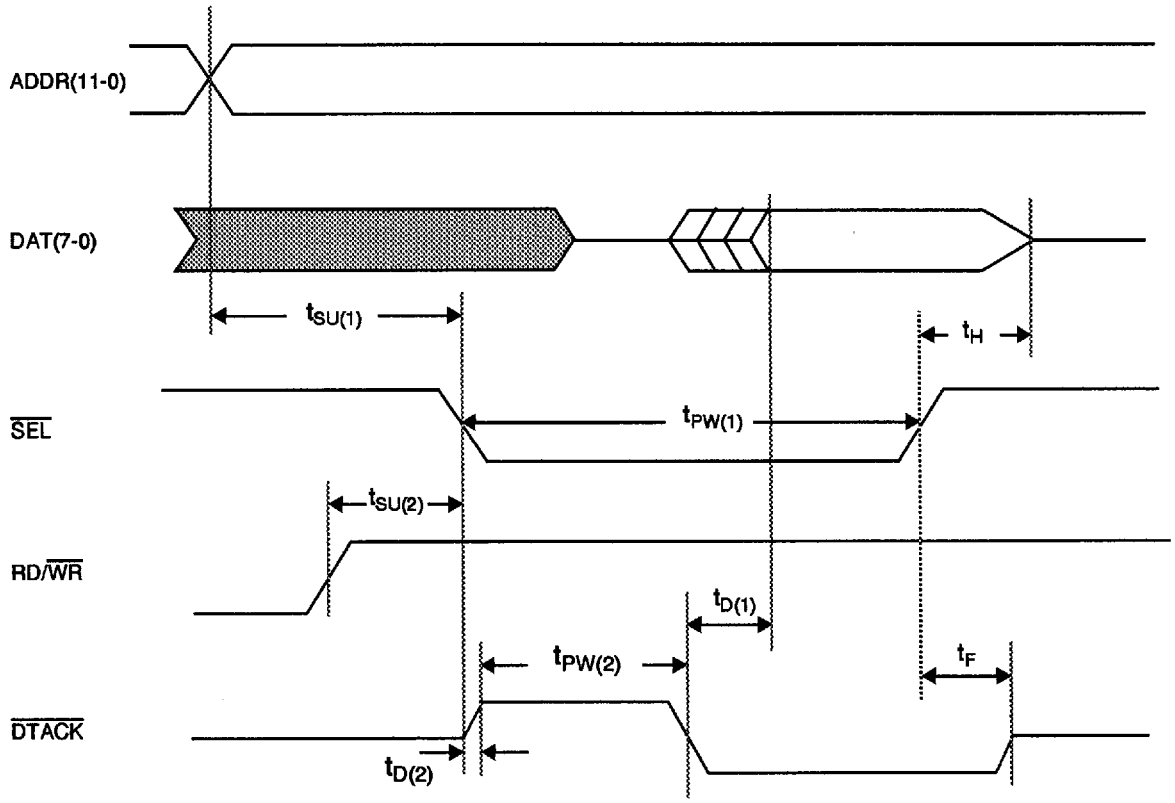
Figure 19. Intel Microprocessor Write Cycle Timing



Parameter	Symbol	Min	Typ	Max	Unit
ADDR set-up time to $\overline{SEL}\downarrow$	$t_{SU(2)}$	0			ns
ADDR hold time after $\overline{WR}\uparrow$	$t_{H(2)}$	5			ns
DAT valid set-up time to $\overline{WR}\uparrow$	$t_{SU(1)}$	20			ns
DAT hold time after $\overline{WR}\uparrow$	$t_{H(1)}$	5			ns
$\overline{SEL}$ set-up time to $\overline{WR}\downarrow$	$t_{SU(3)}$	0			ns
$\overline{WR}$ pulse width	$t_{PW(1)}$	50			ns
RDY delay after $\overline{WR}\downarrow$	t_D	0		12	ns
RDY pulse width	$t_{PW(2)}$	0		10 cycles of SYSCLK*	ns

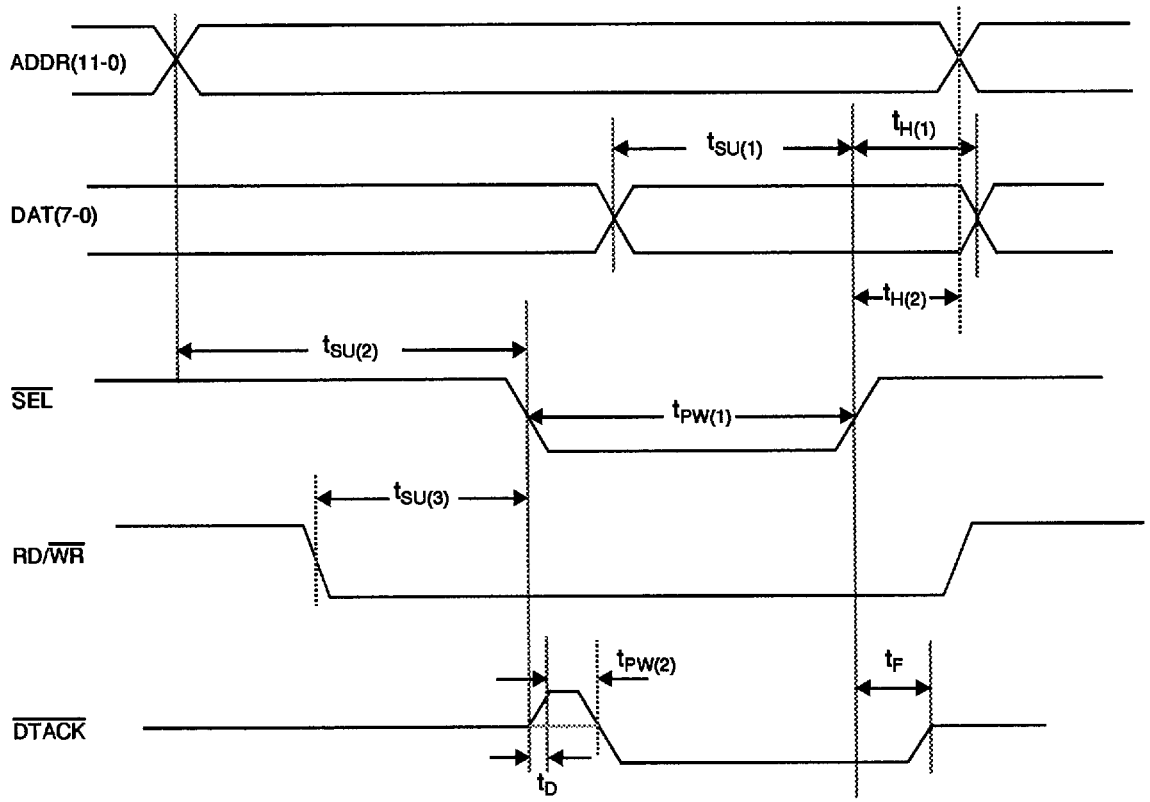
* Wait states only occur if a write cycle immediately follows a previous read or write cycle (e.g.'read modify write' or word wide write).

Figure 20. Motorola Microprocessor Read Cycle Timing



Parameter	Symbol	Min	Typ	Max	Unit
ADDR valid set-up time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	0			ns
DAT hold time after $\overline{SEL}\uparrow$	t_H	1	3	5	ns
DAT output delay after $\overline{DTACK}\downarrow$	$t_{D(1)}$		-1/2 cycle of SYSCLK		ns
$\overline{SEL}$ pulse width	$t_{PW(1)}$	50			ns
RD/$\overline{WR}$ set-up time to $\overline{SEL}\downarrow$	$t_{SU(2)}$	0			ns
$\overline{DTACK}$ pulse width	$t_{PW(2)}$	2 cycles of SYSCLK		10 cycles of SYSCLK	ns
$\overline{DTACK}$ float time after $\overline{SEL}\uparrow$	t_F	1		10	ns
$\overline{DTACK}$ delay after $\overline{SEL}\downarrow$	$t_{D(2)}$	0		12	ns

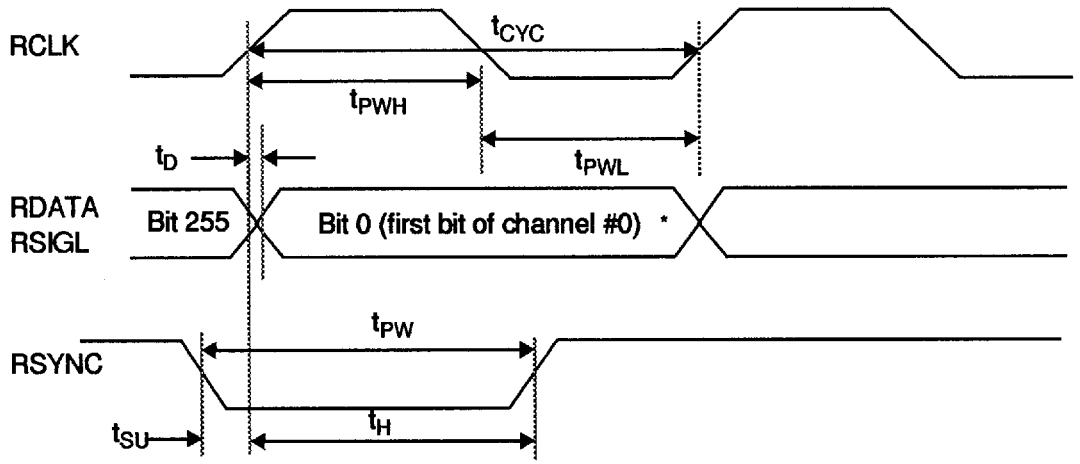
Figure 21. Motorola Microprocessor Write Cycle Timing



Parameter	Symbol	Min	Typ	Max	Unit
ADDR valid set-up time to $\overline{SEL}\downarrow$	$t_{SU(2)}$	0			ns
ADDR hold time after $\overline{SEL}\uparrow$	$t_{H(2)}$	5			ns
DAT valid set-up time to $\overline{SEL}\uparrow$	$t_{SU(1)}$	20			ns
$\overline{SEL}$ pulse width	$t_{PW(1)}$	50			ns
DATA valid hold time after $\overline{SEL}\uparrow$	$t_{H(1)}$	5			ns
RD/$\overline{WR}$ set-up time to $\overline{SEL}\downarrow$	$t_{SU(3)}$	0			ns
$\overline{DTACK}$ pulse width	$t_{PW(2)}$	0		10 cycles of SYSCLK*	ns
$\overline{DTACK}$ float time after $\overline{SEL}\uparrow$	t_F	1		10	ns
$\overline{DTACK}$ delay after $\overline{SEL}\downarrow$	t_D	0		12	ns

* Wait states only occur if a write cycle immediately follows a previous read or write cycle (e.g.'read modify write' or word wide write).

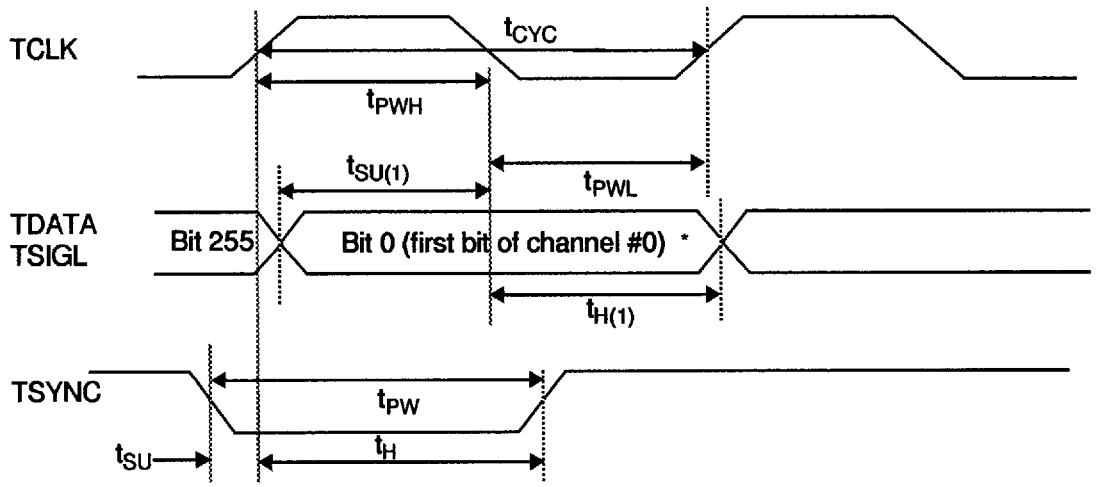
Figure 22. System Interface Output (MVIP Mode)



Parameter	Symbol	Min	Typ	Max	Unit
RCLK clock period	t_{CYC}	465	488.3	513	ns
RCLK low time	t_{PWL}	220	244	268	ns
RCLK high time	t_{PWH}	220	244	268	ns
RDATA/RSIGL delay after RCLK ↑	t_D	20	90	125	ns
RSYNC setup time to RCLK ↑	t_{SU}	20			ns
RSYNC hold time after RCLK ↑	t_H	20			ns
RSYNC pulse width	t_{PW}	200		500	ns
RCLK/RSYNC transition times	t_R			11	ns

*As shown RSYNC offset is zero. RSYNC may be delayed up to four clock periods. With an offset of zero, this position could be Bit 1, Bit 2 or Bit 3 of channel #0. However, the rising edge of RCLK will reset this position to Bit 0 of channel #0.

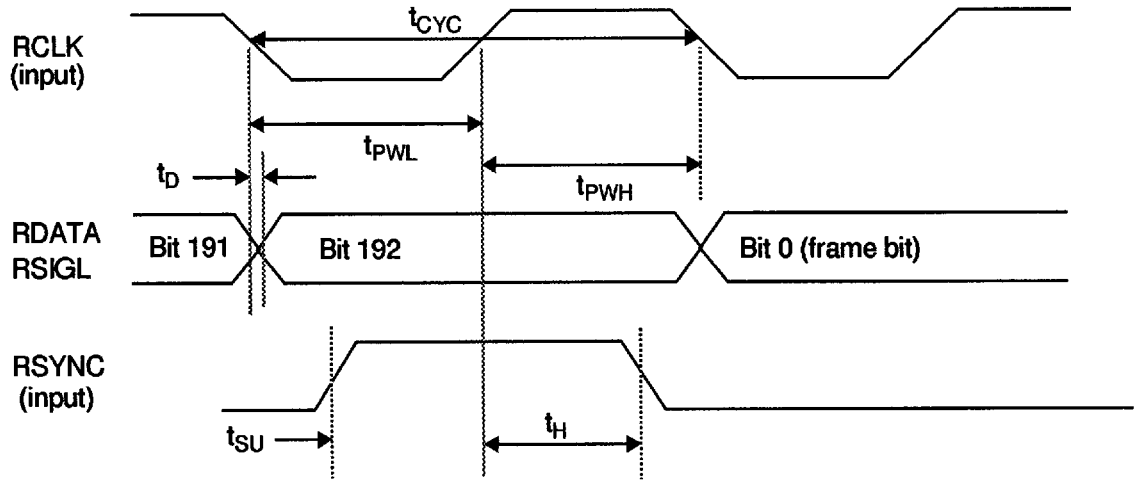
Figure 23. System Interface Input (MVIP Mode)



Parameter	Symbol	Min	Typ	Max	Unit
TCLK clock period	t_{CYC}	480	488.3	497	ns
TCLK low / high time	t_{PWL}/t_{PWH}	220	244	268	ns
TDATA/TSIGL setup time to TCLK ↓	$t_{SU(1)}$	30			ns
TDATA/TSIGL hold time after TCLK ↓	$t_{H(1)}$	224			ns
TSYNC setup time to TCLK ↑	t_{SU}	20			ns
TSYNC hold time after TCLK ↑	t_H	20			ns
TSYNC pulse width	t_{PW}	200		500	ns
TCLK/TSYNC transition times	t_R			11	ns

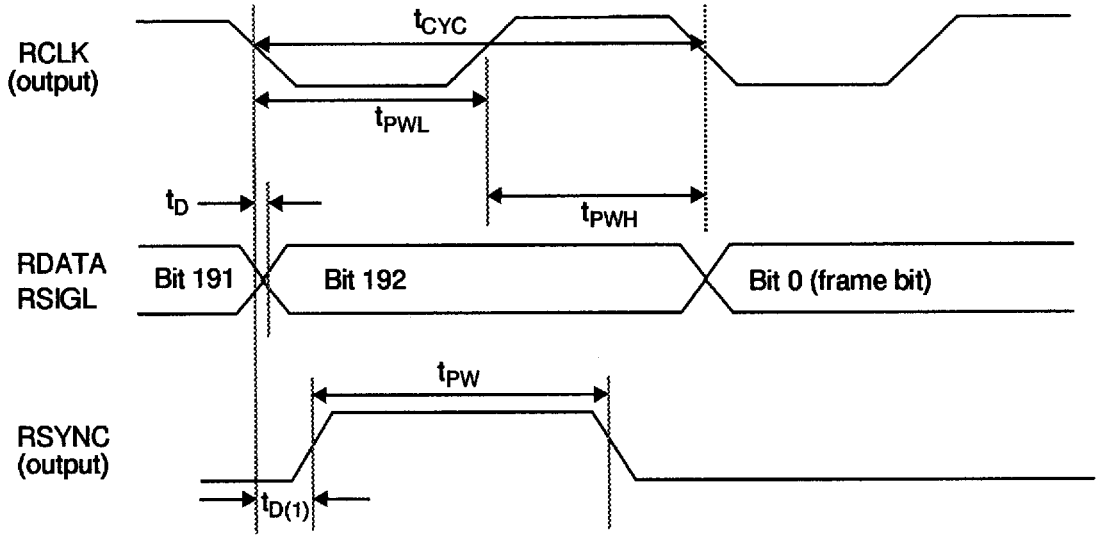
*As shown TSYNC offset is zero. TSYNC may be delayed up to four clock periods. With an offset of zero, this position could be Bit 1, Bit 2 or Bit 3 of channel #0. However, the rising edge of TCLK will reset this position to Bit 0 of channel #0.

Figure 24. System Interface Output (Transmission Mode / System Clock)



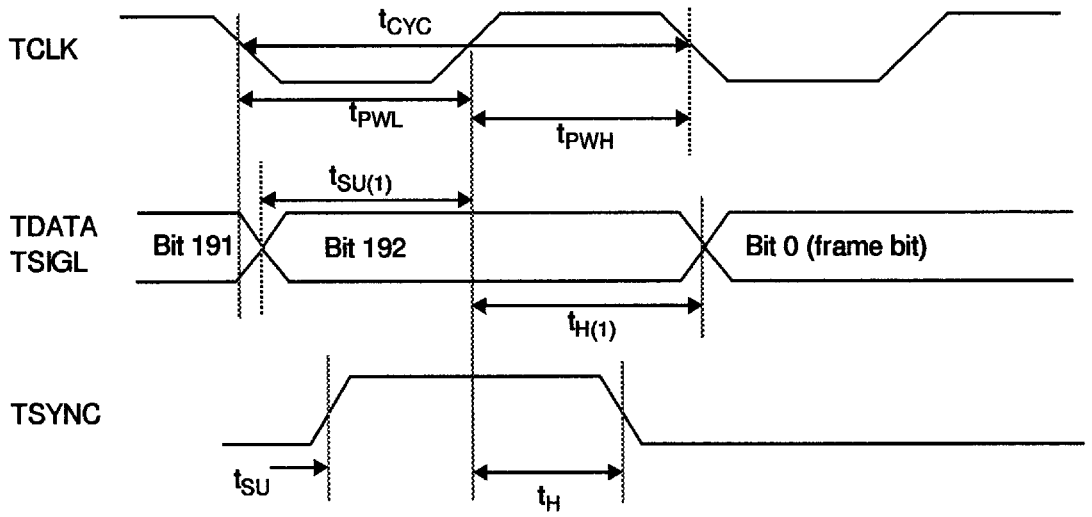
Parameter	Symbol	Min	Typ	Max	Unit
RCLK clock period	t_{CYC}	560	648		ns
RCLK low time	t_{PWL}	240			ns
RCLK high time	t_{PWH}	240			ns
RDATA/RSIGL delay after RCLK↓	t_D	0		50	ns
RSYNC setup time to RCLK↑	t_{SU}	20			ns
RSYNC hold time after RCLK↑	t_H	20			ns
RCLK/RSYNC rise or fall times	t_R			11	ns

Figure 25. System Interface Output (Transmission Mode / Receive Clock)



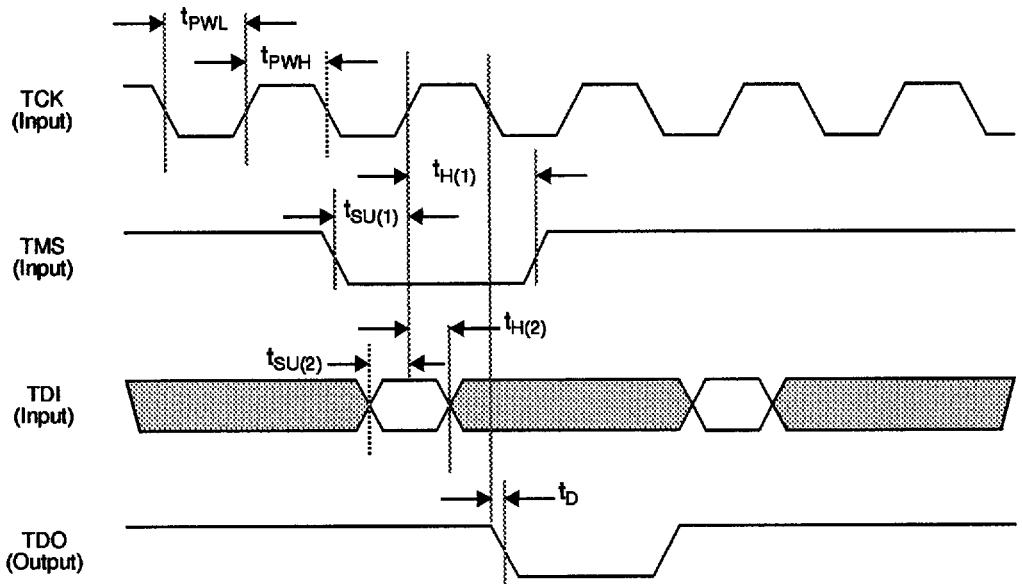
Parameter	Symbol	Min	Typ	Max	Unit
RCLK clock period	t_{CYC}	560	648		ns
RCLK low time	t_{PWL}	240			ns
RCLK high time	t_{PWH}	240			ns
RDATA/RSIGL delay after RCLK↓	t_D			50	ns
RSYNC delay time after RCLK↓	$t_{D(1)}$	0		50	ns
RSYNC pulse width	t_{PW}	500		750	ns
RCLK/RSYNC rise and fall times	t_R			11	ns

Figure 26. System Interface Input (Transmission Mode)



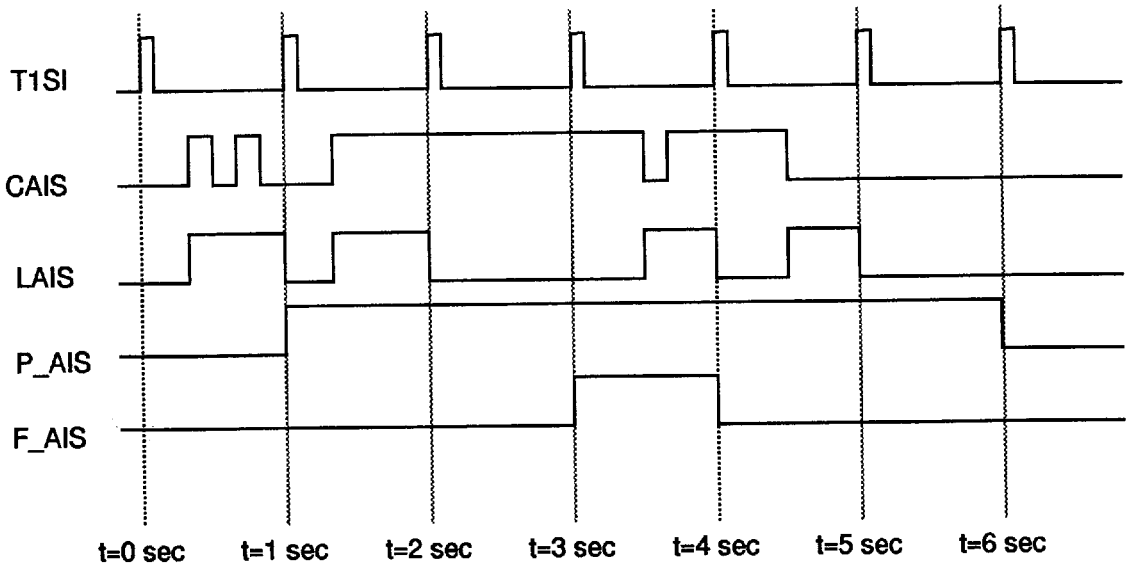
Parameter	Symbol	Min	Typ	Max	Unit
TCLK clock period	t_{CYC}	560	648		ns
TCLK low time	t_{PWL}	240			ns
TCLK high time	t_{PWH}	240			ns
TDATA/TSIGL setup time to TCLK ↑	$t_{SU(1)}$	20			ns
TDATA/TSIGL hold time after TCLK ↑	$t_{H(1)}$	20			ns
TSYNC setup time to TCLK ↑	t_{SU}	20			ns
TSYNC hold time after TCLK ↑	t_H	20			ns
TCLK/TSYNC rise or fall times	t_R			11	ns

Figure 27. Boundary Scan Timing



Parameter	Symbol	Min	Max	Unit
TCK clock high time	t_{PWH}	50		ns
TCK clock low time	t_{PWL}	50		ns
TMS setup time for TCK↑	$t_{SU(1)}$	3.0	-	ns
TMS hold time after TCK↑	$t_{H(1)}$	2.0	-	ns
TDI setup time for TCK↑	$t_{SU(2)}$	3.0	-	ns
TDI hold time after TCK↑	$t_{H(2)}$	2.0	-	ns
TDO delay from TCK↓	t_D	-	7.0	ns

Figure 28. Operation of Performance Monitoring and Fault Monitoring Latching for AIS



Note: The example shown in the above diagram refers to AIS. The same logic applies to LOS, OOF, YEL, CFA, SEF, TXSLIP and RXSLIP. P_ and F_ represent the results of the previous one-second interval during the current one-second interval.

MEMORY MAP

MEMORY MAP PARTITIONING

Hex Address Range	Channel	Functions
000 - 0FF	Common	Device ID, Serial Port Control, Loop Code and Interrupt C[redacted]ol
100 - 1FF	#1	Status, Control, PM/FM, Error Counters and Signaling Ac[redacted]
200 - 2FF	#2	Status, Control, PM/FM, Error Counters and Signaling Ac[redacted]
300 - 3FF	#3	Status, Control, PM/FM, Error Counters and Signaling Ac[redacted]
400 - 4FF	#4	Status, Control, PM/FM, Error Counters and Signaling Ac[redacted]
500 - FFF	Reserved	

COMMON MEMORY

Notes:
Addresses shown as shaded are cleared by software reset (91H value in Address 005H).
*R/W: Read/write; R: Read only; W: Write only.
Bits shown as 'R' in columns Bit 7 through Bit 0 must be set to zero by the microprocessor for proper device ope[redacted]n.

Address (Hex)	Mode*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit [redacted]0
000	R	MI7	MI6	MI5	MI4	MI3	MI2	MI1	[redacted]
001	R	PN3	PN2	PN1	PN0	MI11	MI10	MI9	[redacted]
002	R	PN11	PN10	PN9	PN8	PN7	PN6	PN5	[redacted]
003	R	V3	V2	V1	V0	PN15	PN14	PN13	[redacted]2
004	R/W	Notebook							
005	R/W	Reset							
006	R/W	GIM	RISE	FALL	IPOL	ENPMFM	R	R	[redacted]WM
007	SPARE								
008	SPARE								
009	SPARE								
00A	R	LOS	AIS	OOF	YEL	CFA	SEF	TXSLIP	[redacted]LIP
00B	R/W	GMLOS	GMAIS	GMOOF	GMYEL	GMCFA	GMSEF	GMTXSLIP	G[redacted]SLIP
00C	R	R	R	R	R	CH4	CH3	CH2	[redacted]1
00D	SPARE								
00E	R	R	R	R	R	CH4	CH3	CH2	[redacted]1
00F	SPARE								
010	R/W	D7	D6	D5	D4	D3	D2	D1	[redacted]
011	R/W	D7	D6	D5	D4	D3	D2	D1	[redacted]
012	R	D7	D6	D5	D4	D3	D2	D1	[redacted]
013	R/W	BDCST	PRBSFR	PRBSEN	ESP/ EMON	RXTX	R	DS1 channel n[redacted]ered (0-3)	
014	R/W	R	TLU6	TLU5	TLU4	TLU3	TLU2	TLU1	[redacted]U0
015	R/W	R	TLD6	TLD5	TLD4	TLD3	TLD2	TLD1	[redacted]D0
016	R/W	R	R	R	ULEN1	ULEN0	R	DLEN1	[redacted]EN0
017	R/W	TSD7	TSD6	TSD5	TSD4	TSD3	TSD2	TSD1	[redacted]D0
018	R/W	RSD7	RSD6	RSD5	RSD4	RSD3	RSD2	RSD1	[redacted]D0
019	R/W	DS1 channel numbered (0-3) for CLKREF2		ENREF2	1544KHZ	ENREF1	R	DS1 channel n[redacted]ered (0-3) for CL[redacted]F1	
020 - 0FE	SPARE								
0FF	R/W	R	R	R	R	R	R	R	[redacted]

PER CHANNEL MEMORY

Note: In the address, X = 1 to 4, where X identifies the DS1 framers 1 through 4.
Shaded addresses are cleared by a software reset (either by RESET at Address 005H or by control bit SRST at Address X05H, bit 7).
Shaded bits require soft reset to execute properly.
Bits shown as 'R' must be set to zero by the microprocessor for proper device operation.

Address (Hex)	Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X00	R/W	MODE	BE	ENZC	ENSYEL	FOD	ENSAIS	LIE	RPOL
X01	R/W	TXCP	RXCP	TXNRZP	PWRD	FDAT	FPOL	BFDL	RNRZP
X02	R/W	TXC1	TXC0	RXC	TSE	RSE	TSR	RSR	R
X03	R/W	TYP1	TYP0	RXF	TXF	OSE	ENAIS	ENOOF	RLOS
X04	R/W	OOF1	OOF0	ALT	SYC1	SYC0	FMD1	FMD0	RSYC
X05	R/W	SRST	ALUP	TXUP	TXDN	PAYL	TX1S	RLP	LLP
X06	R/W	R	R	R	R	INSPRBS	SFZ	RXFS	TXFS
X07	R/W	R	SYSVTAIS	SYSALL1	CRC	FRME	YEL	AIS	BPV
X08	R/W	EHR	EHT	TAB	EOM	RHIE	THIE	EBRI	EBT
X09	R/W	MLOS	MAIS	MOOF	MYEL	MCFA	MSEF	MTXSLIP	MRXSLIP
X0A	W	D7	D6	D5	D4	D3	D2	D1	D0
X0B	R/W	R	R	D5	D4	D3	D2	D1	D0
X0C	SPARE								
X0D	SPARE								
X0E	R/W=clr	ERHIS2	ERHIS1	ERHIS0	ETHIS	ERXFS1	ERXFS0	ETXFS1	ETXFS0
X0F	R/W	MRHIS2	MRHIS1	MRHIS0	MTHIS	MRXFS1	MRXFS0	MTXFS1	MTXFS0
X10	R	CLOS	CAIS	COOF	CYEL	CCFA	CSEF	CTXSLIP	CRXSLIP
X11	R/W=clr	LLOS	LAIS	LOOF	LYEL	LCFA	LSEF	LTXSLIP	LRXSLIP
X12	R/W	P_LOS	P_AIS	P_OOF	P_YEL	P_CFA	P_SEF	P_TXSLIP	P_RXSLIP
X13	R/W	F_LOS	F_AIS	F_OOF	F_YEL	F_CFA	F_SEF	F_TXSLIP	F_RXSLIP
X14	R	TXS1	TXS0	RXS1	RXS0	VTAIS	VTRDI	R	R
X15	R	RXFS	TXFS	R	R	R	UP	DOWN	LINT
X16	R	RHIS2	RHIS1	RHIS0	THIS	RXFS1	RXFS0	TXFS1	TXFS0
X17	R	D7	D6	D5	D4	D3	D2	D1	D0
X18	R	R	R	R	C4	C3	C2	C1	C0
X19	R	R	R	D5	D4	D3	D2	D1	D0
X1A - X1F	SPARE								
X20	R/W	TWP7	TWP6	TWP5	TWP4	TWP3	TWP2	TWP1	TWP0
X21	R/W	TRP7	TRP6	TRP5	TRP4	TRP3	TRP2	TRP1	TRP0
X22	R/W	TWSBS	R	R	TWPF4	TWPF3	TWPF2	TWPF1	TWPF0
X23	R/W	TRSBS	R	R	TRPF4	TRPF3	TRPF2	TRPF1	TRPF0

Address (Hex)	Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X24	R/W	RWP7	RWP6	RWP5	RWP4	RWP3	RWP2	RWP1	RWP0
X25	R/W	RRP7	RRP6	RRP5	RRP4	RRP3	RRP2	RRP1	RRP0
X26	R/W	RWSBS	R	R	RWPF4	RWPF3	RWPF2	RWPF1	RWPF0
X27	R/W	RRSBS	R	R	RRPF4	RRPF3	RRPF2	RRPF1	RRPF0
X28 - X2F	SPARE								
X30	R/W	Fe2/Fs4	D1/Ft4	CRC2/Fs3	D1/Ft3	Fe1/Fs2	D1/Ft2	CRC1/Fs1	D1/Ft1
X31	R/W	Fe4/X	D1/X	CRC4/X	D1/X	Fe3/Fs6	D1/Ft6	CRC3/Fs5	D1/Ft5
X32	R/W	Fe6/X	D1/X	CRC6/X	D1/X	Fe5/X	D1/X	CRC5/X	D1/X
X33	R/W	Fe2/Fs4	D1/Ft4	CRC2/Fs3	D1/Ft3	Fe1/Fs2	D1/Ft2	CRC1/Fs1	D1/Ft1
X34	R/W	Fe4/X	D1/X	CRC4/X	D1/X	Fe3/Fs6	D1/Ft6	CRC3/Fs5	D1/Ft5
X35	R/W	Fe6/X	D1/X	CRC6/X	D1/X	Fe5/X	D1/X	CRC5/X	D1/X
X36 - X37	RESERVED								
X38	R/W	LBCC7	LBCC6	LBCC5	LBCC4	LBCC3	LBCC2	LBCC1	LBCC0
X39	R/W	LBCC15	LBCC14	LBCC13	LBCC12	LBCC11	LDCC10	LBCC9	LBCC8
X3A - X3F	RESERVED								
X40	R/W	RDS0(1)							
X41	R/W	RDS0(2)							
X42	R/W	RDS0(3)							
X43	R/W	RDS0(4)							
X44	R/W	RDS0(5)							
X45	R/W	RDS0(6)							
X46	R/W	RDS0(7)							
X47	R/W	RDS0(8)							
X48	R/W	RDS0(9)							
X49	R/W	RDS0(10)							
X4A	R/W	RDS0(11)							
X4B	R/W	RDS0(12)							
X4C	R/W	RDS0(13)							
X4D	R/W	RDS0(14)							
X4E	R/W	RDS0(15)							
X4F	R/W	RDS0(16)							
X50	R/W	RDS0(17)							
X51	R/W	RDS0(18)							
X52	R/W	RDS0(19)							
X53	R/W	RDS0(20)							

Address (Hex)	Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X54	R/W	RDS0(21)							
X55	R/W	RDS0(22)							
X56	R/W	RDS0(23)							
X57	R/W	RDS0(24)							
X58	R/W	RDS0(1)							
X59	R/W	RDS0(2)							
X5A	R/W	RDS0(3)							
X5B	R/W	RDS0(4)							
X5C	R/W	RDS0(5)							
X5D	R/W	RDS0(6)							
X5E	R/W	RDS0(7)							
X5F	R/W	RDS0(8)							
X60	R/W	RDS0(9)							
X61	R/W	RDS0(10)							
X62	R/W	RDS0(11)							
X63	R/W	RDS0(12)							
X64	R/W	RDS0(13)							
X65	R/W	RDS0(14)							
X66	R/W	RDS0(15)							
X67	R/W	RDS0(16)							
X68	R/W	RDS0(17)							
X69	R/W	RDS0(18)							
X6A	R/W	RDS0(19)							
X6B	R/W	RDS0(20)							
X6C	R/W	RDS0(21)							
X6D	R/W	RDS0(22)							
X6E	R/W	RDS0(23)							
X6F	R/W	RDS0(24)							
X70-X7F	RESERVED								
X80	R/W	A8	A7	A6	A5	A4	A3	A2	A1
X81	R/W	A16	A15	A14	A13	A12	A11	A10	A9
X82	R/W	A24	A23	A22	A21	A20	A19	A18	A17
X83	RESERVED								
X84	R/W	B8	B7	B6	B5	B4	B3	B2	B1
X85	R/W	B16	B15	B14	B13	B12	B11	B10	B9

Address (Hex)	Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X86	R/W	B24	B23	B22	B21	B20	B19	B18	B17
X87	RESERVED								
X88	R/W	C8	C7	C6	C5	C4	C3	C2	C1
X89	R/W	C16	C15	C14	C13	C12	C11	C10	C9
X8A	R/W	C24	C23	C22	C21	C20	C19	C18	C17
X8B	RESERVED								
X8C	R/W	D8	D7	D6	D5	D4	D3	D2	D1
X8D	R/W	D16	D15	D14	D13	D12	D11	D10	D9
X8E	R/W	D24	D23	D22	D21	D20	D19	D18	D17
X8F	RESERVED								
X90	R/W	TDS0(1)							
X91	R/W	TDS0(2)							
X92	R/W	TDS0(3)							
X93	R/W	TDS0(4)							
X94	R/W	TDS0(5)							
X95	R/W	TDS0(6)							
X96	R/W	TDS0(7)							
X97	R/W	TDS0(8)							
X98	R/W	TDS0(9)							
X99	R/W	TDS0(10)							
X9A	R/W	TDS0(11)							
X9B	R/W	TDS0(12)							
X9C	R/W	TDS0(13)							
X9D	R/W	TDS0(14)							
X9E	R/W	TDS0(15)							
X9F	R/W	TDS0(16)							
XA0	R/W	TDS0(17)							
XA1	R/W	TDS0(18)							
XA2	R/W	TDS0(19)							
XA3	R/W	TDS0(20)							
XA4	R/W	TDS0(21)							
XA5	R/W	TDS0(22)							
XA6	R/W	TDS0(23)							
XA7	R/W	TDS0(24)							
XA8	R/W	TDS0(1)							

Address (Hex)	Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
XA9	R/W	TDS0(2)							
XAA	R/W	TDS0(3)							
XAB	R/W	TDS0(4)							
XAC	R/W	TDS0(5)							
XAD	R/W	TDS0(6)							
XAE	R/W	TDS0(7)							
XAF	R/W	TDS0(8)							
XB0	R/W	TDS0(9)							
XB1	R/W	TDS0(10)							
XB2	R/W	TDS0(11)							
XB3	R/W	TDS0(12)							
XB4	R/W	TDS0(13)							
XB5	R/W	TDS0(14)							
XB6	R/W	TDS0(15)							
XB7	R/W	TDS0(16)							
XB8	R/W	TDS0(17)							
XB9	R/W	TDS0(18)							
XBA	R/W	TDS0(19)							
XBB	R/W	TDS0(20)							
XBC	R/W	TDS0(21)							
XBD	R/W	TDS0(22)							
XBE	R/W	TDS0(23)							
XBF	R/W	TDS0(24)							
XC0-XCF	RESERVED								
XD0	R/W	A8	A7	A6	A5	A4	A3	A2	A1
XD1	R/W	A16	A15	A14	A13	A12	A11	A10	A9
XD2	R/W	A24	A23	A22	A21	A20	A19	A18	A17
XD3	RESERVED								
XD4	R/W	B8	B7	B6	B5	B4	B3	B2	B1
XD5	R/W	B16	B15	B14	B13	B12	B11	B10	B9
XD6	R/W	B24	B23	B22	B21	B20	B19	B18	B17
XD7	RESERVED								
XD8	R/W	C8	C7	C6	C5	C4	C3	C2	C1
XD9	R/W	C16	C15	C14	C13	C12	C11	C10	C9
XDA	R/W	C24	C23	C22	C21	C20	C19	C18	C17

Address (Hex)	Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
XDB	RESERVED								
XDC	R/W	D8	D7	D6	D5	D4	D3	D2	D1
XDD	R/W	D16	D15	D14	D13	D12	D11	D10	D9
XDE	R/W	D24	D23	D22	D21	D20	D19	D18	D17
XDF	RESERVED								
XE0	R/W	RDE8	RDE7	RDE6	RDE5	RDE4	RDE3	RDE2	RDE1
XE1	R/W	RDE16	RDE15	RDE14	RDE13	RDE12	RDE11	RDE10	RDE9
XE2	R/W	RDE24	RDE23	RDE22	RDE21	RDE20	RDE19	RDE18	RDE17
XE3	RESERVED								
XE4	R/W	TDE8	TDE7	TDE6	TDE5	TDE4	TDE3	TDE2	TDE1
XE5	R/W	TDE16	TDE15	TDE14	TDE13	TDE12	TDE11	TDE10	TDE9
XE6	R/W	TDE24	TDE23	TDE22	TDE21	TDE20	TDE19	TDE18	TDE17
XE7	RESERVED								
XE8	R/W	SE8	SE7	SE6	SE5	SE4	SE3	SE2	SE1
XE9	R/W	SE16	SE15	SE14	SE13	SE12	SE11	SE10	SE9
XEA	R/W	SE24	SE23	SE22	SE21	SE20	SE19	SE18	SE17
XEB	RESERVED								
XEC-XEF	RESERVED								
XF0	R/W	LCRC7	LCRC6	LCRC5	LCRC4	LCRC3	LCRC2	LCRC1	LCRC0
XF1	R/W	LCRCO	R	R	R	R	R	R	LCRC8
XF2	R/W=clr	CRC7	CRC6	CRC5	CRC4	CRC3	CRC2	CRC1	CRC0
XF3	R/W=clr	CRCO	R	R	R	R	R	R	CRC8
XF4	R/W	LCV7	LCV6	LCV5	LCV4	LCV3	LCV2	LCV1	LCV0
XF5	R/W	LCV15	LCV14	LCV13	LCV12	LCV11	LCV10	LCV9	LCV8
XF6	R/W=clr	LBPVO	R	R	R	R	R	R	R
XF7	R/W=clr	CV7	CV6	CV5	CV4	CV3	CV2	CV1	CV0
XF8	R/W=clr	CV15	CV14	CV13	CV12	CV11	CV10	CV9	CV8
XF9	R/W=clr	BPVO	R	R	R	R	R	R	R
XFA	R/W	LFBE7	LFBE6	LFBE5	LFBE4	LFBE3	LFBE2	LFBE1	LFBE0
XFB	R/W=clr	LFBOF	R	R	R	R	R	R	R
XFC	R/W=clr	FBE7	FBE6	FBE5	FBE4	FBE3	FBE2	FBE1	FBE0
XFD	R/W=clr	FBOF	R	R	R	R	R	R	R
XFE-XFF	RESERVED								

MEMORY MAP DESCRIPTIONS

Note: All memory addresses are stated in hexadecimal.

COMMON MEMORY

Device ID, Notebook and Reset

Address	Bit	Symbol	Description
000	7-0	MI7-MI0	**Manufacturer Identity:** Read only register containing the LS two nibbles of the device manufacturer's identity (6B Hex).
001	7-4	PN3-PN0	**Part Number:** Read only register containing the first (LS) nibble of the device part number (E Hex). (Note: 03102 = 0C1E Hex.)
	3-0	MI11-MI8	**Manufacturer Identity:** Read only register containing the MS nibble of the device manufacturer's identity (0 Hex).
002	7-0	PN11-PN4	**Part Number:** Read only register containing the third and second nibbles of the device part number (C1 Hex).
003	7-4	V3-V0	**Version:** Read only register containing the device version number.
	3-0	PN15-PN12	**Part Number:** Read only register containing the fourth (MS) nibble of the device part number (0 Hex).
004	7-0	Notebook	**User Register:** Read/write register for end-user application. The content of this register will have no effect on the operation of the device.
005	7-0	Reset	**Software Reset:** Writing a 91 Hex into this location will generate a software reset to the component. Writing other than 91 Hex to this location will remove the QDS1F from the reset state. Reading this location will return a 00 Hex if the QDS1F is not in reset and 01 Hex if the QDS1F is in reset. The QDS1F will default to reset deactivated on external hardware reset (e.g., power-up). At least 40 ms after power-up, software reset should be used to clear the QDS1F prior to programming its operational mode. Software Reset resets performance counters and latched/shadow registers, as well as all internal state machines. Mode controls are not affected.

Global Registers

Address	Bit	Symbol	Description
006	7	GIM	**Global Interrupt Mask:** When cleared, the external interrupt output pin will be asserted when an internal interrupt event occurs. The internal interrupt status may still be polled by software to detect interrupt events when this bit is set.
	6	RISE	**Rising Edge Interrupt:** When set, internal interrupts will be registered in their appropriate latched value bits on the rising edge of (start of) an event. See ENPMFM below.
	5	FALL	**Falling Edge Interrupt:** When set, internal interrupts will be registered in their appropriate latched value bits on the falling edge of (end of) an event. See ENPMFM below.
	4	IPOL	**Interrupt Polarity:** When set, the polarity of the interrupt pin will be inverted at the pin.
	3	ENPMFM	**Enable PM/FM function:** When set the Performance Monitoring and Fault Monitoring function is the shadow registers (X12 & X13) and the latched counters (XFA, XF4/5 & XF0/1). The latching takes place after the rising edge of T1SI. This bit must be set to 1 to cause the loop-up and loop-down codes to be integrated. Figure 28 shows waveform diagrams illustrating the operation of PM and FM latching for AIS. Note that RISE, FALL and ENPMFM are set.
	2-1	R	**Reserved:** Set to zero.
	0	ENHWM	**Enable Hardware Mask:** When set, the detector masking is enabled. Shading indicates that these alarms are masked by the conditions to the left; for example, LOS masks AIS, OOF and Yellow.

Direction

Direction	LOS	AIS	OOF	YEL	SLIP
Line Port to System	X				
		X			
			X		

007-009			**Spare:**
00A	7	LOS	**LOS Error:** This bit will be set if there is a loss of signal in any of the channels. This bit will be cleared when all LOS errors have been cleared in the individual channel event registers.
	6	AIS	**AIS Error:** This bit will be set if there is an AIS error in any of the channels. This bit will be cleared when all AIS errors have been cleared in the individual channel event registers.
	5	OOF	**OOF Error:** This bit will be set if there is an out of frame error in any of the channels. This bit will be cleared when all out of frame errors have been cleared in the individual channel event registers.

Address	Bit	Symbol	Description
00A	4	YEL	**YEL Error:** This bit will be set if there is a yellow alarm error in any of the channels. This bit will be cleared when all yellow alarm errors have been cleared in the individual channel event registers.
	3	CFA	**CFA Error:** This bit will be set if there is a change of frame alignment error in any of the channels. This bit will be cleared when all CFA errors have been cleared in the individual channel event registers.
	2	SEF	**Severely Errored Frame:** This bit will be set if a severely errored frame is detected in any of the channels. This bit will be cleared when all SEFs have been cleared in the individual channel event registers.
	1	TXSLIP	**Transmit Slip Event:** This bit will be set if the transmit slip buffer executes a slip in any of the channels. This bit will be cleared when all transmit slip events have been cleared in the individual channel event registers.
	0	RXSLIP	**Receive Slip Event:** This bit will be set if the receive slip buffer executes a slip in any of the channels. This bit will be cleared when all receive slip events have been cleared in the individual channel event registers.
00B	7	GMLOS	**LOS Mask:** When set, the LOS bit in the Global Latch Status register is masked and will not be set by a LOS error.
	6	GMAIS	**AIS Mask:** When set, the AIS bit in the Global Latch Status register is masked and will not be set by an AIS error.
	5	GMOOF	**OOF Mask:** When set, the OOF bit in the Global Latch Status register is masked and will not be set by an OOF error.
	4	GMYEL	**YEL Mask:** When set, the YEL bit in the Global Latch Status register is masked and will not be set by a YEL error.
	3	GMCFA	**CFA Mask:** When set, the CFA bit in the Global Latch Status register is masked and will not be set by a CFA error.
	2	GMSEF	**SEF Mask:** When set, the SEF bit in the Global Latch Status register is masked and will not be set by an SEF event.
	1	GMTXSLIP	**TXSLIP Mask:** When set, the TXSLIP bit in the Global Latch Status register is masked and will not be set by a Transmit Slip event.
	0	GMRXSLIP	**RXSLIP Mask:** When set, the RXSLIP bit in the Global Latch Status register is masked and will not be set by a Receive Slip event.
00C	7-4	R	**Reserved:** Set to zero.
	3-0	CH4-CH1	**Channel Activity:** When set, this bit indicates one or more pending interrupts for the channel from line events only.
00D	7-0		**Spare:**
00E	7-4	R	**Reserved:** Set to zero.
	3-0	CH4-CH1	**Channel Activity:** When set, this bit indicates one or more pending interrupts for the channel from FDL events only.
00F	7-0		**Spare:**

Address	Bit	Symbol	Description
010	7-0	D7-D0	**Command Byte:** This register contains the command byte for the serial port. The definitions of the bits will depend on the external device that is selected. The serial port control logic does not depend on the values in this register for operation. This byte is shifted out LSB first and represents the first byte sent out pin LSDO in Fig. 2.
011	7-0	D7-D0	**Line Interface Serial Data Output:** This register contains the serial data to be written to the selected line interface transceiver. The data is shifted out LSB first and represents the second byte sent out pin LSDO in Fig. 2.
012	7-0	D7-D0	**Line Interface Serial Data Input:** This register contains the read back data from the line interface transceiver when a read operation is performed. The data is shifted in LSB first (see LSDI in Fig. 2).
013	7	BDCST	**Broadcast:** This bit set to one broadcast serial port command and data output registers to all lines. Not used for DS1 monitor mode.
	6	PRBSFR	**PRBS Framed:** When set to one, the internal PRBS generator and analyzer operate in the framed mode. When set to zero, the internal PRBS generator and analyzer operate on all the bits of the transmit and receive data highways. PRBS functions in transmission mode only (not MVIP).
	5	PRBSEN	**PRBS Enable:** When set to one, the internal PRBS analyzer and generator are enabled. Bits 1 and 0 of this register select which framer's receive data highway is connected to the analyzer. The analyzer's output is on pin PRBSOOL. When this bit is set to zero or when the PRBS analyzer is in lock, pin PRBSOOL is low. Only functions in transmission mode.
	4	ESP / EMON	**Enable Serial Port:** When set to one, a single transfer takes place to the selected device (single or broadcast) in serial port mode (CONFIG2 = 0). Toggle to zero before another transfer. **Enable Monitor Port:** When set to one, the NRZ data stream selected by bits 0,1 & 3 are sent to pins MONCLK and MONDTO in DS1 monitor mode (CONFIG2 = 1). When set to zero pins MONCLK and MONDTO are tri-stated.
	3	RXTX	**RX or TX Select:** When set to zero the transmit side is monitored; when set to one the receive side is monitored. Used in DS1 monitor mode only.
	2	R	**Reserved:** Set to zero.
	1-0		**DS1 Channel Numbered (0-3):** When decoded with B0 as least significant bit the value selected (v=0-3) drives the active low chip select, $\overline{LCSn}$, where n=v+1. BDCST causes all $\overline{LCS}$ to be selected in serial port mode. In DS1 monitor mode these bits select the channel to be monitored.
014	7	R	**Reserved:** Set to zero.
	6-0	TLU6-TLU0	**Transmit Loop-Up Code:** These bits are transmitted continuously if TXUP in the Loop Code Control Register is set.
015	7	R	**Reserved:** Set to zero.
	6-0	TLD6-TLD0	**Transmit Loop-Down Code:** These bits are transmitted continuously if TXDN in the Loop Code Control Register is set.

<table>
<tr><th>Address</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td rowspan="5">016</td><td>7-5</td><td>R</td><td>Reserved: Set to zero.</td></tr>
<tr><td>4, 3</td><td>ULEN1-
ULEN0</td><td>Loop-Up Length: This sets the number of significant bits in the Loop-Up Code Register. The bits in the register are right justified.

<table>
<tr><th>ULEN1</th><th>ULEN0</th><th>Length of Code in bits</th></tr>
<tr><td>0</td><td>0</td><td>4</td></tr>
<tr><td>0</td><td>1</td><td>5</td></tr>
<tr><td>1</td><td>0</td><td>6</td></tr>
<tr><td>1</td><td>1</td><td>7</td></tr>
</table></td></tr>
<tr><td>2</td><td>R</td><td>Reserved: Set to zero.</td></tr>
<tr><td>1, 0</td><td>DLEN1-
DLEN0</td><td>Loop-Down Length: This sets the number of significant bits in the Loop-Down Code Register. The bits in the register are right justified.

<table>
<tr><th>DLEN1</th><th>DLEN0</th><th>Length of Code in bits</th></tr>
<tr><td>0</td><td>0</td><td>4</td></tr>
<tr><td>0</td><td>1</td><td>5</td></tr>
<tr><td>1</td><td>0</td><td>6</td></tr>
<tr><td>1</td><td>1</td><td>7</td></tr>
</table></td></tr>
<tr><td>017</td><td>7 - 0</td><td>TSD7 -
TSD0</td><td>Transmit Sync Delay: The value of this register specifies the number of TCLKn clock pulses that TSYNCn is delayed internal to the framer. The default is zero. Each bit of delay makes the coincident TDATAn or SOSGIn bit one earlier with respect to TSYNCn. TSD7 is the MSB.</td></tr>
<tr><td>018</td><td>7 - 0</td><td>RSD7 -
RSD0</td><td>Receive Sync Delay: The value of this register specifies the number of RCLKn clock pulses that RSYNCn is delayed internal to the framer. The default is zero. For RCLKn and RSYNCn as inputs, each bit of delay makes the coincident RDATAn or RSIGLn bit one bit earlier with respect to RSYNCn. For RCLKn and RSYNCn as outputs, each bit of delay makes the coincident RDATAn or SOSIGOn bit one bit later with respect to RSYNCn. RSD7 is the MSB.</td></tr>
</table>

Address	Bit	Symbol	Description
019	7 - 6		**DS1 Channel Numbered (0-3):** When decoded with B6 as least significant bit, the value selected N (0-3) indicates the channel from which the reference clock, CLKREF2, is derived.
	5	ENREF2	**Enable Reference 2:** When set to one, the selected channel (B7 and B6) is output on CLKREF2 pin. When set to zero, CLKREF2 pin is tri-stated. CLKREF2 is also tri-stated if LOS or LINT based on LIF and LPOL indicate a loss of signal on the selected channel.
	4	1544KHZ	**1544 KHz Select:** When set to one the 1544 KHz recovered receive clock (LRCLKn) is output on CLKREF1 and/or CLKREF2. When set to zero, a divide by 193 is inserted between the recovered receive clock and each of CLKREF1 and CLKREF2.
	3	ENREF1	**Enable Reference 1:** When set to one, the selected channel (B0 and B1) is output on CLKREF1 pin. When set to zero, CLKREF1 pin is tri-stated. CLKREF1 is also tri-stated if LOS or LINT based on LIE and LPOL indicate a loss of signal on the selected channel.
	2	R	**Reserved:** Set to zero.
	1, 0		**DS1 Channel numbered (0-3):** When decoded with B0 as least significant bit, the value selected N(0-3) indicates the channel from which the reference clock, CLKREF1 is derived.
020-0FE	7-0		**Spare:**
0FF	7-0		**Reserved:** Set to zero.

PER CHANNEL MEMORY

Framer Configuration

Address	Bit	Symbol	Description
X00	7	MODE	**Dual Unipolar/NRZ Mode Select:** When set to one, the line interface port will operate in dual unipolar mode. When cleared, the line interface port will operate in NRZ mode. B8ZS transcoding is not available in NRZ mode.
	6	BE	**B8ZS Enable:** When set to one in Dual Unipolar mode, the B8ZS transcoder will be enabled. In NRZ mode, this bit determines the TMODE output bit value (e.g. to enable an external B8ZS transcoder) if Fast Sync is not selected.
	5	ENZC	**Enable Excess Zeros Count:** When set to one, this bit will enable the BPV counter to also count excess zeros. When B8ZS transcoding is enabled, 8 or more consecutive zeros is an error. When B8ZS transcoding is disabled, 16 or more consecutive zeros is an error.
	4	ENSYEL	**Enable Signaling Highway Yellow:** When set to one, Yellow alarm from the signaling highway will cause the yellow alarm determined by framing mode and ALT to be propagated to the line. (transmission mode only)
	3	FOD	**Force Ones Density:** When set to one and the QDS1F is in a framed mode with AMI line coding, this bit causes AMI with forced ones density to be enabled in the transcoder. Forced ones density is done on an all zero DS0 (after signaling insertion) by setting bit 7 of the DS0 to one.
	2	ENSAIS	**Enable Signaling Highway AIS:** When set to one, AIS alarm from the signaling highway will cause AIS (all ones) to be propagated to the line. (transmission mode only)
	1	LIE	**LINT Interrupt Enable:** When set to one, the value of LINT is logically ored in with the LOS signal to form the LOS interrupt. LINT in this mode will cause the CLKREF(1, 2) output to tri-state if this framer channel is selected and the value of LINT as determined by LPOL is active.
	0	LPOL	**LINT Polarity Inversion:** When set to one, the value in the register bit LINT will be inverted from the signal at the external input pin LINT.

Address	Bit	Symbol	Description
X01	7	TXCP	**Transmit Clock Polarity:** When set to one, the rising edge of the clock is the active edge. When cleared, the falling edge of the clock is the active edge. Data is shifted out the transmit side of the line interface port on the active edge of the clock.
	6	RXCP	**Receive Clock Polarity:** When set to one, the rising edge of the clock is the active edge. When cleared, the falling edge of the clock is the active edge. Data is sampled on the active edge.
	5	TXNRZP	**Transmit NRZ Data Polarity:** When set to one, the polarity of the transmit data will be inverted at the pin, TLDAT.
	4	PWRD	**Power Down:** When reset, the channel will enter an inactive, low power state in both transmit and receive; FPOL will determine the transmit data.
	3	FDAT	**Force Transmit Data:** When set to one, the transmit data will be forced to the value specified in FPOL. This bit does not affect the receive path, but may be used to conserve power in the transmit path.
	2	FPOL	**Force Transmit Data Polarity:** When set to one, forced transmit data bits will be set to one (transmit AIS). When cleared, forced transmit data bits will be set to zero (used for power reduction on unequipped channels). The forcing function will occur prior to the selected line encoding (AMI, B8ZS, etc.).
	1	BFDL	**Bypass FDL:** When set to one, the FDL "M" bits (D1 bits as shown in figure 11) from the signaling highway (TSIGL) are used in place of the on board HDLC controller. The bit code transmitter is not bypassed. In SF mode this bit when set allows the Fs (see figure 10) bit to be substituted by the signaling highway. (transmission mode only)
	0	RXNRZP	**Receive NRZ Data Polarity:** When set to one, the polarity of the receive data will be inverted at the pin, RLDAT.

<table>
<tr><th>Address</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td>X02</td><td>7-6</td><td>TXC1-TXC0</td><td>Transmit Clock Select: These two bits select the clock used to shift data out of the transmit slip buffer to the line interface port. This is the clock used to multiplex and transmit the T1 data stream.

<table>
<tr><th>TXC1</th><th>TXC0</th><th>Transmit Clock Source</th></tr>
<tr><td>0</td><td>0</td><td>Local Oscillator, LO</td></tr>
<tr><td>0</td><td>1</td><td>Mapper Transmit Clock, TCLK</td></tr>
<tr><td>1</td><td>0</td><td>Recovered Receive Clock, LRCLK</td></tr>
<tr><td>1</td><td>1</td><td>Illegal code</td></tr>
</table></td></tr>
<tr><td></td><td>5</td><td>RXC</td><td>Receive Clock Select: This bit selects the clock used shift data out of the receive slip buffer to the mapper. When set, this bit selects the recovered receive clock (LRCLK). When cleared, this bit selects the clock supplied by the system (RCLK) if RSE is set; see table below. RCLK always used in MVIP mode. When LOS is detected LO is substituted in LRCLK.</td></tr>
<tr><td></td><td>4</td><td>TSE</td><td>Transmit Slip Buffer Enable: When set to one, the transmit slip buffer is enabled. When cleared, the transmit slip buffer is disabled, and data from the system bypasses the slip buffer. This bit only has an effect in transmission mode. Transmit slip buffer is always enabled in MVIP mode.</td></tr>
<tr><td></td><td>3</td><td>RSE</td><td>Receive Slip Buffer Enable: When set to one, the receive slip buffer is enabled. When cleared, the receive slip buffer is disabled, and data from the framer bypasses the slip buffer. This bit only has an effect in transmission mode. The receive slip buffer must always be enabled in MVIP mode.

<table>
<tr><th>RXC</th><th>RSE</th><th>Receive Clock Source</th></tr>
<tr><td>0</td><td>0</td><td>Recovered Receive Clock, LRCLK</td></tr>
<tr><td>0</td><td>1</td><td>System Receive Clock, RCLK</td></tr>
<tr><td>1</td><td>0</td><td>Recovered Receive Clock, LRCLK</td></tr>
<tr><td>1</td><td>1</td><td>Recovered Receive Clock, LRCLK</td></tr>
</table></td></tr>
<tr><td></td><td>2</td><td>TSR</td><td>Transmit Slip Buffer Recenter: When set, this bit will force the transmit slip buffer to recenter once. When cleared, the buffer will recenter automatically to avoid the loss of data (programmed slip).</td></tr>
<tr><td></td><td>1</td><td>RSR</td><td>Receive Slip Buffer Recenter: When set, this bit will force the receive slip buffer to recenter once. When cleared, the buffer will recenter automatically to avoid the loss of data (programmed slip).</td></tr>
<tr><td></td><td>0</td><td>R</td><td>Reserved: Set to zero.</td></tr>
<tr><td>X03</td><td>7-0</td><td></td><td>See Signaling and DS0 Control subsection below.</td></tr>
</table>

<table>
<tr><th>Address</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td rowspan="5">X04</td><td>7-6</td><td>OOF1-
OOF0</td><td>Out of Frame Criteria: The OOF bits determine the out of frame criteria as shown in the table below.

<table>
<tr><th>OOF1</th><th>OOF0</th><th>Out of Frame Criteria</th></tr>
<tr><td>0</td><td>0</td><td>2 out of 4 frame sync bits in error</td></tr>
<tr><td>0</td><td>1</td><td>2 out of 5 frame sync bits in error</td></tr>
<tr><td>1</td><td>0</td><td>2 out of 6 frame sync bits in error</td></tr>
<tr><td>1</td><td>1</td><td>2 out of 4 frame sync bits in error</td></tr>
</table></td></tr>
<tr><td>5</td><td>ALT</td><td>Alternate Yellow Alarm: When set to one, this bit enables Japanese or Bit 12 yellow alarm.</td></tr>
<tr><td>4-3</td><td>SYC1-
SYC0</td><td>Frame Synchronization Bits: The SYC bits determine which framing bits are used for frame synchronization, as shown in the table below. Out Of Frame (OOF) criteria are based on this setting. Severely Errored Frame (SEF) criteria are not affected by these bits.

<table>
<tr><th>SYC1</th><th>SYC0</th><th>D4 SF</th><th>ESF</th></tr>
<tr><td>0</td><td>0</td><td>Not Used</td><td>Not Used</td></tr>
<tr><td>0</td><td>1</td><td>Fs bits</td><td>Fe bits</td></tr>
<tr><td>1</td><td>0</td><td>Ft bits</td><td>Not Used</td></tr>
<tr><td>1</td><td>1</td><td>Fs and Ft bits</td><td>Fe and CRC-6 bits</td></tr>
</table></td></tr>
<tr><td>2-1</td><td>FMD1-
FMD0</td><td>Framing Mode Select: The FMD bits set the mode of the framer, as shown in the table below.

<table>
<tr><th>FMD1</th><th>FMD0</th><th>Mode</th></tr>
<tr><td>0</td><td>0</td><td>Transparent (no framing)</td></tr>
<tr><td>0</td><td>1</td><td>D4SF</td></tr>
<tr><td>1</td><td>0</td><td>Not used</td></tr>
<tr><td>1</td><td>1</td><td>ESF</td></tr>
</table></td></tr>
<tr><td>0</td><td>RSYC</td><td>Resync Control: When set to one, this bit causes the framer to begin a reframe operation. This bit is useful in ESF mode when only Fe bits are used. This bit is useful in SF mode when SLC 96 or alternated SF modes are used and SYCI/SYCO ≠ 11.</td></tr>
<tr><td>X05-X08</td><td>7-0</td><td></td><td>See Miscellaneous subsection below for X05 - X07.
See Facility Data Link subsection below for X08.</td></tr>
</table>

DS1 Status

Address	Bit	Symbol	Description
X09	7	MLOS	**LOS Interrupt Mask:** When set to one, loss of signal interrupt events will be masked from generating interrupts for this channel.
	6	MAIS	**AIS Interrupt Mask:** When set to one, AIS events will be masked from generating interrupts for this channel.
	5	MOOF	**OOF Interrupt Mask:** When set to one, out of frame events will be masked from generating interrupts for this channel.
	4	MYEL	**YEL Interrupt Mask:** When set to one, yellow alarm events will be masked from generating interrupts for this channel.
	3	MCFA	**CFA Interrupt Mask:** When set to one, change of frame alignment events will be masked from generating an interrupt for this channel.
	2	MSEF	**Severely Errored Frame Interrupt Mask:** When set to one, the SEF events will be masked from generating an interrupt for this channel.
	1	MTXSLIP	**Transmit Slip Interrupt Mask:** When set to one, the Transmit Slip events will be masked from generating an interrupt for this channel.
	0	MRXSLIP	**Receive Slip Interrupt Mask:** When set to one, the Receive Slip events will be masked from generating an interrupt for this channel.

Address	Bit	Symbol	Description
X10	7	CLOS	**Current LOS:** This bit reflects the current state of the LOS detector. This bit is a combination of the loss detector in dual unipolar mode (MODE=1) and the LINT pin if enabled (by LIE=1). The LOS detector indicates LOS if 175 ± 75 pulse positions have no transitions. The LOS detector clears the LOS indication if a ones density of 12.5% or more is detected in 175 ± 75 pulse positions.
	6	CAIS	**Current AIS:** This bit reflects the current state of the AIS alarm bit. AIS is detected if 99.9% or more ones are present in a period of 48 ms. AIS is cleared if fewer than 99.9% of ones occur in a period of 48 ms.
	5	COOF	**Current Out of Frame Alignment:** This bit reflects the current state of the out of frame alignment alarm bit. Bits OOF0, OOF1, SYCO and SYCI determine the criteria for COOF.
	4	CYEL	**Current Yellow Alarm:** This bit reflects the current state of the yellow alarm bit. A yellow alarm is detected in one second or less in the presence of line errors occurring at the rate of one error in 1000 or more bits. Detection time is 32 ms for ESF and 335 ms for SF, with no line errors present.
	3	CCFA	**Current Change of Frame Alignment:** This bit reflects the current state of the change of frame alignment alarm bit. This bit is set if a change of frame alignment has occurred in the last 125 µsec. This bit is set only on a re-frame if the bit position for start of multiframe changes.
	2	CSEF	**Current SEF:** This bit reflects the current status of the framer with respect to severely errored frame detection. This bit is set if a SEF has been determined in the last 125 µsec. For SF, SEF is declared if two or more frame bit errors (for Ft only) occur over a 0.75 ms period. For ESF, SEF is declared if two or more frame bit errors occur over a 3.0 ms period. SEF is removed if fewer than two errors occur over the same time periods.
	1	CTXSLIP	**Current TXSLIP:** This bit reflects the current status of the transmit slip buffer with respect to executing slips in the last 125 µsec.
	0	CRXSLIP	**Current RXSLIP:** This bit reflects the current status of the receive slip buffer with respect to executing slips in the last 125 µsec.

Address	Bit	Symbol	Description
X11	7	LLOS	**Latched LOS:** This bit will be set to one when the active edge, as selected by RISE and FALL in the Global Configuration Register, has occurred. If not masked, an interrupt is generated when this bit is set. This bit is cleared by writing a zero to this bit location.
	6	LAIS	**Latched AIS:** This bit will be set to one when the active edge, as selected by RISE and FALL in the Global Configuration Register, has occurred. If not masked, an interrupt is generated when this bit is set. This bit is cleared by writing a zero to this bit location.
	5	LOOF	**Latched Out of Frame Alignment:** This bit will be set to one when the active edge, as selected by RISE and FALL in the Global Configuration Register, has occurred. If not masked, an interrupt is generated when this bit is set. This bit is cleared by writing a zero to this bit location.
	4	LYEL	**Latched Yellow Alarm:** This bit will be set to one when the active edge, as selected by RISE and FALL in the Global Configuration Register, has occurred. If not masked, an interrupt is generated when this bit is set. This bit is cleared by writing a zero to this bit location.
	3	LCFA	**Latched Change of Frame Alignment:** This bit will be set to one when the active edge, as selected by RISE and FALL in the Global Configuration Register, has occurred. If not masked, an interrupt is generated when this bit is set. This bit is cleared by writing a zero to this bit location.
	2	LSEF	**Latched Severely Errored Frame Event:** This bit will be set to one when the active edge, as selected by RISE and FALL in the Global Configuration Register, has occurred. If not masked, an interrupt is generated when this bit is set. This bit is cleared by writing a zero to this bit location.
	1	LTXSLIP	**Latched Transmit Slip Event:** This bit will be set to one when the active edge, as selected by RISE and FALL in the Global Configuration Register, has occurred. If not masked, an interrupt is generated when this bit is set. This bit is cleared by writing a zero to this bit location.
	0	LRXSLIP	**Latched Receive Slip Event:** This bit will be set to one when the active edge, as selected by RISE and FALL in the Global Configuration Register, has occurred. If not masked, an interrupt is generated when this bit is set. This bit is cleared by writing a zero to this bit location.

Address	Bit	Symbol	Description
X12	7	P_LOS	**LOS Error:** This bit is set to one if a LOS error occurred at any time in the last one second interval.
	6	P_AIS	**AIS Error:** This bit is set to one if an AIS error occurred at any time in the last one second interval.
	5	P_OOF	**OOF Error:** This bit is set to one if an OOF error occurred at any time in the last one second interval.
	4	P_YEL	**YEL Error:** This bit is set to one if a YEL error occurred at any time in the last one second interval.
	3	P_CFA	**CFA Error:** This bit is set to one if a CFA error occurred at any time in the last one second interval.
	2	P_SEF	**SEF Error:** This bit is set to one if a SEF error occurred at any time in the last one second interval. This parameter is defined as two frame bits in error out of six.
	1	P_TXSLIP	**TX SLIP Error:** This bit is set to one if a SLIP error occurred at any time in the last one second interval on the transmit slip buffer.
	0	P_RXSLIP	**RX SLIP Error:** This bit is set to one if a SLIP error occurred at any time in the last one second interval on the receive slip buffer.
X13	7	F_LOS	**LOS Error:** This bit is set to one if a LOS error is active but the transition to the active state did not occur in the last one second interval (the event has persisted for longer than one second).
	6	F_AIS	**AIS Error:** This bit is set to one if an AIS error is active but the transition to the active state did not occur in the last one second interval (the event has persisted for longer than one second).
	5	F_OOF	**OOF Error:** This bit is set to one if an OOF error is active but the transition to the active state did not occur in the last one second interval (the event has persisted for longer than one second).
	4	F_YEL	**YEL Error:** This bit is set to one if a YEL error is active but the transition to the active state did not occur in the last one second interval (the event has persisted for longer than one second).
	3	F_CFA	**CFA Error:** This bit is set to one if a CFA error is active but the transition to the active state did not occur in the last one second interval (the event has persisted for longer than one second).
	2	F_SEF	**SEF Error:** This bit is set to one if a SEF error is active but the transition to the active state did not occur in the last one second interval (the event has persisted for longer than one second). This parameter is defined as two frame bits in error out of six.
	1	F_TXSLIP	**TX SLIP Error:** This bit is set to one if a TX SLIP error is active but the transition to the active state did not occur in the last one second interval (the event has persisted for longer than one second).
	0	F_RXSLIP	**RX SLIP Error:** This bit is set to one if a RX SLIP error is active but the transition to the active state did not occur in the last one second interval (the event has persisted for longer than one second).

Address	Bit	Symbol	Description
X14-XEF	7-0		See Miscellaneous subsection below for X14H, X15H and X20H to X3FH. See Facility Data Link subsection below for X16H to X19H and X1AH to X1FH. See Signaling and DS0 Control subsection below for X40H to XEFH.
XF0	7-0	LCRC7-LCRC0	**Latched CRC Error Count Shadow Register:** This 9-bit shadow register (includes bit 0 in address XF1) is updated from the CRC-6 Error Counter (XF2) once a second. The one second interval is derived from the external one second input, T1SI.
XF1	7	LCRCO	**Latched CRC overflow:** This bit is set if the CRC counter overflows. It can be cleared by writing a zero in this register.
	6-3	R	**Reserved:** Set to zero.
	2-1	R	**Reserved:** Set to zero.
	0	LCRC8	**Latched CRC Error Count Shadow Register:** This 9-bit shadow register (includes bits 7-0 in address XF0) is updated from the CRC-6 Error Counter (XF3) once a second. The one second interval is derived from the external one second input, T1SI.
XF2	7-0	CRC7-CRC0	**CRC Error Counter:** This is the lower byte of a 9-bit free running counter which will increment by one for each received CRC error. It can be cleared by writing a zero to the least significant byte of the counter. If ENPMFM is set, this counter's latched value is updated every one second at address XF0.
XF3	7	CRCO	**CRC overflow:** This bit is set if the CRC counter overflows. It can be cleared by writing a zero in this register.
	6-3	R	**Reserved:** Set to zero.
	2-1	R	**Reserved:** Set to zero.
	0	CRC8	**CRC Error Counter:** This is the most significant bit of a 9-bit free running counter which will increment by one for each received CRC error. It can be cleared by writing a zero to this bit of the counter. If ENPMFM is set, this counter's latched value is updated every one second at address XF1.
XF4	7-0	LCV7-LCV0	**Latched Line Code Count Shadow Register:** This is the lower byte of a 16-bit shadow register which is updated from the Line Code Error Counter once a second. The one second interval is derived from the external one second input, T1SI.
XF5	7-0	LCV15-LCV8	**Latched Line Code Count Shadow Register:** This is the upper byte of a 16-bit shadow register which is updated from the Line Code Error Counter once a second. The one second interval is derived from the external one second input, T1SI.
XF6	7	LBPVO	**Latched BPV Counter Overflow:** When set, the Line Code Error Counter has overflowed. This bit may be cleared by writing a zero in this register.
	6-0	R	**Reserved:** Set to zero.

Address	Bit	Symbol	Description
XF7	7-0	CV7-CV0	**Line Code Error Counter:** This is the lower byte of a 16 bit free running counter which will increment by one for each received line code violation. If excessive zeros counting is enabled they will also be counted with the line code errors. This counter can be cleared by writing its value to zero. If the counter overflows the BPV bit in location XF9 will be set. If ENP-MFM is set, this counter's latched value is updated every one second at address XF4.
XF8	7-0	CV15-CV8	**Line Code Error Counter:** This is the upper byte of a 16 bit free running counter which will increment by one for each received line code violation. If excessive zeros counting is enabled they will also be counted with the code errors. This counter can be cleared by writing its value to zero. If the counter overflows the BPV bit in location XF9 will be set. If ENPMFM is set, this counter's latched value is updated every one second at address XF5.
XF9	7	BPVO	**BPV Counter Overflow:** When set, the Line Code Error Counter has overflowed. This bit may be cleared by writing a zero in this register.
	6-0	R	**Reserved:** Set to zero.
XFA	7-0	LFBE7-LFBE0	**Latched Frame Bit Error Count Shadow Register:** This 8-bit shadow register is updated from the Frame Bit Error Counter once a second. The one second interval is derived from the external one second input, T1SI.
XFB	7	LFBOF	**Latched Frame Bit Overflow:** This bit is set to one if the frame bit error counter overflows. It is updated from the Frame Bit Overflow once a second. The one second interval is derived from the external one second input, T1SI.
	6-0	R	**Reserved:** Set to zero.
XFC	7-0	FBE7-FBE0	**Frame Bit Error Counter:** This 8 bit free running counter will increment by one for each received frame bit in error. It can be cleared by writing a zero to the counter. If ENPMFM is set, this counter's latched value is updated every one second at address XFA.
XFD	7	FBOF	**Frame Bit Overflow:** This bit is set to one if the frame bit error counter overflows. It can be cleared by writing a zero to this register.If ENPMFM is set, this counter's latched value is updated every one second at address XFB.
	6-0	R	**Reserved:** Set to zero.
XFE-XFF	7-0	R	**Reserved:** Set to zero.

Signaling and DS0 Control

<table>
<tr><th>Address</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td>X03</td><td>7-6</td><td>TYP1-TYP0</td><td>Signaling Type: These two bits select the signaling type for both the transmit and receive directions, as shown in the table below.
<table>
<tr><th>TYP1</th><th>TYP0</th><th>Type</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>None</td><td>Clear channel mode, no signaling</td></tr>
<tr><td>0</td><td>1</td><td>2-state</td><td>A bits in frames 6,12,18, and 24</td></tr>
<tr><td>1</td><td>0</td><td>4-state</td><td>A bits in frames 6 and 18
B bits in frames 12 and 24</td></tr>
<tr><td>1</td><td>1</td><td>16-state</td><td>A bits in frame 6
B bits in frame 12
C bits in frame 18
D bits in frame 24</td></tr>
</table></td></tr>
<tr><td></td><td>5</td><td>RXF</td><td>Receive Signaling Freeze: When set to one, received signaling bits from the DS1 line will not be written into the signaling buffer. The current contents of the signaling buffer will be used for the receive data path to the system.</td></tr>
<tr><td></td><td>4</td><td>TXF</td><td>Transmit Signaling Freeze: When set to one, transmit signaling bits from the system will not be written into the signaling buffer. The current contents of the signaling buffer will be used for the transmit data path to the DS1 line interface port.</td></tr>
<tr><td></td><td>3</td><td>OSE</td><td>Ones Stuffing Enable: When set to one, the signaling bit position in the receive path will be forced to a one after the signaling has been extracted. If cleared, the signaling bits remain in the DS0 unchanged.</td></tr>
<tr><td></td><td>2</td><td>ENAIS</td><td>Enable AIS: When set to one, line AIS detected is sent to the AIS bit on the signaling highway in transmission mode only. It also controls SYSVTAIS.</td></tr>
<tr><td></td><td>1</td><td>ENOOF</td><td>Enable OOF: When set to one, OOF detected is sent to the AIS bit on the signaling highway in transmission mode only. It also controls SYSVTAIS.</td></tr>
<tr><td></td><td>0</td><td>ENLOS</td><td>Enable LOS: When set to one, LOS/LOC detected is sent to the AIS bit on the signaling highway in transmission mode only. It also controls SYSVTAIS.</td></tr>
<tr><td>X40-X57/
X58-X6F</td><td>7-0</td><td>RDS0(1) -
RDS0(24)</td><td>Receive DS0n: These bytes appear at two locations representing their respective locations in the two frame slip buffers. When the received DS0 is enabled (RDE1-RDE24 @XE0 - XE2), the DS0 is written to this buffer from the received line. Whether enabled or not, the stored DS0 is always read out on the system side. Microprocessor access allows observing received DS0s from the DS1 line as well as sending idle patterns or out of service codes to the system side. Both locations must be written to send a continuous pattern.</td></tr>
<tr><td>X70-X7F</td><td>7-0</td><td></td><td>Reserved: Set to zero.</td></tr>
</table>

Address	Bit	Symbol	Description
X80	7-0	A8-A1	**Receive Signaling Bits:** Bits A1 - A8 are the most recently received signaling bits from the DS1 line.
X81	7-0	A16-A9	**Receive Signaling Bits:** Bits A9 - A16 are the most recently received signaling bits from the DS1 line.
X82	7-0	A24-A17	**Receive Signaling Bits:** Bits A17 - A24 are the most recently received signaling bits from the DS1 line.
X83	7-0		**Reserved:** Set to zero.
X84	7-0	B8-B1	**Receive Signaling Bits:** Bits B1 - B8 are the most recently received signaling bits from the DS1 line.
X85	7-0	B16-B9	**Receive Signaling Bits:** Bits B9 - B16 are the most recently received signaling bits from the DS1 line.
X86	7-0	B24-B17	**Receive Signaling Bits:** Bits B17 - B24 are the most recently received signaling bits from the DS1 line.
X87	7-0		**Reserved:** Set to zero.
X88	7-0	C8-C1	**Receive Signaling Bits:** Bits C1 - C8 are the most recently received signaling bits from the DS1 line.
X89	7-0	C16-C9	**Receive Signaling Bits:** Bits C9 - C16 are the most recently received signaling bits from the DS1 line.
X8A	7-0	C24-C17	**Receive Signaling Bits:** Bits C17 - C24 are the most recently received signaling bits from the DS1 line
X8B	7-0		**Reserved:** Set to zero.
X8C	7-0	D8-D1	**Receive Signaling Bits:** Bits D1 - D8 are the most recently received signaling bits from the DS1 line.
X8D	7-0	D16-D9	**Receive Signaling Bits:** Bits D1 - D16 are the most recently received signaling bits from the DS1 line.
X8E	7-0	D24-D17	**Receive Signaling Bits:** Bits D1 - D24 are the most recently received signaling bits from the DS1 line.
X8F	7-0		**Reserved:** Set to zero.
X90-XA7/ XA8-XBF	7-0	TDS0(1) - TDS0(24)	**Transmit DS0n:** These bytes appear at two locations representing their respective locations in the two frame slip buffers. When the transmit DS0 is enabled (TDE1-TDE24 @ XE4 - XE6), the DS0 is written to this buffer from the system side. Whether enabled or not, the stored DS0 is always read out to the DS1 line. Microprocessor access allows observing DS0s from the system side as well as sending idle or out of service patterns to the DS1 line. Both locations must be written to send a continuous pattern.
XC0-XCF	7-0		**Reserved:** Set to zero.
XD0	7-0	A8-A1	**Transmit Signaling Bits:** Bits A1 - A8 are the most recently received signaling bits from the system interface.
XD1	7-0	A16-A9	**Transmit Signaling Bits:** Bits A9 - A16 are the most recently received signaling bits from the system interface.

Address	Bit	Symbol	Description
XD2	7-0	A24-A17	**Transmit Signaling Bits:** Bits A17 - A24 are the most recently received signaling bits from the system interface.
XD3	7-0		**Reserved:** Set to zero.
XD4	7-0	B8-B1	**Transmit Signaling Bits:** Bits B1 - B8 are the most recently received signaling bits from the system interface.
XD5	7-0	B16-B9	**Transmit Signaling Bits:** Bits B9 - B16 are the most recently received signaling bits from the system interface.
XD6	7-0	B24-B17	**Transmit Signaling Bits:** Bits B17 - B24 are the most recently received signaling bits from the system interface.
XD7	7-0		**Reserved:** Set to zero.
XD8	7-0	C8-C1	**Transmit Signaling Bits:** Bits C1 -C8 are the most recently received signaling bits from the system interface.
XD9	7-0	C16-C9	**Transmit Signaling Bits:** Bits C9 -C16 are the most recently received signaling bits from the system interface.
XDA	7-0	C24-C17	**Transmit Signaling Bits:** Bits C17 - C24 are the most recently received signaling bits from the system interface.
XDB	7-0		**Reserved:** Set to zero.
XDC	7-0	D8-D1	**Transmit Signaling Bits:** Bits D1 - D8 are the most recently received signaling bits from the system interface.
XDD	7-0	D16-D9	**Transmit Signaling Bits:** Bits D9 - D16 are the most recently received signaling bits from the system interface.
XDE	7-0	D24-D17	**Transmit Signaling Bits:** Bits D17 - D24 are the most recently received signaling bits from the system interface.
XDF	7-0		**Reserved:** Set to zero.
XE0	7-0	RDE8-RDE1	**Receive DS0 Enable for DS0 Channels 1-8:** When set to one, the DS0 received from the DS1 line will be sent to the system interface for the selected DS0. When cleared the DS0 sent to the system interface will be the last value in the Receive Slip Buffer; this value is writable by the microprocessor allowing idle or other codes to be inserted on a per DS0 basis by the microprocessor. Signaling enable is independent of these bits.
XE1	7-0	RDE16-RDE9	**Receive DS0 Enable for DS0 Channels 9-16:** When set to one, the DS0 received from the DS1 line will be sent to the system interface for the selected DS0. When cleared the DS0 sent to the system interface will be the last value in the Receive Slip Buffer; this value is writable by the microprocessor allowing idle or other codes to be inserted on a per DS0 basis by the microprocessor. Signaling enable is independent of these bits.

Address	Bit	Symbol	Description
XE2	7-0	RDE24-RDE17	**Receive DS0 Enable for DS0 Channels 17-24:** When set to one, the DS0 received from the DS1 line will be sent to the system interface for the selected DS0. When cleared the DS0 sent to the system interface will be the last value in the Receive Slip Buffer; this value is writable by the microprocessor allowing idle or other codes to be inserted on a per DS0 basis by the microprocessor. Signaling enable is independent of these bits.
XE3	7-0		**Reserved:** Set to zero.
XE4	7-0	TDE8-TDE1	**Transmit DS0 Enable for DS0 Channels 1-8:** When set to one, the DS0 received by the system side will be transmitted on the DS1 line for the selected DS0. When cleared the DS0 transmitted will be the last value in the Transmit Slip Buffer; this value is writable by the microprocessor allowing idle or other codes to be inserted on a per DS0 basis by the microprocessor. Signaling enable is independent of these bits.
XE5	7-0	TDE16-TDE9	**Transmit DS0 Enable for DS0 Channels 9-16:** When set to one, the DS0 received by the system side will be transmitted on the DS1 line for the selected DS0. When cleared the DS0 transmitted will be the last value in the Transmit Slip Buffer; this value is writable by the microprocessor allowing idle or other codes to be inserted on a per DS0 basis by the microprocessor. Signaling enable is independent of these bits.
XE6	7-0	TDE24-TDE17	**Transmit DS0 Enable for DS0 Channels 17-24:** When set to one, the DS0 received by the system side will be transmitted on the DS1 line for the selected DS0. When cleared the DS0 transmitted will be the last value in the Transmit Slip Buffer; this value is writable by the microprocessor allowing idle or other codes to be inserted on a per DS0 basis by the microprocessor. Signaling enable is independent of these bits.
XE7	7-0		**Reserved:** Set to zero.
XE8	7-0	SE8-SE1	**Signaling Enable for DS0 Channels 1-8:** When set to one, robbed bit signaling will be enabled for the individual DS0 channel. Bits will be inserted into the transmit data stream and extracted from the receive data stream. When cleared, bits are not inserted in the transmit data stream and a zero is written into the receive signaling buffer instead of an extracted signaling bit.
XE9	7-0	SE16-SE9	**Signaling Enable for DS0 Channels 9-16:** When set to one, robbed bit signaling will be enabled for the individual DS0 channel. Bits will be inserted into the transmit data stream and extracted from the receive data stream. When cleared, bits are not inserted in the transmit data stream and a zero is written into the receive signaling buffer instead of an extracted signaling bit.
XEA	7-0	SE24-SE17	**Signaling Enable for DS0 Channels 17-24:** When set to one, robbed bit signaling will be enabled for the individual DS0 channel. Bits will be inserted into the transmit data stream and extracted from the receive data stream. When cleared, bits are not inserted in the transmit data stream and a zero is written into the receive signaling buffer instead of an extracted signaling bit.
XEB-XEF	7-0		**Reserved:** Set to zero.

Facility Data Link

Address	Bit	Symbol	Description
X08	7	EHR	**Enable HDLC Receiver:** When set to one, the HDLC receiver is enabled. When valid characters are received, they are placed into the receive FIFO and receive HDLC interrupts are enabled. When cleared, the FIFO is cleared and HDLC receive interrupts are disabled.
	6	EHT	**Enable HDLC Transmitter:** When set to one, the HDLC transmitter is enabled and transmit HDLC interrupts are enabled. Once enabled the HDLC transmitter will send flags continuously when the FIFO is empty. When the transmit FIFO has characters in it, they are sent and transmit HDLC interrupts are enabled. When cleared, the FIFO is cleared and HDLC transmit interrupts are disabled.
	5	TAB	**Transmit Abort:** When set to one, the HDLC transmitter will send a 7FH to signal an abort after the current character, clear the FIFO and follow with continuous flags.
	4	EOM	**Transmitter End of Message Flag:** When set to one, the transmitter FIFO contains the last byte of the message. When the FIFO is emptied, CRC will be sent followed by an interrupt.
	3	RHIE	**Receiver Half Full Interrupt Enable:** When set to one, the receiver will generate an interrupt when its FIFO is half full or at the end of a message. When cleared, the receiver will generate an interrupt only at the end of a message or FIFO overflow.
	2	THIE	**Transmitter Half Full Interrupt Enable:** When set to one, the transmitter will generate an interrupt when its FIFO is half empty or at the end of a message. When cleared, the transmitter will generate an interrupt only at the end of a message or FIFO underflow.
	1	EBRI	**Enable Bit Code Receiver Interrupt:** When set to one, the bit code receiver interrupt is enabled.
	0	EBT	**Enable Bit Code Transmitter:** When set to one, the bit code transmitter is enabled and will immediately start sending the two byte bit code defined by the transmit bit code register. The transmitter does not generate an interrupt.
X0A	7-0	D7-D0	**HDLC Transmit Data:** This is the write port of the HDLC transmit FIFO.
X0B	7-6	R	**Reserved:** Set to zero.
	5-0	D5-D0	**Transmit Bit Code Data:** These six bits will be formatted into a valid 16 bit message and transmitted continuously.
X0C	7-0		**Spare:**
X0D	7-0		**Spare:**

Address	Bit	Symbol	Description
X0E	7-5	ERHIS2-ERHIS0	**Receive HDLC Interrupt Event:** These bits will be set when the active edge, as selected by RISE and FALL in the Global Configuration Register, has occurred. If not masked, an interrupt is generated when these bits are set. These bits are cleared by writing a zero to these bit locations. When non zero, the receive HDLC channel requires service for the reasons listed for RHIS2-RHIS0.
	4	ETHIS	**Transmit HDLC Interrupt Event:** This bit will be set when the active edge, as selected by RISE and FALL in the Global Configuration Register, has occurred. If not masked, an interrupt is generated when this bit is set. This bit is cleared by writing a zero to this bit location. When non zero, the transmit HDLC channel requires service for the reasons listed for THIS.
	3-2	ERXFS1-ERXFS0	**Receive FIFO Event:** These bits will be set when the active edge, as selected by RISE and FALL in the Global Configuration Register, has occurred. If not masked, an interrupt in generated when these bits are set. These bits are cleared by writing a zero to these bit locations. When non zero, the receive FIFO requires service for the reasons listed for RXFS1-RXFS0.
	1-0	ETXFS1-ETXFS0	**Transmit FIFO Event:** These bits will be set when the active edge, as selected by RISE and FALL in the Global Configuration Register, has occurred. If not masked, an interrupt in generated when these bits are set. These bits are cleared by writing a zero to these bit locations. When non zero, the transmit FIFO requires service for the reasons listed for RXFS1-RXFS0.
X0F	7-5	MRHIS2-MRHIS0	**Receive HDLC Interrupt Mask:** When set to one, receive HDLC events corresponding to the bit(s) set will be masked from generating interrupts (see the definition of these bits in the table for RHIS2-RHIS0).
	4	MTHIS	**Transmit HDLC Interrupt Mask:** When set to one, transmit HDLC events will be masked from generating interrupts.
	3-2	MRXFS1-MRXFS0	**Receive FIFO Interrupt Mask:** When set to one, receive FIFO events corresponding to the bit(s) set will be masked from generating interrupts (see the definition of these bits in the table for RXFS1-RXFS0).
	1-0	MTXFS1-MTXFS0	**Transmit FIFO Interrupt Mask:** When set to one, transmit FIFO events corresponding to the bit(s) set will be masked from generating interrupts (see the definition of these bits in the table for TXFS1-TXFS0).
X10-X15	7-0		See DS1 Status subsection above for X10H to X13H. See Miscellaneous subsection below for X14H and X15H.

<table>
<tr><th>Address</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td>X16</td><td>7-5</td><td>RHIS2-
RHIS0</td><td>Receive HDLC Interrupt Status: When non-zero, the receive HDLC channel requires service for the reasons listed below:
<table>
<tr><th>RHIS2</th><th>RHIS1</th><th>RHIS0</th><th>Condition</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Idle</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Message in progress</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Valid message received or FIFO needs service</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Message received with CRC error or "zero length" message</td></tr>
<tr><td>1</td><td>0</td><td>X</td><td>Message aborted</td></tr>
<tr><td>1</td><td>1</td><td>X</td><td>Bit code received (RX FIFO automatically cleared)</td></tr>
</table></td></tr>
<tr><td></td><td>4</td><td>THIS</td><td>Transmit HDLC Interrupt Status: When set, the transmit HDLC channel requires service (message complete or FIFO half empty).</td></tr>
<tr><td></td><td>3-2</td><td>RXFS1-
RXFS0</td><td>Receive FIFO Status: The following conditions indicate the status of the receive FIFO:
<table>
<tr><th>RXFS1</th><th>RXFS0</th><th>Receive FIFO Condition</th></tr>
<tr><td>0</td><td>0</td><td>Normal (less than half full)</td></tr>
<tr><td>0</td><td>1</td><td>Half or more than half full</td></tr>
<tr><td>1</td><td>0</td><td>FIFO full</td></tr>
<tr><td>1</td><td>1</td><td>FIFO overflowed (attempt to overwrite last character)</td></tr>
</table></td></tr>
<tr><td></td><td>1-0</td><td>TXFS1-
TXFS0</td><td>Transmit FIFO Status: The following conditions indicate the status of the transmit FIFO:
<table>
<tr><th>TXFS1</th><th>TXFS0</th><th>Transmit FIFO Condition</th></tr>
<tr><td>0</td><td>0</td><td>Normal (more than half full)</td></tr>
<tr><td>0</td><td>1</td><td>Less than half full</td></tr>
<tr><td>1</td><td>0</td><td>FIFO overwritten (attempt to write to full FIFO)</td></tr>
<tr><td>1</td><td>1</td><td>FIFO underflowed (attempt to read empty FIFO)</td></tr>
</table></td></tr>
<tr><td>X17</td><td>7-0</td><td>D7-D0</td><td>HDLC Receive Data: This is the read port of the HDLC receive FIFO.</td></tr>
</table>

Address	Bit	Symbol	Description
X18	7-5	R	**Reserved:** Set to zero.
	4-0	C4-C0	**HDLC Receive FIFO Depth:** This register contains the number of bytes in the receive FIFO.
X19	7-6	R	**Reserved:** Set to zero.
	5-0	D5-D0	**Receive Bit Code Data:** When a valid bit code has been received 8 out of 10 times, these bits will be set to that pattern. If no valid code is detected, these six bits will be set to all ones.
X1A-X1F	7-0		**Spare:**

Miscellaneous

Address	Bit	Symbol	Description
X05	7	SRST	**Software Reset:** When set to one, the framer is initialized and held in its reset state.
	6	ALUP	**Automatic Loop back:** When set to one, a remote line loop back is automatically entered when a loop-up condition is detected, and automatically cleared when a loop-down condition is detected. This action is taken after the loop-up or loop-down code has been received for 5 seconds. ENP-MFM must also be set to one for this function to operate.
	5	TXUP	**Transmit Loop-Up Code Enable:** When set to one, the loop-up code is sent continuously on the DS1 line.
	4	TXDN	**Transmit Loop-Down Code Enable:** When set to one, the loop-down code is sent continuously on the DS1 line.
	3	PAYL	**Payload Loop Back Enable:** When set to one, a payload loop back will be enabled.
	2	TX1S	**Transmit Ones:** When set to one, the transmitter will transmit all ones instead of data during a local loop back.
	1	RLP	**Remote Line Loop back Enable:** When set to one, a remote line loop back will be enabled. The TXCP and RXCP bit values must be unequal for RLP to function correctly.
	0	LLP	**Local Loop back Enable:** When set to one, a local loop back will be enabled. **NOTE: If both RLP and LLP are set, a bidirectional loop back is enabled and TX1S is ignored.

Address	Bit	Symbol	Description
X06	7-4	R	**Reserved:** Set to zero.
	3	INSPRBS	**Insert PRBS:** When set to one, PRBS is substituted for the data received on the transmit data highway. This only functions in transmission mode.
	2	SFZ	**System Freeze:** When set to one, the output clocks (LTCLK and RCLK) go to zero and the input clocks (LRCLK and TCLK) are gated off.
	1	RXFS	**Receive Fast Sync:** When set to one and the QDS1F channel is in NRZ mode, a pulse received on RNEG will force sync being interpreted as bit position 193 of the last frame of a superframe.
	0	TXFS	**Transmit Fast Sync:** When set to one and the QDS1F channel is in NRZ mode, a synchronization pulse is sent every three milliseconds on TNEG corresponding to bit position 193 of frame 24 for ESF or of every other frame 12 for SF.
X07	7	R	**Reserved:** Set to zero.
	6	SYSVTAIS	**System VTAIS:** When set to one, any condition that causes the AIS bit to be set on the signaling highway (see ENOOF, ENLOS & ENAIS) will cause all ones to be placed on the data highway toward the system in transmission mode. In MVIP this function also works if any of ENOOF, ENLOS or ENAIS is set and the condition (OOF, LOS or AIS) is present.
	5	SYSALL1	**System All Ones:** When set to one, all ones are place on the data highway toward the system.
	4	CRC	**Generate CRC Errors:** When set to one, the CRC bits are inverted, generating 6 CRC bit errors. This will cause only 1 bad frame to be generated to the line.
	3	FRME	**Generate Frame Error:** When set to one, the framer will transmit one bad frame bit to the line. The bit to be errored will depend on which bits are being used for frame synchronization (Fs, Ft, or Fe).
	2	YEL	**Generate Yellow Alarm:** When set to one, a yellow alarm is generated in the selected mode (SF, Japanese SF or ESF) until cleared.
	1	AIS	**Send AIS:** When set to one, the framer transmits AIS to the line until this bit is cleared.
	0	BPV	**Generate BPV:** When set to one, the framer will send a single code error. A code error is a single BPV. Excess zero code errors can not be forced.

<table>
<tr><th>Address</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td rowspan="5">X14</td><td>7-6</td><td>TXS1-TXS0</td><td>Transmit Slip Buffer Status: These bits indicate the direction of transmit slips, as shown in the table below:
<table>
<tr><th>TXS1</th><th>TXS0</th><th>Transmit Slip Buffer Status</th></tr>
<tr><td>0</td><td>0</td><td>No slips</td></tr>
<tr><td>0</td><td>1</td><td>Slip overflow - drop one frame</td></tr>
<tr><td>1</td><td>0</td><td>Slip underflow - repeat one frame</td></tr>
<tr><td>1</td><td>1</td><td>Slip buffer error - two slips in a row</td></tr>
</table></td></tr>
<tr><td>5-4</td><td>RXS1-RXS0</td><td>Receive Slip Buffer Status: These bits indicate the direction of receive slips, as shown in the table below.
<table>
<tr><th>RXS1</th><th>RXS0</th><th>Receive Slip Buffer Status</th></tr>
<tr><td>0</td><td>0</td><td>No slips</td></tr>
<tr><td>0</td><td>1</td><td>Slip overflow - drop one frame</td></tr>
<tr><td>1</td><td>0</td><td>Slip underflow - repeat one frame</td></tr>
<tr><td>1</td><td>1</td><td>Slip buffer error - two slips in a row</td></tr>
</table></td></tr>
<tr><td>3</td><td>VTAIS</td><td>VT AIS Received: When set, VT AIS is being received on the signaling highway, TSIGL. (Transmission mode only)</td></tr>
<tr><td>2</td><td>VTRDI</td><td>VT RDI (Yellow) Received: When set, VT RDI is being received on the signaling highway, TSIGL. (Transmission mode only)</td></tr>
<tr><td>1-0</td><td>R</td><td>Reserved: Set to zero.</td></tr>
</table>

Address	Bit	Symbol	Description
X15	7	RXSF	**Receive Signaling Freeze:** When set, this status bit indicates that receive signaling has been frozen as a result of either a loss of the receive line as indicated by LOS/OOF (automatic freeze) or a manual request to freeze receive signaling (RXF bit set @ location X03).
	6	TXSF	**Transmit Signaling Freeze:** When set, this status bit indicates that transmit signaling has been frozen as a result of either receiving system AIS on the signaling highway (automatic freeze in transmission mode only) or a manual request to freeze transmit signaling (TXF bit set @ location X03).
	5-3	R	**Reserved:** Set to zero.
	2	UP	**Receive Loop Code Status:** When set, indicates a loop-up code has been detected. After loop-up is received for 5 seconds the remote line loop back is entered.
	1	DOWN	**Receive Loop Code Status:** When set after a loop-up code has been detected, indicates a loop-down code has been detected. After loop-down is received for 5 seconds the remote line loop back is cleared. If no loop codes have been received, this bit is set to one as an initial condition. When a loop-up code is received the UP bit is set and this bit is cleared.
	0	LINT	**General Purpose Input:** This bit reflects the external input pin, LINT. The polarity of this bit may be modified by LPOL or included with LOS by LIE at location X00. This bit also controls the CLKREF(1, 2) output if LIE is set.
X20	7-0	TWP7 - TWP0	**Transmit Slip Buffer Write Pointer:** These bits give the current value of the transmit slip buffer write pointer; 0 - 192.
X21	7-0	TRP7 - TRP0	**Transmit Slip Buffer Read Pointer:** These bits give the current value of the transmit slip buffer read pointer; 0 - 192.
X22	7	TWSBS	**Transmit Write Slip Buffer Side:** This bit indicates upper (1) or lower (0) side of the transmit slip buffer currently being written.
	6, 5	R	**Reserved:** Set to zero.
	4-0	TWPF4 - TWPF0	**Transmit Slip Buffer Write Pointer Frame:** These bits indicates which SF (0-11) or ESF (0-23) frame is being written.
X23	7	TRSBS	**Transmit Read Slip Buffer Side:** This bit indicates upper (1) or lower (0) side of the transmit slip buffer currently being read.
	6, 5	R	**Reserved:** Set to zero.
	4-0	TRPF4 - TRPF0	**Transmit Slip Buffer Read Pointer Frame:** These bits indicates which SF (0-11) or ESF (0-23) frame is being read.
X24	7-0	RWP7- RWP0	**Receive Slip Buffer Write Pointer:** These bits give the current value of the receive slip buffer write pointer; 0 - 192.
X25	7-0	RRP7 - RRP0	**Receive Slip Buffer Read Pointer:** These bits give the current value of the receive slip buffer read pointer; 0 - 192.

Address	Bit	Symbol	Description
X26	7	RWSBS	**Receive Write Slip Buffer Side:** This bit indicates upper (1) or lower (0) side of the transmit slip buffer currently being written.
	6, 5	R	**Reserved:** Set to zero.
	4-0	RWPF4 - RWPF0	**Receive Slip Buffer Write Pointer Frame:** These bits indicates which SF (0-11) or ESF (0-23) frame is being written.
X27	7	RRSBS	**Receive Read Slip Buffer Side:** This bit indicates upper (1) or lower (0) side of the receive slip buffer currently being read.
	6, 5	R	**Reserved:** Set to zero.
	4-0	RRPF4 - RRPF0	**Receive Slip Buffer Read Pointer Frame:** These bits indicates which SF (0-11) or ESF (0-23) frame is being read.
X28-X2F	7-0		**Spare:**
X30, X33	7	Fe2/Fs4	**Receive Frame Bit FIFO Frame bits:** Bit Fe2 in ESF; bit Fs4 in SF.
	6	D1/Ft4	**Receive Frame Bit FIFO Frame bits:** FDL bit ESF; bit Ft4 in SF.
	5	CRC2/Fs3	**Receive Frame Bit FIFO Frame bits:** CRC bit 2 in ESF; bit Fs3 in SF.
	4	D1/Ft3	**Receive Frame Bit FIFO Frame bits:** FDL bit in ESF; bit Ft3 in SF.
	3	Fe1/Fs2	**Receive Frame Bit FIFO Frame bits:** Bit Fe1 in ESF; bit Fs2 in SF.
	2	D1/Ft2	**Receive Frame Bit FIFO Frame bits:** FDL bit in ESF; bit Ft2 in SF.
	1	CRC1/Fs1	**Receive Frame Bit FIFO Frame bits:** CRC bit 1 in ESF; bit Fs1 in SF.
	0	D1/Ft1	**Receive Frame Bit FIFO Frame bits:** FDL bit in ESF; bit Ft1 in SF.
X31, X34	7	Fe4/X	**Receive Frame Bit FIFO Frame bits:** Bit Fe4 in ESF; don't care in SF.
	6	D1/X	**Receive Frame Bit FIFO Frame bits:** FDL bit ESF; don't care in SF.
	5	CRC4/X	**Receive Frame Bit FIFO Frame bits:** CRC bit 4 in ESF; don't care in SF.
	4	D1/X	**Receive Frame Bit FIFO Frame bits:** FDL bit in ESF; don't care in SF.
	3	Fe3/Fs6	**Receive Frame Bit FIFO Frame bits:** Bit Fe3 in ESF; bit Fs6 in SF.
	2	D1/Ft6	**Receive Frame Bit FIFO Frame bits:** FDL bit in ESF; bit Ft6 in SF.
	1	CRC3/Fs5	**Receive Frame Bit FIFO Frame bits:** CRC bit 3 in ESF; bit Fs5 in SF.
	0	D1/Ft5	**Receive Frame Bit FIFO Frame bits:** FDL bit in ESF; bit Ft5 in SF.
X32, X35	7	Fe6/X	**Receive Frame Bit FIFO Frame bits:** Bit Fe6 in ESF; don't care in SF.
	6	D1/X	**Receive Frame Bit FIFO Frame bits:** FDL bit ESF; don't care in SF.
	5	CRC6/X	**Receive Frame Bit FIFO Frame bits:** CRC bit 6 in ESF; don't care in SF.
	4	D1/X	**Receive Frame Bit FIFO Frame bits:** FDL bit in ESF; don't care in SF.
	3	Fe5/X	**Receive Frame Bit FIFO Frame bits:** Bit Fe5 in ESF; don't care in SF.
	2	D1/X	**Receive Frame Bit FIFO Frame bits:** FDL bit in ESF; don't care in SF.
	1	CRC5/X	**Receive Frame Bit FIFO Frame bits:** CRC bit 5 in ESF; don't care in SF.
	0	D1/X	**Receive Frame Bit FIFO Frame bits:** FDL bit in ESF; don't care in SF.

Address	Bit	Symbol	Description
X36-37	7-0		**Reserved:** Set to zero.
X38	7-0	LBCC7 - LBCC0	**Loopback Code Counter:** This is the lower byte of a 16 bit counter that contains the count of valid loop-up or loop-down codes received during the current one second divided by 8. A match is to the TLU6/0 or TLD6 /0 bits per the length (ULEN1/0, DLEN1/0) depending on the state of the channel.
X39	7-0	LBCC15 - LBCC8	**Loopback Code Counter:** This is the upper byte of a 16 bit counter that contains the count of valid loop-up or loop-down codes received during the current one second divided by 8. A match is to the TLU6/0 or TLD6/0 bits per the length (ULEN1/0, DLEN1/0) depending on the state of the channel.
X3A-3F	7-0		**Reserved:** Set to zero.

APPLICATION DIAGRAM

The diagram in Figure 29 illustrates the use of the QDS1F device to provide framing and DS0 access for a variety of DS1 sources. Direct control of most commercial line interface unit devices (LIUs) is provided.

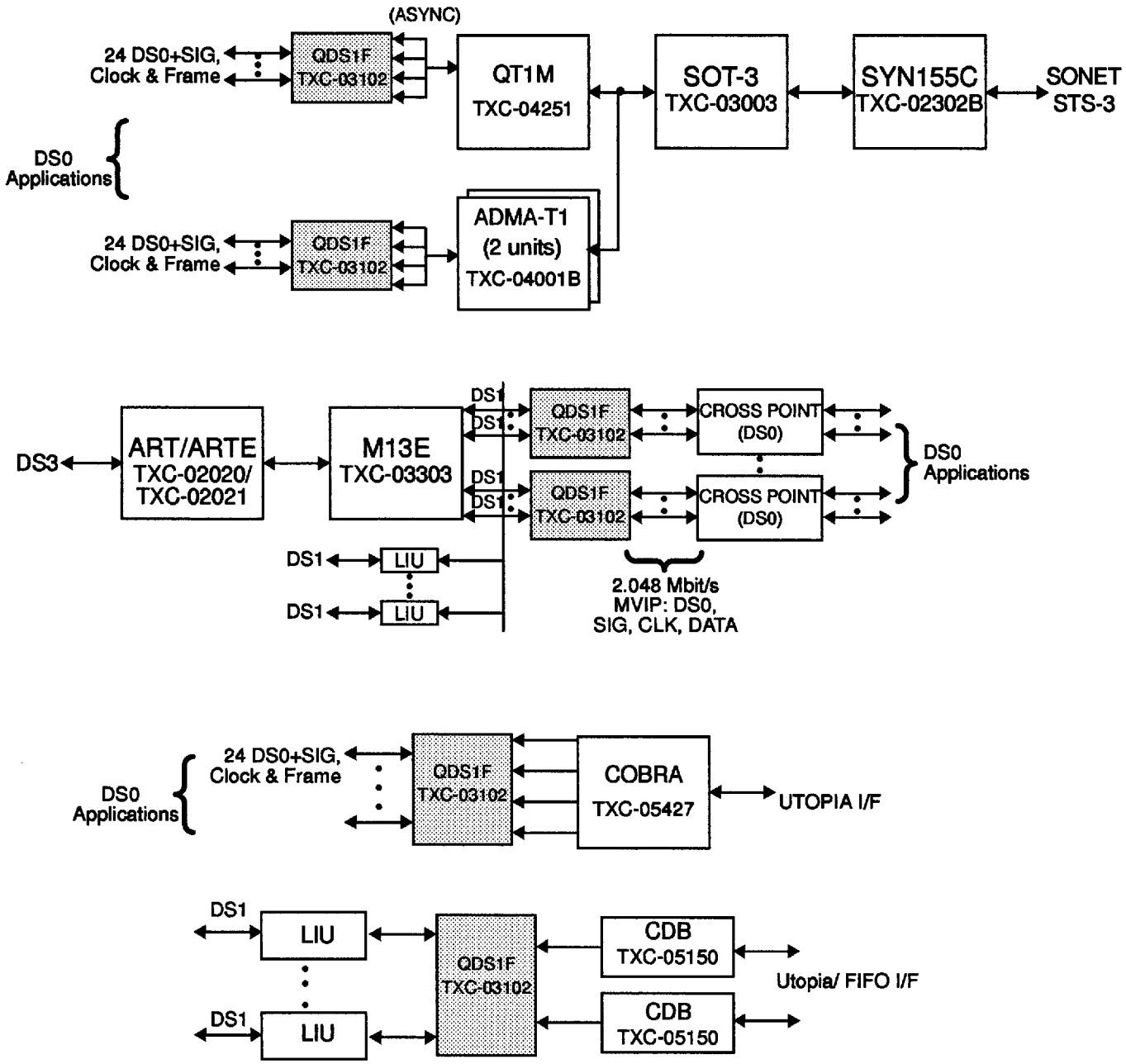


Figure 29. Some QDS1F TXC-03102 Applications

PACKAGE INFORMATION

The QDS1F device is packaged in a 128-pin plastic quad flat package suitable for surface mounting, as illustrated in Figure 30.

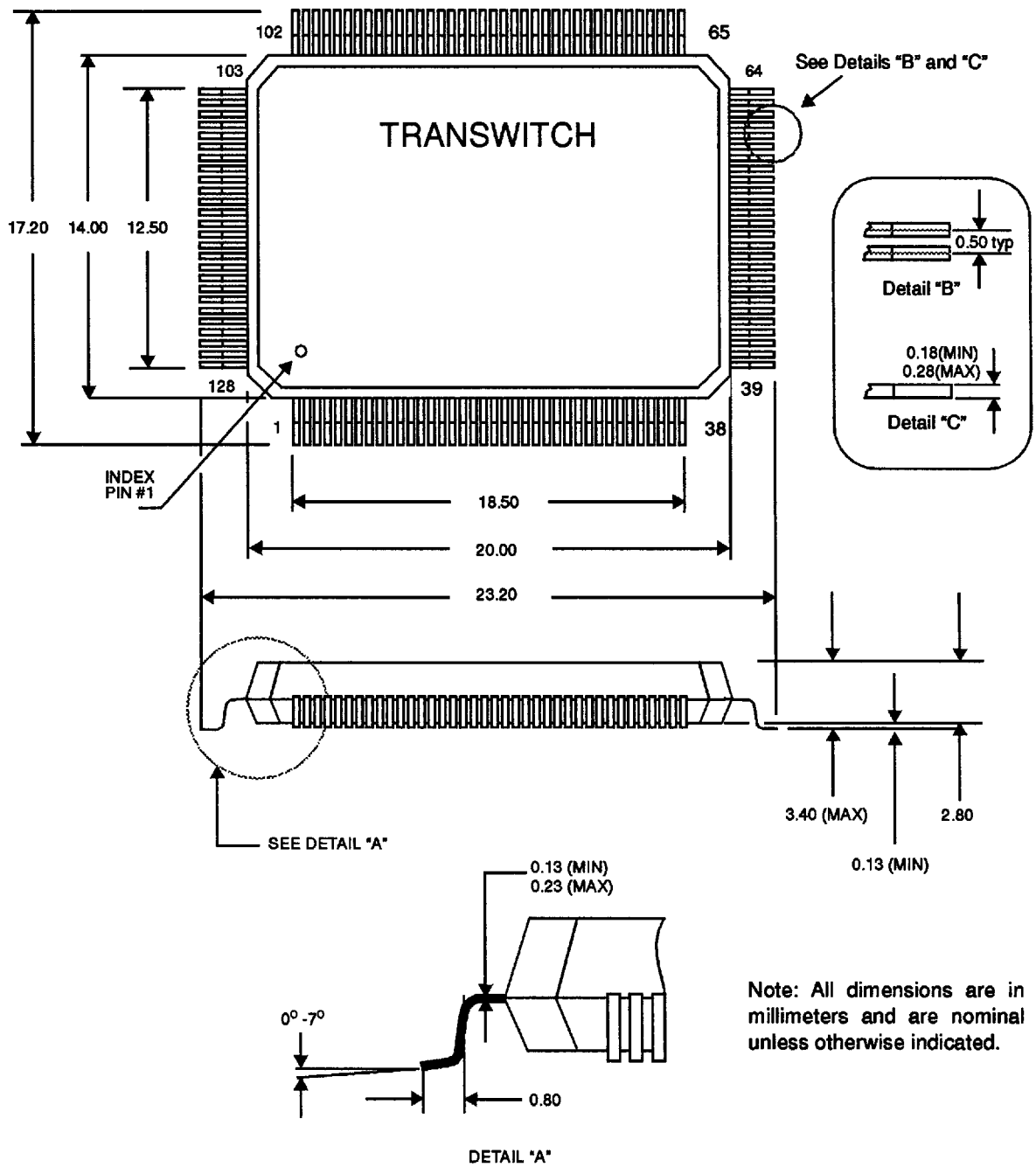


Figure 30. QDS1F TXC-03102 128-Pin Plastic Quad Flat Package

ORDERING INFORMATION

Part Number: TXC-03102-AIPQ	128-pin Plastic Quad Flat Package

RELATED PRODUCTS

TXC-02020, ART VLSI Device (Advanced STS-1/DS3 Receiver/Transmitter). ART performs the transmit and receive line interface functions required for transmission of STS-1 (51.840 Mbit/s) and DS3 (44.736 Mbit/s) signals across a coaxial interface.

TXC-02021, ARTE VLSI Device (Advanced STS-1/DS3 Receiver/Transmitter). ARTE has the same functionality as ART, plus expanded features.

TXC-02302B, SYN155C VLSI Device (155-Mbit/s Synchronizer, Clock and Data Output). This device is similar to the SYN155. It has both clock and data outputs on the line side.

TXC-03001, SOT-1 VLSI Device (SONET STS-1 Overhead Terminator). This device performs section, line and path overhead processing for STS-1 SONET signals. Has programmable STS-1 or STS-N modes.

TXC-03003, SOT-3 VLSI Device (STM-1/STS-3/STS-3c Overhead Terminator). This device performs section, line and path overhead processing for STM-1/STS-3/STS-3c signals. Compliant with ANSI and ITU-T standards.

TXC-03301, M13 VLSI Device (DS3/DS1 Mux/Demux). This single-chip multiplex/demultiplex device provides the complete interfacing function between a single DS3 signal and 28 independent DS1 signals.

TXC-03303, M13E VLSI Device, Extended feature version of the TXC-03301 (M13).

TXC-03375, M12 VLSI Device (DS2/DS1 Mux/Demux). Multiplexes four DS1 signals into one DS2 signal, and in the other direction demultiplexes one DS2 signal into its four constituent DS1 signals.

TXC-04001B, ADMA-T1 VLSI Device (Dual DS1 to VT1.5 or TU-11 Async Mapper-Desync). Interconnects two DS1 signals with any two asynchronous mode VT1.5 or TU-11 tributaries carried in SONET STS-1 or SDH AU-3 rate payload interface.

TXC-04251, QT1M VLSI Device (Quad DS1 to VT1.5 or TU-11 Async Mapper-Desync). Interconnects four DS1 signals with any four asynchronous mode VT1.5 or TU-11 tributaries carried in SONET STS-1 or SDH AU-3 rate payload interface.

TXC-05101C, HDLC VLSI Device (HDLC Controller, 36-Bit Terminal I/O). High Speed High Level Data Link Controller that sends and receives packets at line rates up to 51.84 Mbit/s using either a nibble, byte-parallel, or serial interface.

TXC-05150, CDB VLSI Device (Cell Delineation Block). Provides cell delineation for ATM cells carried in a physical line at rates of 1.544 to 155 Mbit/s.

TXC-05427, COBRA VLSI Device (Constant Bit Rate ATM Adaptation Layer 1). Provides ATM AAL1 Structured and Unstructured service for four T1, E1 or n x 64k constant bit rate interfaces.

TXC-06125, XBERT VLSI Device (Bit Error Rate Generator/Receiver). Programmable multi-rate test pattern generator and receiver in a single chip with serial, nibble, or byte interface capability.