QLUM3317-PQ208C Device Data Sheet

Utopia Level 3 Master/Master Bridge

1.0 Utopia Level 3 (L3) Bridge Core Features

- Implements two Utopia L3 Masters providing a solution to bridge Utopia Slave devices
- Compliant with ATM-Forum af-phy-0136.000 (Utopia L3)
- Meets 104MHz performance offering up to 3.2Gbps cell rate transfers (32 bit)
- Single chip solution for improved system integration
- Support cell level transfer mode
- Cell and clock rate decoupling with on chip FIFOs
- Up to 1.5 KByte of on chip FIFO per data direction
- Integrated management interface and built-in errored cell discard
- ATM Cell size programmable via external pins from 16 to 128 bytes
- Optional Utopia parity generation/checking enable/disable via external pin
- Built in JTAG port (IEEE1149 compliant)
- Simulation model available for system level verification (Contact Quicklogic for details)
- Solution also available as flexible Soft-IP core, delivered with a full device modelization and verification testbenches

2.0 Utopia Overview

The Utopia (Universal Test & Operations PHY Interface for ATM) interface is defined by the ATM Forum to provide a standard interface between ATM devices and ATM PHY or SAR (segmentation and Re-assembly) devices.

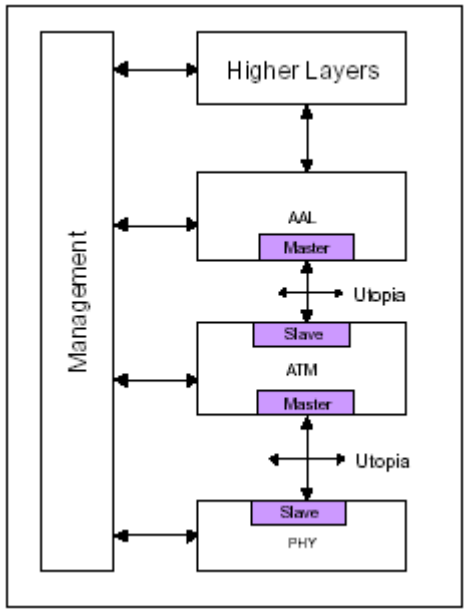

Figure 1: Utopia Reference Model

The Utopia Standard defines a full duplex bus interface with a Master/Slave paradigm. The Slave interface responds to the requests from the Master. The Master performs PHY arbitration and initiates data transfers to and from the Slave device.

The ATM forum has standardized the Utopia Levels 1 (L1) to 3 (L3). Each level extends the maximum supported interface speed from OC3, 155Mbps (L1) over OC12, 622Mbps (L2) to 3.2Gbit/s (L3).

The following Table 1 gives an overview of the main differences in these three levels.

Table 1: Utopia Level Differences

Utopia Level	Interface Width	Max. Interface Speed	Maximum Throughput
1	8-bit	25 MHz	200 Mbps (typ. OC3 155 Mbps)
2	8-bit, 16-bit	50 MHz	800 Mbps (typ. OC12 622 Mbps)
3	8-bit, 32-bit	104 MHz	3.2 Gbps (typ. OC48 2.5 Gbps)

Utopia Level 1 implements an 8-bit interface running at up to 25MHz. Level 2 adds a 16 Bit interface and increases the speed to 50MHz. Level 3 extends the interface further by a 32 Bit word-size and speeds up to 104MHz providing rates up to 3.2 Gbit/s over the interface.

In addition to the differences in throughput, Utopia Level 2 uses a shared bus offering to physically share a single interface bus between one master and up to 31 slave devices (Multi-PHY or MPHY operation). This allows the implementation of aggregation units that multiplex several slave devices to a single Master device. The Level 2 and Level 3 are point-to-point only, whereas Level 1 has no notion of multiple slaves. Level 3 still has the notion of multiple slaves, but they must be implemented in a single physical device connected to the Utopia Interface.

3.0 Utopia Master/Master Bridge Application

As it is not possible to connect two Slave devices together, the Master/Master Bridge provides the necessary interfaces to convey between two Slave devices as shown in Figure 2.

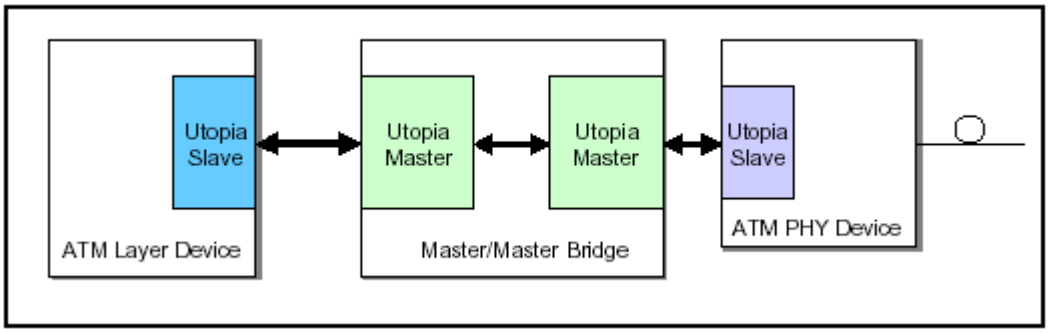

Figure 2: Utopia Master Bridge

The Bridge automatically transfers data as soon as it becomes available from one side to the other. Internal asynchronous FIFOs enable independent clock domains for each interface.

4.0 Application

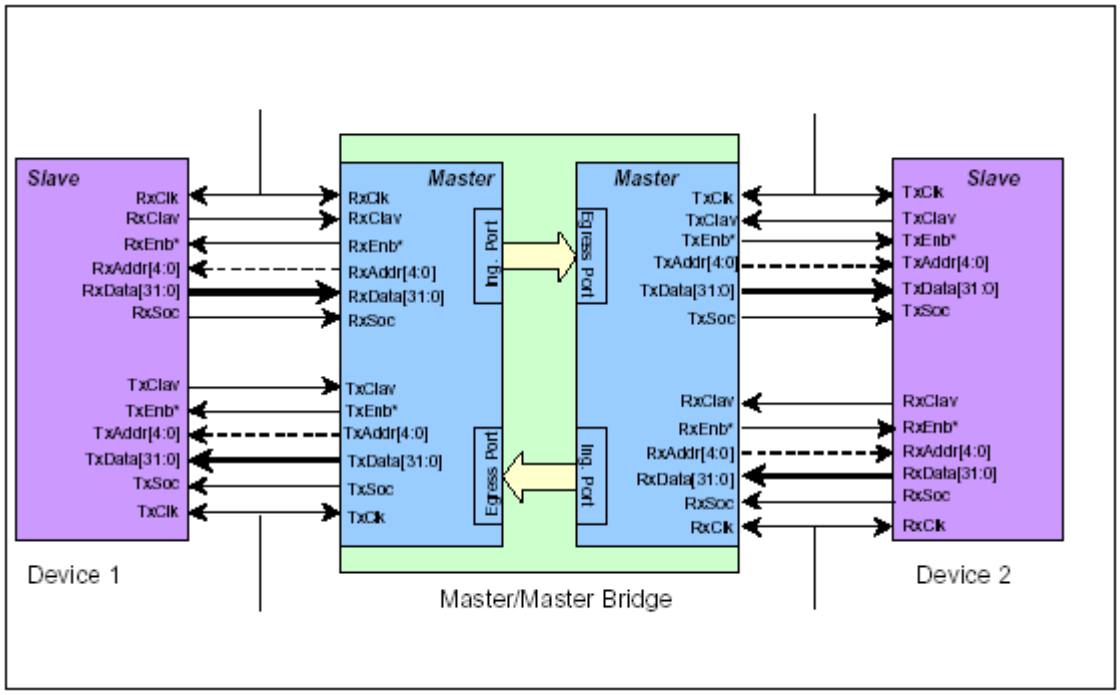

Figure 3: Master/Master Bridge connecting two Slave Devices

Data flows from the Bridge's RX Ports to the corresponding TX Ports on the other side of the bridge.

5.0 Core Pinout

Bridge Core implements all the required Utopia signals and provides all the Utopia optional signals (Indicated by an 'O' in the following tables).

In addition to the Utopia Interface signals, error indication signals are available for error monitoring or statistics. An error indication always shows that a cell has been discarded by the bridge. Possible errors are parity or cell-length errors on the receive interface of the corresponding Utopia Interfaces.

All Utopia interfaces work in the same transfer mode (cell level).

To identify the sides of the bridge, the notion "WEST" and "EAST" for the corresponding interfaces will be used.

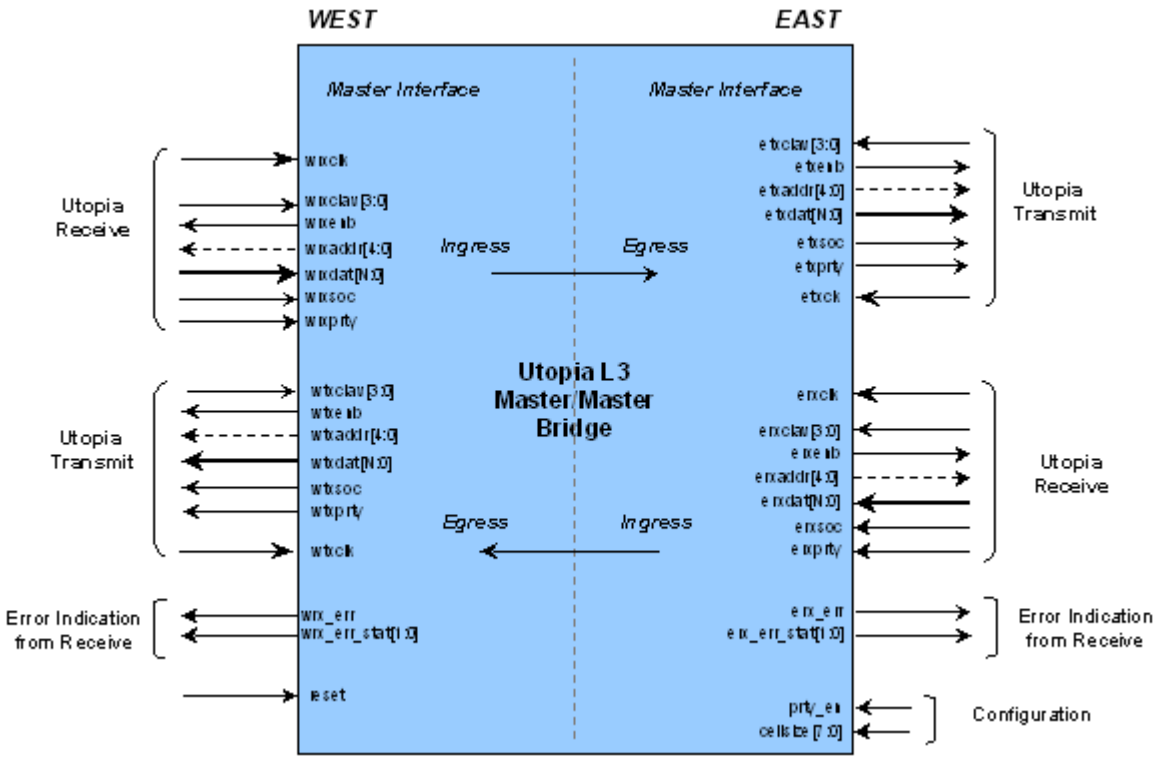

Figure 4: Utopia Level 3 Master/Master Bridge Top Entity

5.1 Signal Descriptions

Table 2: Global Signal

Pin	Mode	Description
reset	In	Active high chip reset

Table 3: Device Management Interface

Pin	Mode	Description
wrx_err	Out	Receive error indication on west receive interface. When driven high, indicates that an errored cell (Wrong parity or wrong length) was received from the device connected to the west interface and is discarded.
wrx_err_stat(1:0)	Out	Receive error status information for west receive interface. When wrx_err is driven, indicates the error status of the discarded cell: • wrx_err_stat(0) : When set to '1' indicates that a cell is discarded because of a parity error. • wrx_err_stat(1) : When set to '1' indicates that a cell is discarded because it has a wrong length (Consecutive assertion of ut_tx_soc on the Utopia interface within less than a complete cell time).
erx_err(n)	Out	Receive error indication on east receive interface(s). When driven high, indicates that an errored cell (Wrong parity or wrong length) was received from the device connected to the east interface side.
erx_err_stat (1:0)	Out	Receive error status information for east receive interface. When erx_err is driven, indicates the error status of the discarded cell: • erx_err_stat(0) : When set to '1' indicates that a cell is discarded because of a parity error. • erx_err_stat(1) : When set to '1' indicates that a cell is discarded because it has a wrong length (Consecutive assertion of ut_tx_soc on the Utopia interface within less than a complete cell time).

Table 4: West Utopia Master Transmit Interface

Pin	Mode	Description
wtxclk	In	104MHz transmit byte clock. The Core samples all Utopia Transmit signals on txclk rising edge.
wtxdata[15:0]	Out	Transmit data bus.
wtxprty	Out	Transmit data bus parity. Standard odd or non-standard even parity can be optionally checked by the connected Slave.
		When the parity check is disabled during the Core configuration, or not used in the design, the pin txprty should be left open.
wtxsoc	Out	Transmit start of cell. Asserted by the Master to indicate that the current word is the first word of a cell.
wtxenb	Out	Active low transmit data transfer enable.
wtxclav[0]	In	Cell buffer available. Asserted in octet level transfers to indicate to the Master that the FIFO is almost full (Active low) or, in cell level transfers, to indicate to the Master that the PHY port FIFO has space to accept one cell.
wtxclav[3:1] (0)	In	Extra FIFO Full / Cell buffer available. In MPHY mode and when direct status indication is selected during the Core configuration, one txclav signal is implemented per PHY port. The maximum number of clav signals is limited to four.
wtxaddr[4:0]	Out	Utopia transmit address. When the Core operates in MPHY mode, address bus used during polling and slave port selection. Bit 4 is the MSB. txaddr(4:0) becomes optional (And should be left open) when the Core does not operate in MPHY mode.

NOTE: *(O) indicates optional signals.*

Table 5: West Utopia Master Receive Interface

Pin	Mode	Description
wrxclk	In	104MHz receive byte clock. The Core samples all Utopia Receive signals on rxclk rising edge.
wrxdata[15:0]	In	Receive data bus.
wrxprty(0)	In	Receive data bus parity. Standard odd or non standard even parity can be optionally generated by the Utopia Slave Core. When the parity generation is disabled during the Core configuration, the pin rxprty can be let unconnected.
wrxsoc	In	Receive start of cell. Asserted to indicate that the current word is the first word of a cell.
wrxenb	Out	Active low transmit data transfer enable.
wrxclav[0]	In	Cell buffer available. Asserted in octet level transfers to indicate to the Master that the FIFO is almost empty (Active low) or, in cell level transfers, to indicate to the Master that the PHY port FIFO has space one cell available in the FIFO.
wrxclav[3:1] (0)	In	Extra FIFO Full / Cell buffer available. In MPHY mode and when direct status indication is selected, one rxclav signal is implemented per PHY port. The maximum number of clav signals is limited to four.
wrxaddn(4:0)	Out	Utopia receive address. When the Core operates in MPHY mode, address bus used during polling and slave port selection. Bit 4 is the MSB. txaddr(4:0) becomes optional (And should be left open) when the Core does not operate in MPHY mode.

Table 6: East Utopia Master Transmit Interface

Pin	Mode	Description
etxclk	In	104MHz transmit byte clock. The Core samples all Utopia Transmit signals on txclk rising edge.
etxdata[15:0]	Out	Transmit data bus.
etxprty	Our	Transmit data bus parity. Standard odd or non-standard even parity can be optionally checked by the connected Slave. When the parity check is disabled during the Core configuration, or not used in the design, the pin txprty should be left open.
etxsoc	Out	Transmit start of cell. Asserted by the Master to indicate that the current word is the first word of a cell.
etxenb	Out	Active low transmit data transfer enable.
etxclav[0]	In	Cell buffer available. Asserted in octet level transfers to indicate to the Master that the FIFO is almost full (Active low) or, in cell level transfers, to indicate to the Master that the PHY port FIFO has space to accept one cell.
etxclav[3:1] (0)	In	Extra FIFO Full / Cell buffer available. In MPHY mode and when direct status indication is selected during the Core configuration, one txclav signal is implemented per PHY port. The maximum number of clav signals is limited to four.
etxaddr[4:0]	Out	Utopia transmit address. When the Core operates in MPHY mode, address bus used during polling and slave port selection. Bit 4 is the MSB. txaddr(4:0) becomes optional (And should be left open) when the Core does not operate in MPHY mode.

NOTE: *(O) indicates optional signals.*

Table 7: East Utopia Master Receive Interface

Pin	Mode	Description
erxclk	In	104MHz receive byte clock. The Core samples all Utopia Receive signals on rxclk rising edge.
erxdata[15:0]	In	Receive data bus.
erxprty (0)	In	Receive data bus parity. Standard odd or non standard even parity can be optionally generated by the Utopia Slave Core. When the parity generation is disabled during the Core configuration, the pin rxprty can be let unconnected.
erxsoc	In	Receive start of cell. Asserted to indicate that the current word is the first word of a cell.
erxenb	Out	Active low transmit data transfer enable.
erxclav[0]	In	Cell buffer available. Asserted in octet level transfers to indicate to the Master that the FIFO is almost empty (Active low) or, in cell level transfers, to indicate to the Master that the PHY port FIFO has space one cell available in the FIFO.
rxclav[3:1] (0)	In	Extra FIFO Full / Cell buffer available. In MPHY mode and when direct status indication is selected, one rxclav signal is implemented per PHY port. The maximum number of clav signals is limited to four.
erxaddr(4:0)	Out	Utopia receive address. When the Core operates in MPHY mode, address bus used during polling and slave port selection. Bit 4 is the MSB. taddr(4:0) becomes optional (And should be left open) when the Core does not operate in MPHY mode.

Table 8: Device Configuration Pins

Pin	Mode	Description
prty_en	In	Enable parity checking on the Utopia interface. If disabled (tied to 0), the wrx_err_stat(0) signal can be ignored and left open and the rx parity input should be tied to 0. Also the tx parity pins can be left open.
cellsize[7:0]	In	Define cellsize: sets the size in bytes of a cell. Binary value to be set usually by board wiring. The size must be a multiple of 2.

The configuration pins are not intended for change during operation. They are usually board wired to configure the device for operation.

6.0 Signal Descriptions

The externally provided Utopia Transmit and Receive clocks are connected to global resources to provide low skew and fast chip level distribution. In both data directions, the two corresponding Utopia Interfaces are decoupled by asynchronous FIFOs.

Therefore each interface runs completely independently each at its own tx and rx clocks which typically are 104 MHz.

The Error indications of the two receive interfaces are always sampled within the west clock domains. The errors of the east rx interface is available on the erx_err signal, which is handled using the west clock domain (wtxclk). The west rx error is directly derived from the west rx block (wrxclk).

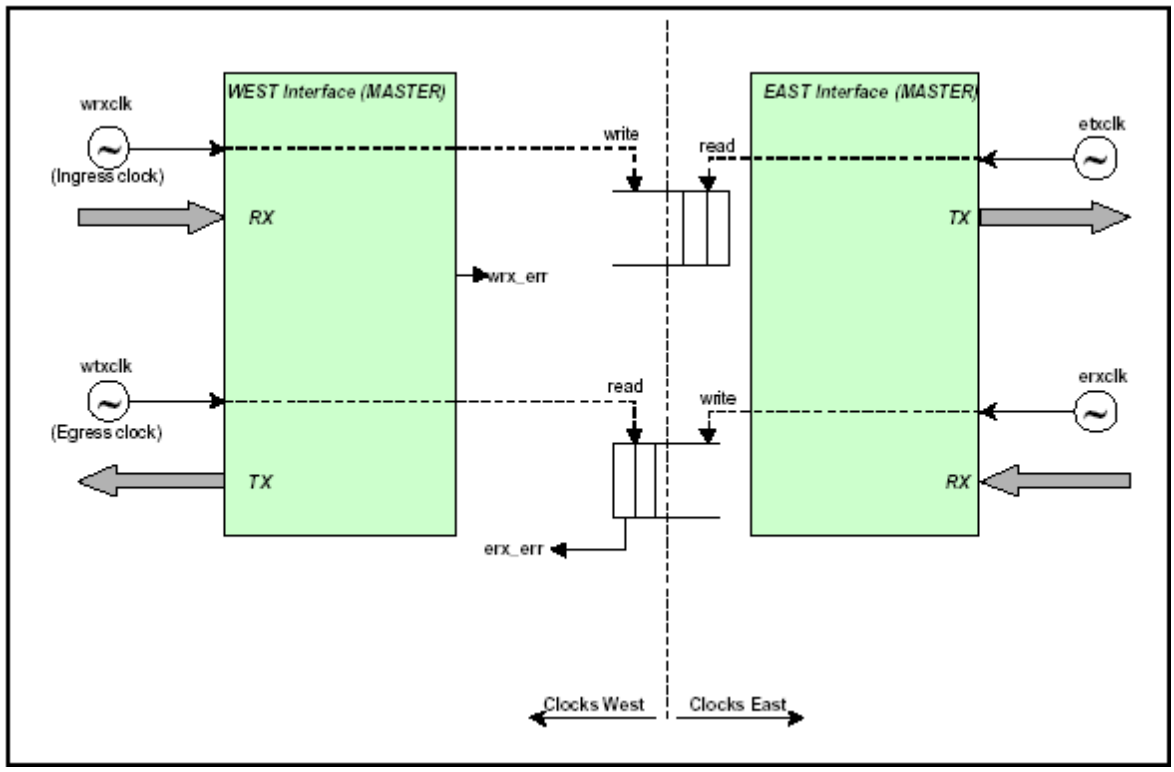

Figure 5: Master/Master Bridge Clock Distribution

7.0 Functional Description - Utopia Interface

The Utopia Bridge operates in single PHY mode. Therefore no address bus and only a single status pin (clav[0]) per direction is used on the interfaces.

7.1 Utopia Interface Single PHY Transmit Interface

The Transmit interface is controlled by the ATM layer.

The transmit interface has data flowing in the same direction as the ATM enable ut_txenb. The ATM transmit block generates all output signals on the rising edge of the `ut_txclk`.

Transmit data is transferred from the ATM layer to PHY layer via the following procedure. The Core indicates it can accept data using the `ut_txclav` signal, then the ATM layer drives data onto `ut_txdat` and asserts `ut_txenb`.

When a cell transfer is initiated, the Master or the Slave cannot pause the transfer by any means.

7.1.1 Single Cell Transfer

The Slave asserts `ut_txclav` **1** when it is capable of accepting the transfer of a whole cell. The Core asserts `ut_txenb` (Low) to indicates that it drives valid data to the Slave **2**. Together with the first word of a cell, the Core device asserts `ut_txsoc` for one clock cycle **3**.

To ensure that the ATM Layer (Core) does not cause transmit overrun, the Slave de-asserts `ut_txclav` when `ut_txsoc` is de-asserted by the Core **4**.

To complete the cell transfer, the Core de-asserts the Utopia enable signal `ut_txenb` **5**.

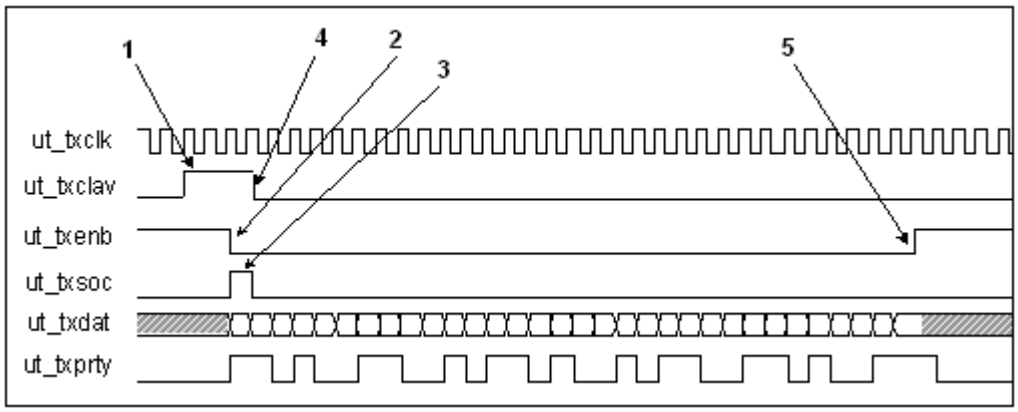

Figure 6: Single Cell Transfer - Cell Level Transfer

7.1.2 Back to Back Cells Transfer

When, during a cell transfer, the Slave is able to receive a subsequent cell, the Core keeps `ut_txenb` asserted between two cells **1** and asserts `ut_txsoc`, to start a new cell transfer, immediately after the last word of the previous cell **2**.

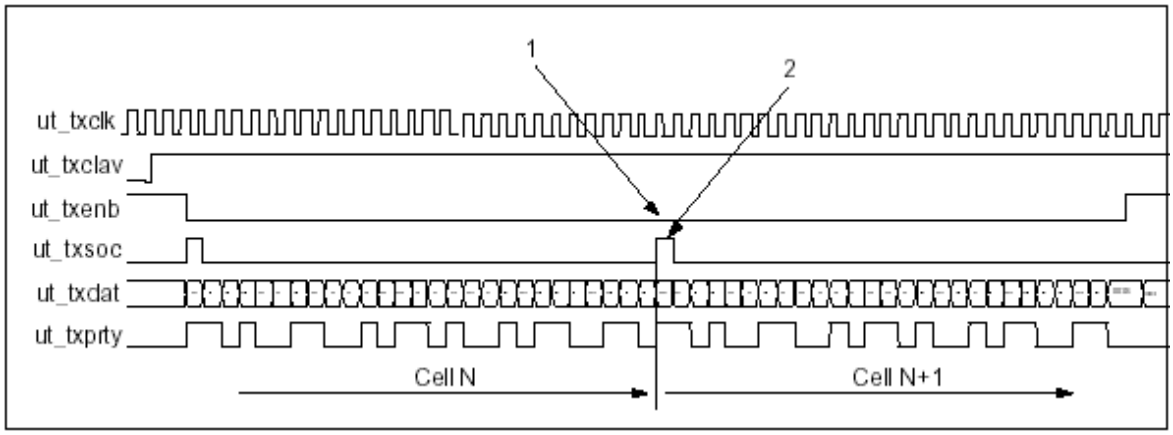

Figure 7: Back to Back Cell Transfer

7.2 Utopia Interface Single PHY Receive Interface

The Receive interface is controlled by the Master interface. The receive interface has data flowing in the opposite direction to the Master's enable `ut_rxenb`.

Receive data is transferred from the Slave to the Master via the following procedure. The Slave indicates it has valid data, then the Master asserts `ut_rxenb` to read this data from the Slave. The Master indicates valid data (thereby controlling the data flow) via the `ut_rxclav` signal.

When a cell transfer is initiated, the transfer cannot be paused by the Master or the Slave.

7.2.1 Cell Level Transfer - Single Cell

The Slave asserts `ut_rxclav` when it is ready to send a complete cell to the Master **1**. The Master interface asserts `ut_rxenb` to start the cell transfer **2**. The Slave samples `ut_rxenb` and start driving data on the following clock edge **3**. The Slave asserts `ut_rxsoc` together with the cell first word to indicate the start of a cell **4**.

The Master drives ut_txenb high two clock cycles before the expected end of the current cell if the Slave has no more cell to transfer **5**. The Slave de-asserts ut_rxclav to indicate that no new cell is available **6** together with the start of cell indication.

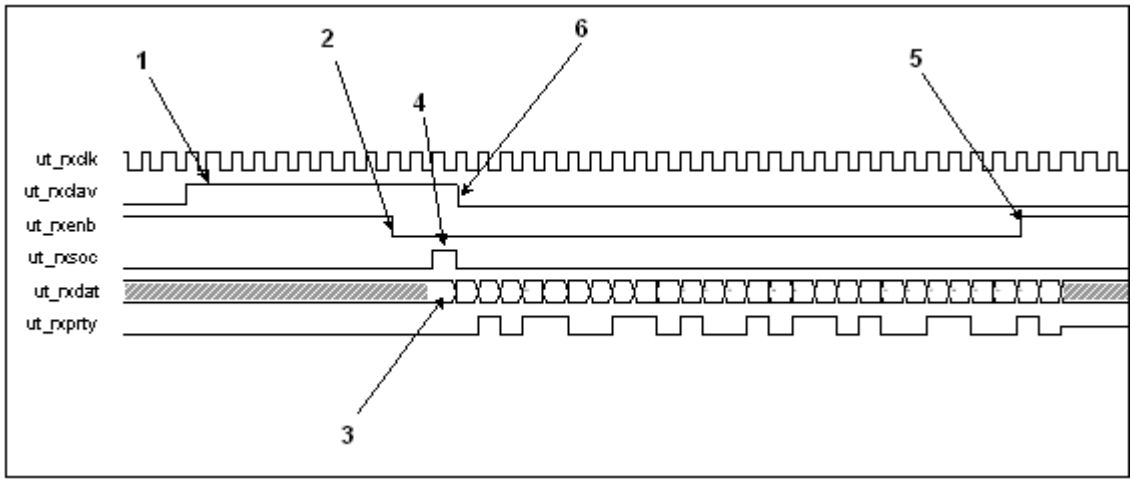

Figure 8: Single Cell Transfer

7.2.2 Cell Level Transfer - Back to Back Cells

If the Master keeps ut_rxenb asserted at the end of a cell transfer **1** and if the Slave has a new cell to send, the Slave keeps ut_rxclav drives the new cell asserting ut_rxsoc to indicate the start of a new cell **2**.

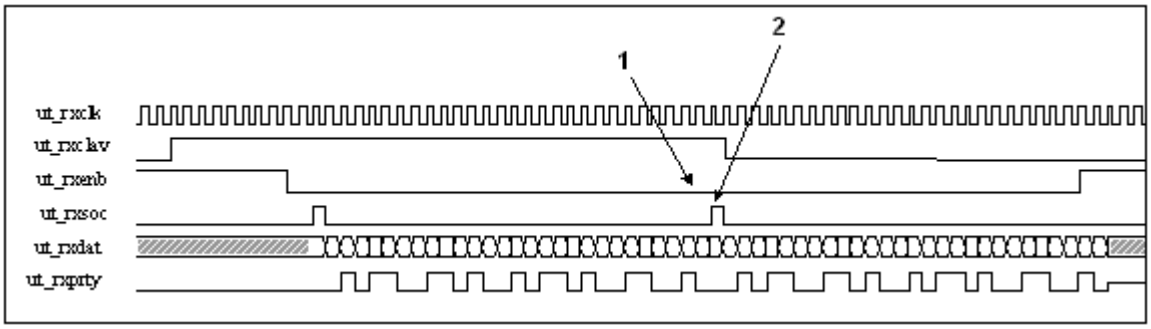

Figure 9: Back to Back Cells Transfer

8.0 Core Management and Error Handling

On Ingress, the Utopia Master Blocks are designed to handle and report Utopia errors such as Parity error or wrong cell length. Errored cells are discarded with an error status provided on pins for use by external management facilities.

The error handling only applies to the corresponding receive parts of the core (i.e. Ingress Ports).

When an errored cell is received on the Utopia interface, the Core discards the complete cell and provides a cell discard indication (Signal eg_err asserted) **1** together with a cell discard status (Signal eg_err_stat(n)(m:0)) **2**.

NOTE: *eg_err is routed to the corresponding wrx_err and erx_err respectively (see Figure 4).*

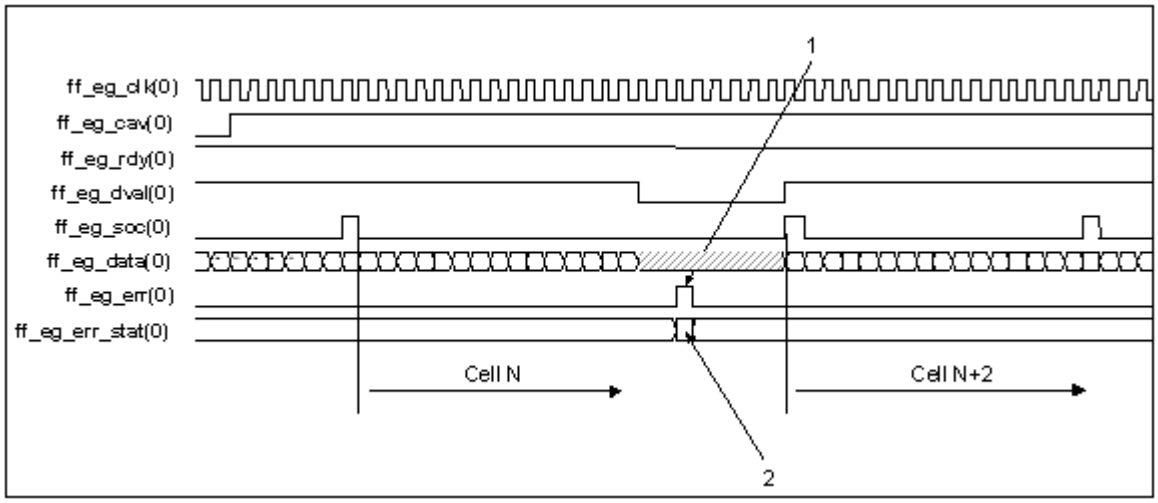

Figure 10: Cell Discard Indication

Table 9: Error Status Word Bit Coding

Error Status Bit	Name	Description
0	PARITY_ERR	Valid when wrx/erx_err is asserted. If set to one indicates that a cell is discarded with a parity error decoded by the Core.
1	LENGTH_ER	Valid when wrx/erx_err is asserted. If set to one indicates that a cell is discarded with a cell length error detected on the Utopia interface.

The signals are sampled on the corresponding clocks from the west interface:

- erx_... sampled with wtxclk (west transmit clock)
- wrx_... sampled with wrxclk (west receive clock)

9.0 Complexity and Performance Summary

9.1 Timing Parameters Definition

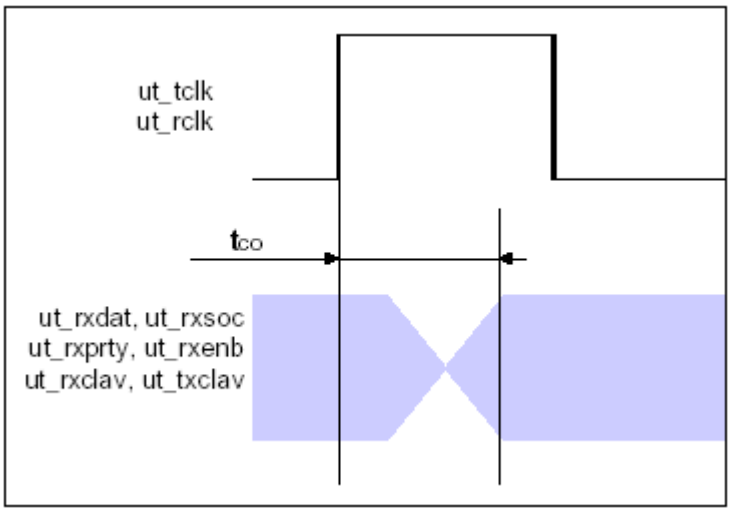

Figure 11: Tco Timing Parameter Definition

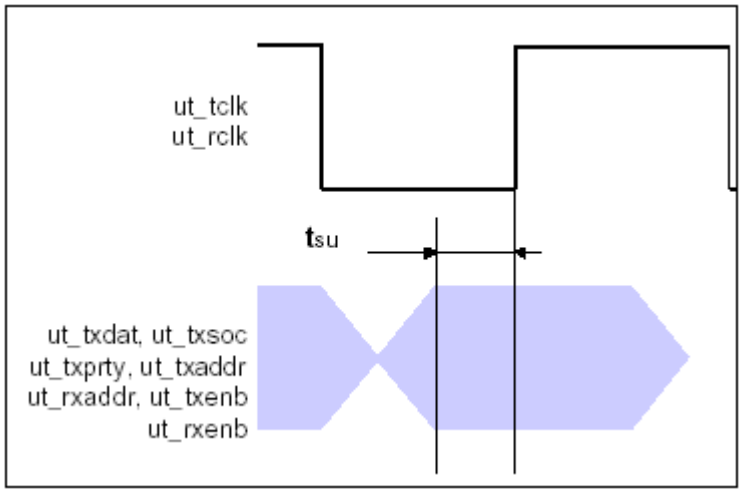

Figure 12: Tsu Timing Parameter Definition

Table 10: 16-Bit Utopia Interface Timing Characteristics

Parameter	typ	Max	Unit
tco	7.0	6.0	ns
tsu	2.5	1.8	ns
wrxclk		104	MHz
wtxclk		104	MHz
erxclk		104	MHz
etxclk		104	MHz
minimum reset time	50		ns

NOTE: *Timing model "worst" case is used.*

10.0 Device Pinout

10.1 Signals Overview

Table 11: Signals Overview Table

Signals	Description
wrxclk, wrxclav, wrxenb*, wrxdat, wrxsoc	West Utopia Receive Interface.
wtxclk, wtxclav, wtxenb*, wtxdata, wtxsoc	West Utopia Transmit Interface.
wrx_err, wrx_err_stat	West Interface error indication (sampled with wrxclk).
erxclk, erxclav, erxenb*, erxdata, erxsoc	East Utopia Receive Interface.
etxclk, etxclav, etxenb*, etxdata, etxsoc	East Utopia Transmit Interface.
erx_err, erx_err_stat	East Interface error indication (sampled with wtxclk).
prty_en, cellsize	Configuration Pins to be board wired. Cellsize [0] should be tied to GND.
reset	Active high device reset
GND	Ground
VCC	Device Power 2.5 V
clk(x)	unused clock inputs should be tied to GND
IOCTRL(x)	
VCCIO(x)	IO Power 3.3 V
INREF(x)	connect to GND
PLLRST(x)	connect to GND or VCC
PLLOUT(x)	connect to GND or VCC
VCCPLL(x)	
GNDPLL(x)	
TCK, TRSTB	JTAG signals. connect to GND
TMS, TDI	JTAG signals. connect to VCC
TDO	JTAG signal. leave open
iov	
nc	not connected. should be left open

*: active low signal

NOTE: *Unused Pins (data busses) in the following tables are to be handled like "nc".*

10.2 PQ208 PQFP Device Diagram

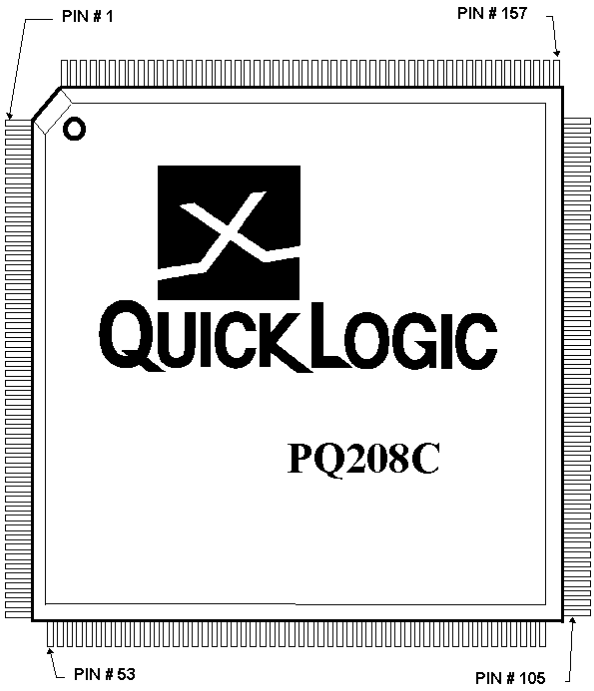

Figure 13: PQ208 top view

10.3 PQ208 PQFP Pinout Table

Table 12: 208 Pin PQFP (PQ208) Pinout Table

PIN	Function	PIN	Function	PIN	Function	PIN	Function
1	pllrst(3)	53	gnd	105	pllrst(1)	157	gnd
2	vccpll(3)	54	vccpll(2)	106	vccpll(1)	158	vccpll(0)
3	gnd	55	pllrst(2)	107	etxclav[0]	159	pllrst(0)
4	gnd	56	vcc	108	gnd	160	gnd
5	wtxclav[0]	57	wrxprty	109	etxprty	161	erxdat[0]
6	wtxprty	58	gnd	110	etxenb	162	vccio(g)
7	wtxenb	59	wrxenb	111	vccio(e)	163	erxdat[1]
8	vccio(a)	60	vccio(c)	112	etxsoc	164	erxdat[2]
9	wtxsoc	61	wrxsoc	113	vcc	165	vcc
10	wtxdat[0]	62	wrxdat[0]	114	etxdat[0]	166	erxdat[3]
11	ioctrl(a)	63	wrxdat[1]	115	etxdat[1]	167	erxdat[4]
12	vcc	64	wrxdat[2]	116	etxdat[2]	168	erxdat[5]
13	inref(a)	65	wrxdat[3]	117	ioctrl(e)	169	ioctrl(g)
14	ioctrl(a)	66	wrxdat[4]	118	inref(e)	170	inref(g)
15	wtxdat[1]	67	ioctrl(c)	119	ioctrl(e)	171	ioctrl(g)
16	wtxdat[2]	68	inref(c)	120	etxdat[3]	172	erxdat[6]
17	wtxdat[3]	69	ioctrl(c)	121	etxdat[4]	173	erxdat[7]
18	wtxdat[4]	70	wrxdat[5]	122	vccio(e)	174	iov
19	vccio(a)	71	wrxdat[6]	123	gnd	175	vcc
20	wtxdat[5]	72	vccio(c)	124	etxdat[5]	176	etxdat[8]
21	gnd	73	wrxdat[7]	125	etxdat[6]	177	vccio(g)
22	wtxdat[6]	74	wtxdat[8]	126	etxdat[7]	178	gnd
23	tdi	75	gnd	127	clk(5)	179	etxdat[9]
24	wtxclk	76	vcc	128	etxclk	180	etxdat[10]
25	clk(1)	77	wtxdat[9]	129	vcc	181	etxdat[11]
26	vcc	78	trstb	130	erxclk	182	vcc
27	wrxclk	79	vcc	131	vcc	183	tck
28	clk(3)	80	wtxdat[10]	132	clk(8)	184	vcc
29	vcc	81	wtxdat[11]	133	tms	185	etxdat[12]
30	clk(4)	82	wtxdat[12]	134	etxdat[8]	186	etxdat[13]
31	wtxdat[7]	83	gnd	135	etxdat[9]	187	etxdat[14]
32	wtxdat[8]	84	vccio(d)	136	etxdat[10]	188	gnd
33	gnd	85	wtxdat[13]	137	gnd	189	vccio(h)
34	vccio(b)	86	vcc	138	vccio(f)	190	etxdat[15]
35	wtxdat[9]	87	wtxdat[14]	139	etxdat[11]	191	cellsize[7]
36	wtxdat[10]	88	wtxdat[15]	140	etxdat[12]	192	ioctrl(h)
37	wtxdat[11]	89	vcc	141	etxdat[13]	193	cellsize[6]
38	wtxdat[12]	90	wrx_err	142	etxdat[14]	194	inref(h)
39	ioctrl(b)	91	wrx_err_stat[0]	143	etxdat[15]	195	vcc
40	inref(b)	92	ioctrl(d)	144	ioctrl(f)	196	ioctrl(h)
41	ioctrl(b)	93	inref(d)	145	inref(f)	197	cellsize[5]
42	wtxdat[13]	94	ioctrl(d)	146	vcc	198	cellsize[4]
43	wtxdat[14]	95	wrx_err_stat[1]	147	ioctrl(f)	199	cellsize[3]
44	vccio(b)	96	erx_err	148	nc	200	cellsize[2]
45	N/C	97	erx_err_stat[0]	149	erxclav[0]	201	cellsize[1]
46	vcc	98	vccio(d)	150	vccio(f)	202	cellsize[0]
47	nc	99	erx_err_stat[1]	151	erxprty	203	vccio(h)
48	wrxclav[0]	100	reset	152	erxenb	204	gnd
49	gnd	101	gnd	153	gnd	205	prty_en
50	tdo	102	pllout(0)	154	erxsoc	206	pllout(2)
51	pllout(1)	103	gnd	155	pllout(3)	207	gnd
52	gndpll(2)	104	gndpll(1)	156	gndpll(0)	208	gndpll(3)

11.0 References

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12.0 Contact

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