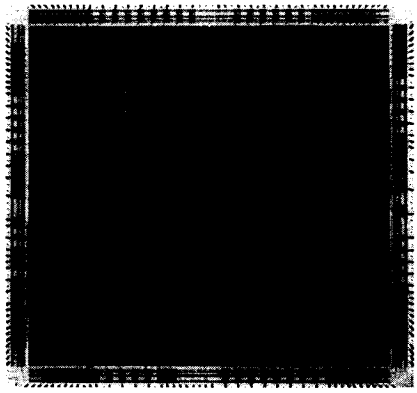
L64133
32-Bit HCMOS IEEE Floating-Point Processor

LSI LOGIC

Description

The L64133 is a high-speed processor which contains a full 32-bit floating-point multiplier and a full 32-bit floating-point ALU on a single chip. This three-bus device has a clean architecture with no internal pipelines. It is ideally suited for high-speed graphics and digital signal processing applications.

The L64133 supports the ANSI/IEEE Standard P754-1985 (commonly called IEEE) format. The device has been implemented in a 0.7-micron HCMOS process for high-speed with low power dissipation, and is packaged in an industry standard 144-pin ceramic pin grid array.



L64133 Chip

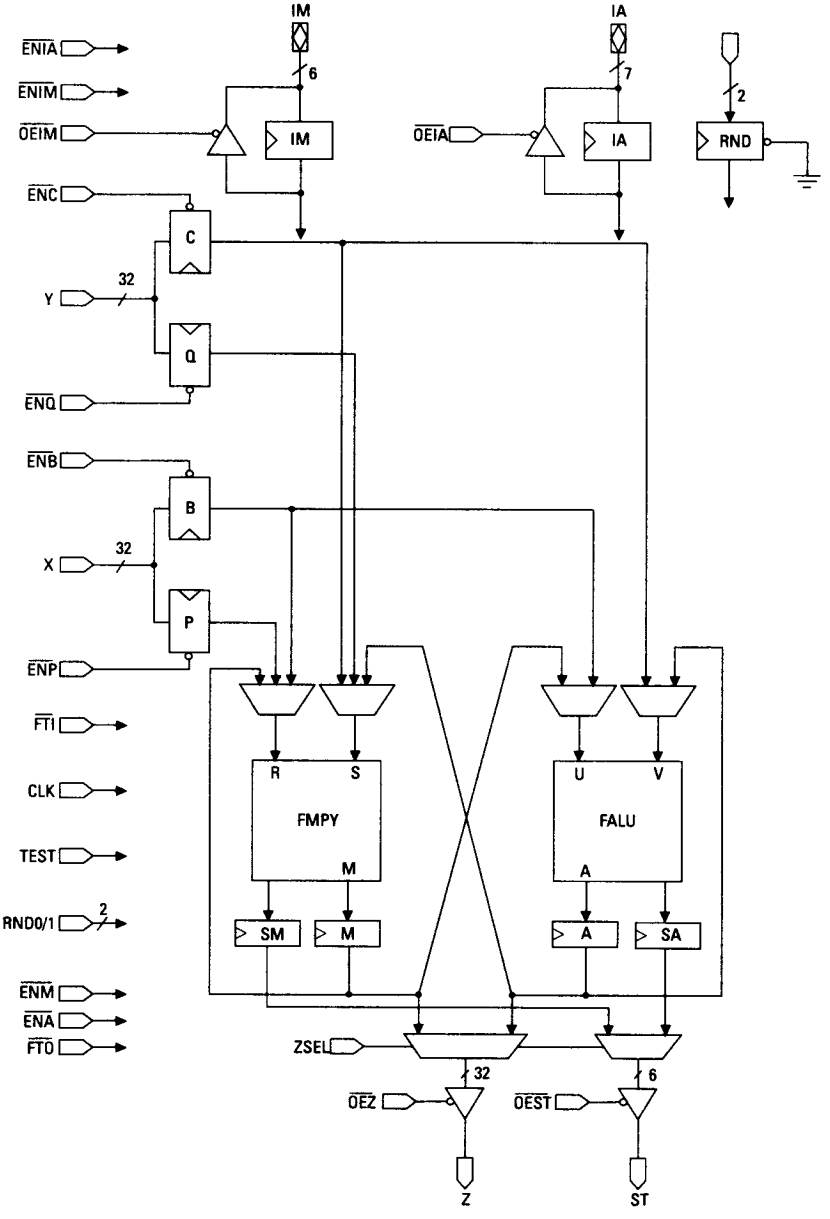
Features

- Provides separate 32-bit floating-point multiplier and floating-point ALU on a single chip
- Fully supports all boundary conditions of the IEEE format except operations with denormalized numbers, which are treated as zero
- Three-bus architecture for high throughput
- Separate register enable signals
- Fast cycle times

Commercial	Military
50 ns	60 ns
60 ns	80 ns
80 ns	100 ns

- No internal pipelines for high throughput with low latency
- Architecture optimized for sum of products and product of sums calculations
- All input registers can be selected as edge-triggered flip-flops or level-triggered latches
- All output registers can be selected as edge-triggered flip-flops or transparent buffers
- Single master clock
- Four separate input registers
- Provides conversion from integer to floating-point and from floating-point to integer formats
- Performs (2 minus X) for Newton-Raphson division
- Special graphics operation such as Min and Max
- Full serial scan test mode for all input and output registers eases board and system level testing

Block Diagram



Architecture

The L64133 has two separate processing sections–the Floating-Point Multiplier (FMPY), and the Floating-Point ALU (FALU). Each of these sections has separate instruction inputs and can operate fully independently of each other. Neither the FMPY nor the FALU are internally pipelined, thus providing high throughput with low latency.

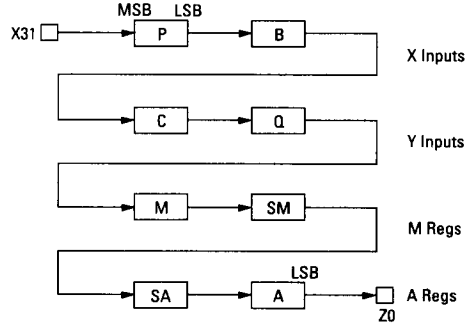
The device contains a total of six data registers (four input and two output). There are also two instruction registers, and two status registers (one of each for the FMPY and FALU). Input data and instruction registers can operate as either edge-triggered master-slave flip-flops, or as level-triggered latches. These register modes are controlled by $\overline{FTI}$. Output data and status registers can operate as either edge-triggered flip-flops, or as completely transparent buffers. These register modes are controlled by $\overline{FTO}$.

The L64133 is designed so that either processor can be fed data from any input data bus. This flexibility and the lack of internal pipelines is the key to fast solutions to complicated problems such as multiplication of complex numbers or matrices.

The output of the chip is controlled by ZSEL. This selects the results residing in either the M and SM or A and SA registers. Both the Z data output and ST status output are 3-stated.

The L64133 supports IEEE single precision format. IEEE denormalized numbers are treated as zero.

L64133 Test Mode Scan Path Diagram (TEST = HIGH)



Note: In each register the path is from MSB to LSB.

L64133 Operations Supported

NOP	No Operation
MUL	Floating-Point Multiplication
PASS	Pass input data
NRS	(2 - X) for Newton-Raphson division
ADD	Floating-Point Addition
NEG	Negation
SUB	Floating-Point Subtraction
MIN	Comparison yields Minimum
MAX	Comparison yields Maximum
12F	Integer to Floating-Point format conversion
F21	Floating-Point to Integer format conversion

Pin Listing and Description

X0:31
X operand input bus.

Y0:31
Y operand input bus.

Z0:31
Z result 3-state output bus.

CLK
Clock input. Operates the registers as edge-triggered flip-flops when $\overline{FTI}$ and/or $\overline{FTO}$ are HIGH.

$\overline{FTI}$
Flowthrough control for all input registers. When $\overline{FTI}$ is HIGH all input registers (P, Q, B, C IM and IA) act as edge-triggered flip-flops under control of the CLK and the input register enables. Data is loaded into the registers at the rising edge of CLK when the enable for a given register is LOW.

When $\overline{FTI}$ is LOW, all input registers act as level-triggered latches under control of the individual active-LOW input enables for each register. When an enable is LOW, the latches become transparent and data flows through. When an enable is HIGH, the register is not transparent and previous data is held.

$\overline{FTO}$
Flowthrough control for all output registers. When FTO is HIGH, all output registers (M, A, SM and SA) act as edge-triggered flip-flops under control of the CLK, ENM (for M and SM registers) and ENA (for A and SA registers). Data is loaded into the registers at the rising edge of CLK when the enable for a given register is LOW.

When $\overline{FTO}$ is LOW, all output registers (M, SM, A, and SA) become completely transparent. They act as simple buffers regardless of $\overline{ENM}$ and $\overline{ENA}$.

$\overline{ENP}$, $\overline{ENQ}$, $\overline{ENB}$, $\overline{ENC}$, $\overline{ENIM}$, $\overline{ENIA}$
Input Register Enables (for the P, Q, B, C, IM and IA registers). When $\overline{FTI}$ is HIGH (registers act as edge-triggered flip-flops) and an input enable is LOW, data will be clocked into the register at the rising edge CLK. When an input enable is HIGH, the new data input is disabled and previous data is maintained in the register.

When $\overline{FTI}$ is LOW (registers act as level-triggered latches) and an input enable is LOW, the register is transparent. Previous data is held in the register when an input enable is HIGH.

$\overline{ENM}$, $\overline{ENA}$
Output Register Enables for the M and SM, A and SA registers. When $\overline{FTO}$ is HIGH (registers act as edge-triggered flip-flops) and ENM or ENA is LOW, data and status bits will be clocked into the data and status registers at the rising edge of CLK. When $\overline{ENM}$ or $\overline{ENA}$ is HIGH, the new data input is disabled and previous data is maintained in the data and status registers.

When $\overline{FTO}$ is LOW, all output registers (M, SM, A, and SA) become competely transparent. They act as simple buffers regardless of $\overline{ENM}$ and $\overline{ENA}$.

ST0:5
Multiplexed status port for the FMPY and FALU. When ZSEL is LOW, status information contained in the SM register is available at the ST output. When ZSEL is HIGH, status information contained in the SA register is available at the ST output. The status bits ST0:5 are for zero (ZER), not-a-number (NaN), inexact (INE), underflow (UNF), overflow (OVF), and invalid (INV) from ST0 to ST5, respectively.

IM0:5
Bidirectional Instruction input for the FMPY. The instruction stored in the IM register can be read out of IM0:5 by holding $\overline{OEIM}$ LOW (for context switching). Source for the FMPY S bus is indicated by IM0:1. Source for the R bus is indicated by IM2:3 and the FMPY operation mode is indicated by IM4:5.

IA0:6
Bidirectional Instruction input for the FALU. The instruction stored in the IA register can be read out of IA0:6 by holding $\overline{OEIA}$ LOW (for context switching). Source for the FALU V bus is indicated by IA0. Source for the U bus is indicated by IA1. FALU operation mode is indicated by IA2:6 with IA6 indicating an absolute value operation.

RND0:1
RND0 and RND1 inputs are applied to an RND register which sets the rounding mode for the device. This register is permanently enabled. See section on Rounding Mode Select for definition of rounding modes.

Pin Listing and Description (Continued)

$\overline{OEIM}$
Bidirectional output control for the IM port. When $\overline{OEIM}$ is HIGH, input data at the IM port is available to the IM register. When $\overline{OEIM}$ is LOW, contents of the IM register are available at the IM port.

$\overline{OEIA}$
Bidirectional output control for the IA port. When $\overline{OEIA}$ is HIGH, input data at the IA port is available to the IA port is available to the IA register. When $\overline{OEIA}$ is LOW, contents of the IA registers are available at the IA port.

ZSEL
Output Register Select. If ZSEL is LOW, the data contained in register M is placed at the Z output while the status information contained in SM is placed at the ST output. If ZSEL is HIGH, data in register A is placed at the Z output bus while status in SA is made available at the ST output.

$\overline{OEZ}$
Active-LOW 3-state control for the Z output.

$\overline{OEST}$
Active-LOW 3-state control for the ST output.

TEST
When TEST is HIGH, all input and output data registers are placed into a single long serial scan chain. This mode is useful for board and system level testing.

Input Register Operation (P, Q, B, C, IM, IA)

$\overline{FTI}$	Input Register Enable	CLK	Input Register Mode	
0	0	X	Latch transparent, data feeds through	Level-Triggered (Latch)
0	1	X	Latch retains previous state	
1	0	↑	New data loaded into register	Edge-Triggered (Flip-Flop)
1	0	0, 1	Register retains previous state	
1	1	X	Register retains previous state	

Output Register Operation (M, SM, A, SA)

$\overline{FTO}$	Output Register Enable	CLK	Output Register Mode	
0	X	X	Data feeds through	Transparent Data Buffer
1	0	↑	New data loaded into register	Edge-Triggered (Flip-Flop)
1	0	0, 1	Register retains previous state	
1	1	X	Register retains previous state	

Multiplier Instructions (IM)

The IM0:5 input is divided into three separate instruction fields, Source R, Source S and operation. Each of these fields is two bits in length.

Source: The FMPY can receive input data from any of the four input registers as well as the M-register (FMPY result) or A-register (FALU result). The P-register, B-register and M-register can be placed onto the R-bus. The Q-register, C-register and A-register can be placed onto the S-bus.

Operation: The FMPY performs one arithmetic operation (to multiply R x S). Also included is the ability to pass R, pass S and a NOP instruction.

When $\overline{FTO}$ is HIGH and the FMPY operation is a NOP, the M and SM registers will retain previous data regardless of $\overline{ENM}$.

The IM register is read-writable. That is, the instruction stored in the IM register can be read out of the IM port by holding the $\overline{OEIM}$ input LOW. This is useful during context switching and other operations.

The PASS operation in the FMPY is completely transparent, ie input exceptions will not be flagged.

Multiplier Instruction Format

	OP Code		Source R		Source S	
IM	5	4	3	2	1	0

Op Code

IM5	IM4	Operation	
0	0	NOP	No Operation
0	1	MUL	Multiply R x S
1	0	PASS (R)	Pass R
1	1	PASS (S)	Pass S

Source R

IM3	IM2	Source R
0	0	P-Register
0	1	B-Register
1	X	M-Register

Source S

IM1	IM0	Source S
0	0	Q-Register
0	1	C-Register
1	X	A-Register

ALU Instructions (IA)

The 7-bit IA0:6 FALU instruction input is divided into three fields. Source U (IA1), Source V (IA0) and Op Code (IA2:6).

Source: The FALU can receive input data from the B or C-registers as well as the M-register (FMPY result) or A-register (FALU result). The B and M-registers can be placed onto the U-bus while the C and A-registers can be placed onto the V-bus.

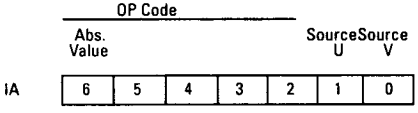
Operation: The FALU provides 16 basic operations including addition, subtraction, negation, pass, min, max, conversion to and from integer and 2 - X (for Newton-Raphson division) as well as signed or absolute value. A single instruction bit (IA6) controls the absolute value operation.

When $\overline{FTO}$ is HIGH and the FALU operation is a NOP, the A and SA registers will retain previous data regardless of ENA.

The IA register is read-writable. That is, the instruction stored in the IA register can be read out of the IA port by holding the $\overline{OE}$IA input LOW. This is useful during context switching and other operations.

For the PASS and NEG operations in the FALU, the input is examined as an ordinary floating-point number. Therefore input exceptions will be flagged and denormalized numbers will be flushed to zero.

ALU Instruction Format



Normal Operation (IA6 = 0) Op Codes

IA6	IA5	IA4	IA3	IA2	Operation
0	0	0	0	0	NOP
0	0	0	0	1	NRS(U)
0	0	0	1	0	NRS(V)
0	0	0	1	1	ADD
0	0	1	0	0	PASS(U)
0	0	1	0	1	NEG(U)
0	0	1	1	0	PASS(V)
0	0	1	1	1	NEG(V)
0	1	0	0	0	SUB(U - V)
0	1	0	0	1	SUB(V - U)
0	1	0	1	0	MIN(U,V)
0	1	0	1	1	MAX(U,V)
0	1	1	0	0	12F(U)
0	1	1	0	1	12F(V)
0	1	1	1	0	F21(U)
0	1	1	1	1	F21(V)

Absolute Value Operation (IA = 1) Op Codes

IA6	IA5	IA4	IA3	IA2	Operation
1	0	0	0	0	NOP
1	0	0	0	1	| NRS(U) |
1	0	0	1	0	| NRS(V) |
1	0	0	1	1	| ADD |
1	0	1	0	0	| PASS(U) |
1	0	1	0	1	| NEG(U) |
1	0	1	1	0	| PASS(V) |
1	0	1	1	1	| NEG(V) |
1	1	0	0	0	| SUB(U - V) |
1	1	0	0	1	| SUB(V - U) |
1	1	0	1	0	| MIN(U,V) |
1	1	0	1	1	| MAX(U,V) |
1	1	1	0	0	| 12F(U) |
1	1	1	0	1	| 12F(V) |
1	1	1	1	0	Reserved Operation
1	1	1	1	1	Reserved Operation

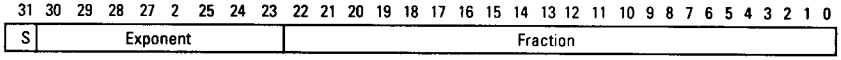
Source U

IA1	Source U
0	B-Register
1	M-Register

Source V

IA0	Source V
0	C-Register
1	A-Register

IEEE Single Precision Floating-Point Format



Features

- Bit <31> is the sign bit
- Bits <30:23> are an excess 127 (biased) binary exponent
- Bits <22:0> are a normalized 24-bit fraction with the redundant most significant integer bit (1.0...) not represented (hidden bit)
- A zero value is indicated by a zero fraction with zero exponent. The zero value can be positive or negative
- Infinity is indicated by a zero fraction with a one's filled exponent (255_{10}). Can be positive or negative
- A reserved operand known as not-a-number (NaN) is represented by one's filled exponent (255_{10}) and a non-zero fraction. The two types of NaNs called signaling NaN and quiet NaN are discussed below

Not-a-Number

A signaling NaN (sNaN) is indicated by a fraction with a 1 in the MSB and X everywhere else. Signaling NaNs are generally useful for indicating uninitialized variables, or for implementing user-designed extensions to the operations provided. A signaling NaN is never produced as the final result of an operation.

A quiet NaN (qNaN) is indicated by a fraction with a 0 in the MSB and at least one 1 elsewhere in the fraction. Quiet NaNs are generated for invalid operations. When they appear as an input operand, they are generally passed through (without setting the INV flag). Thus, quiet NaNs are useful as flags or to pass a "marker" through a series of operations.

IEEE Format Boundries and Special Cases[1]

Operand	Sign	Fraction Exponent	Exponent (*f*22...*f*0)	Exponent Bias	Hidden Bit	Magnitude
Normalized Numbers:						$2^{e-127}(1.f)$
| NORM.MAX |	x	254	111...11	+127	1.0	$2^{127}(2-2^{-23})$
| NORM.MIN|	x	1	000...00	+127	1.0	2^{-126}
Denormalized[2] Numbers:	x	0	Non-Zero	+126	0	$2^{-126}(0.f)$
| DNRM.MAX |	x	0	111...11	+126	0	$2^{-126}(1-2^{-23})$
| DNRM.MIN |	x	0	000...01	+126	0	$2^{-126}(2^{-23})$
Special:						
Zero	x	0	0	_	0	±0
Signaling NaN	x	255	1xx...xx	_	_	_
Quiet NaN	x	255	0xx..xx[3]	_	_	_
Infinity	x	255	000...00	_	_	±∞

Notes:
1. Exponent, Exponent Bias and Magnitude values all represented in base 10 (decimal) format, x indicates a don't care.
2. The L64133 treats denormalized numbers as zero.
3. At least one of the 22 LSBs of a qNaN must be a 1 (see Not-a-Number above).

IEEE Numerical Representations

- Denormalized numbers are represented by a zero exponent and a non-zero fraction. These numbers are treated as zero by the L64133.

IEEE convention is as follows:
s = sign bit
e = exponent
f = fraction

s	e	f	Value Equation	Value
x	0	0	$(-1)^{s}*(0)$	+0, -0
x	0	≠0		Denormalized number
x	0 < e < 255	x	$(-1)^{s}*(2^{e-127})*(1.f)$	Normalized number
x	255	0	$(-1)^{s}*(\infty)$	+ ∞, - ∞
x	255	≠0		NaN (Not-a-Number)

Integer Data Type Longword (32-Bits)

31

S	Two's Complement Integer

Features

- Two's complement format
- Bit < 31 > is the sign bit
- Order from least to most significant is from bit < 0 > through bit < 30 >

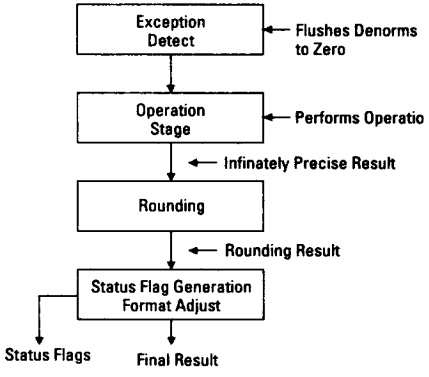
Rounding Mode Select

RND1	RND0	Mode
0	0	Round to nearest (unbiased)
0	1	Round toward - ∞
1	0	Round toward + ∞
1	1	Round toward zero

Rounding

There are four rounding modes supported by the L64133 controlled by RND0:1. These are: round to nearest, round toward + ∞, round toward - ∞ and round toward zero. In the case where the infinitely precise result is exactly halfway between two representable values, round to nearest mode will round to the value whose LSB is 0 (unbiased round).

L64133 Multiplier and ALU Internal Architecture



Status (ST) Output

INV	OVF	UNF	INE	NaN	ZER
ST5	ST4	ST3	ST2	ST1	ST0

The status (ST0:5) output displays the status of the FMPY (contained in register SM) when ZSEL is LOW or of the FALU (contained in register SA) when ZSEL is HIGH.

FALU Operations (±0.0) ± (±0.0)

There are three status flags for FALU operations of {(±0.0) ± (±0.0)}, that should be noted. In all rounding modes, the ST.0 (ZER) flag is 0, the ST.2 (INE) flag is 1, and the ST.3 (UNF) flag is 1 for these particular operations.

Ordinarily, the output result, Z, is (±0,0) for these operations. However for {(+0.0) + (0.0)} when the rounding mode is +∞, the result will be + NORM.MIN (the minimum normalized number). For {(-0.0) + (-0.0)} and {(-0.0) - (+0.0)} when the rounding mode is -∞, the result will be -NORM.MIN.

FMU Underflow Operations

When the infinitely precise result of a multiply operation falls within the range $\pm(1.0 \times 2^{-127}, 1.0 \times 2^{-126})$ and the rounding mode is nearest, the L64133 returns ±NORM.MIN and clears the UNF and ZER flags. However, when the infinitely precise result is in the range $\pm(0.0, 1.0 \times 2^{-127})$ and the rounding mode is nearest, the L64133 returns ±0.0 and sets the UNF and ZER flags. In both cases the INE flag will be set.

Definition of Status Flags

Invalid (INV)
If an Invalid operation is performed, the INV flag will be set HIGH. These operations are listed in the Invalid Operations table.

Overflow (OVF)
If an operation performed on finite operands produces a rounded result which is too large to fit in the destination format, an overflow is said to have occurred. The result will be indicated as $\pm\infty$ or $\pm$ | NORM.MAX | (depending on sign and rounding mode), and both the OVF and INE flags will be set HIGH.

An overflow may also occur when an integer conversion is attempted on a number larger than 2^{31} -1 or smaller thean -2^{31}. The INV flag will be HIGH while the OVF and INE flags will be LOW.

Underflow (UNF)
If an operation produces a result which is too small to be expressed as a normalized floating-point number but larger than zero, an underflow is said to have occurred. The result will be indicated as zero ($\pm$0) or | NORM.MIN | (depending on sign and rounding mode), and the UNF and INE flags will be set HIGH.

Inexact (INE)
If an operation produces a result which, after rounding, is not equal to the "infinitely precise result" an inexact operation is said to have occurred and the INE flag is set HIGH. The INE flag will also be set HIGH on an underflow or overflow.

Not-a-Number (NaN)
A NaN is defined as either a quiet NaN (qNaN) or a signaling NaN (sNaN). When an operation is performed where a NaN is used as an input or appears as an output, the NaN flag will be set HIGH.

Zero (ZER)
If an operation is perform, which produces a rounded result of zero ($\pm$0), the ZER flag will usually be set HIGH. For SUB operations where U,V have the same valve, the ZER flag will not be set.

Invalid Operations

FMPY or FALU	Operation	Single or Dual Input Operands	Result
FMPY	MUL	sNaN	qNaN
	MUL	Denorm, $\pm\infty$	qNaN
	MUL	0, $\pm\infty$	qNaN
FALU	NRS, ADD, SUB	sNaN	qNaN
	ADD	$+\infty$, $-\infty$	qNaN
	SUB	$+\infty$, $+\infty$	qNaN
	SUB	$-\infty$, $-\infty$	qNaN
FALU	F21	$> 2^{31} - 1$	$7FFFFFFF_{16}$
	F21	$< -2^{31}$	80000000_{16}

Flag Summary

Operation	Condition(s)	INV	OVF	UNF	INE	NaN	ZER
Any operation listed in Invalid Operations table, that produces a NaN		1	0	0	0	1	0
Any operation	One or both operand/s is qNaN	0	0	0	0	1	0
ADD, SUB, NRS, MUL	Input operands are finite and | rounded result | $\geq 2^{128}$	0	1	0	1	0	0
ADD, SUB, NRS, MUL	$0 <$ | rounded result | $\geq 2^{-126}$	0	0	1	1	0	X
ADD, SUB, NRS, F21, MUL	Input operands are normal and final result does not equal infinitely precise result	0	X	X	1	0	X
ADD, SUB, MUL	Final result is zero	0	0	X	X	0	1

Note: "X" indicates that the status flag is determined by the definitions given in the text.

L64133 AC Switching Characteristics - Commercial Conditions: TA = 0°C to 70°C, VDD = 4.75 V to 5.25 V

Symbol	Description	L64133-50		L64133-60		L64133-80		Reference Timing Diagram
		Min	Max	Min	Max	Min	Max	
tFLOP	Floating-point operation time	50		60		80		4, 5
tSD	Input data setup time	6		8		10		2, 4
tHD	Input data hold time	3		3		4		2, 4
tSDL	Input data setup time relative to latch	10		12		14		1, 3
tHDL	Input data hold time relative to latch	5		6		7		1, 3
tSI	Input register enable setup time	6		8		10		2, 4
tHI	Input register enable hold time	3		3		4		2, 4
tSO	Output register enable setup time	6		7		9		3, 4
tHO	Output register enable hold time	1		1		1		3, 4
tSEL	Setup time input register enable LOW	58		70		95		3
tHEH	Hold time input register enable HIGH	0		0		0		3
tDELAY	Output delay time from input register		75	20	80	20	105	1, 2
tOD	Output delay time from clock	9	21	9	25	9	33	3, 4, 5
tZSEL	Output delay time from ZSEL	7	17	7	20	7	25	5
tPWLE	Min pulse width LOW, input reg enable	13		15		20		1, 3
tPWH	Min pulse width HIGH, clock	9		10		14		5
tPWL	Min pulse width LOW, clock	9		10		14		5
tOZ	Output disable		13		15		20	5
tOE	Output enable time		13		15		20	5
tBI	Bidirect input mode enable time		13		15		20	5
tBO	Bidirect output mode enable time		13		15		20	5

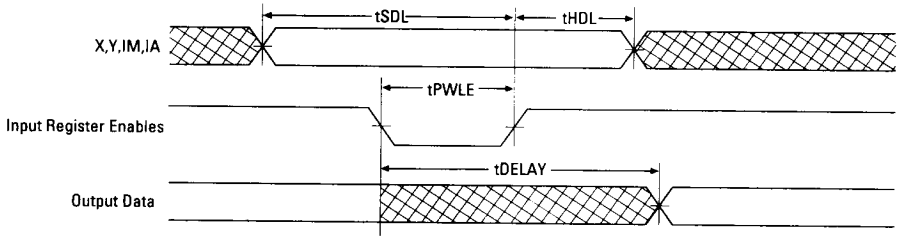
All units are in ns, output loading = 50 pF

L64133 AC Switching Characteristics - Military Conditions: TA = -55°C to 125°C, VDD = 4.5 V to 5.5 V

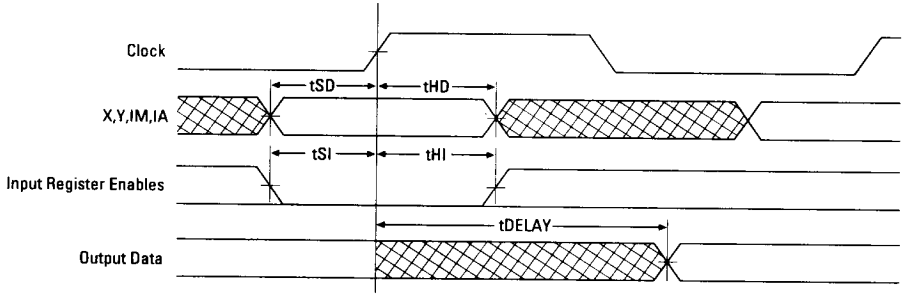
Symbol	Description	L64133-60		L64133-80		L64133-10		Reference Timing Diagram
		Min	Max	Min	Max	Min	Max	
tFLOP	Floating-point operation time	60		80		100		4, 5
tSD	Input data setup time	8		10		12		2, 4
tHD	Input data hold time	3		4		5		2, 4
tSDL	Input data setup time relative to latch	12		14		16		1, 3
tHDL	Input data hold time relative to latch	6		7		8		1, 3
tSI	Input register enable setup time	8		10		12		2, 4
tHI	Input register enable hold time	3		4		5		2, 4
tSO	Output register enable setup time	7		9		12		3, 4
tHO	Output register enable hold time	1		1		1		3, 4
tSEL	Setup time input register enable LOW	70		95		115		3
tHEH	Hold time input register enable HIGH	0		0		0		3
tDELAY	Output delay time from input register	20	80	20	90	20	105	1, 2
tOD	Output delay time from clock	7	25	7	33	7	42	3, 4, 5
tZSEL	Output delay time from ZSEL	4	20	4	25	4	30	5
tPWLE	Min pulse width LOW, input reg enable	15		20		25		1, 3
tPWH	Min pulse width HIGH, clock	10		14		17		5
tPWL	Min pulse width LOW, clock	10		14		17		5
tOZ	Output disable		15		20		25	5
tOE	Output enable time		15		20		25	5
tBI	Bidirect input mode enable time		15		20		25	5
tBO	Bidirect output mode enable time		15		20		25	5

All units are in ns, output loading = 50 pF

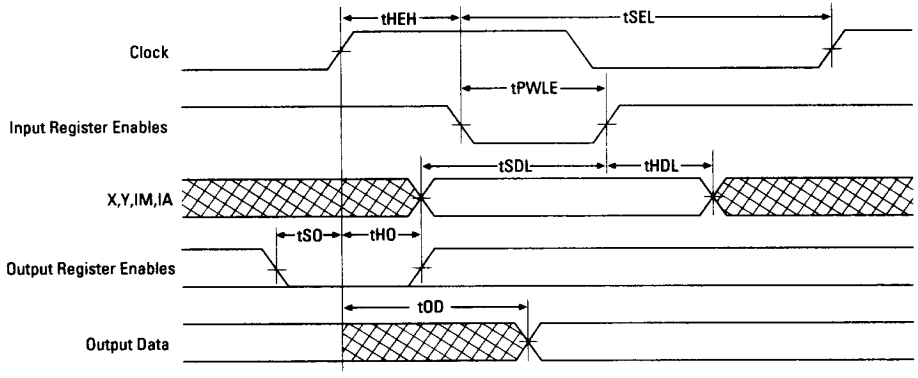
L64133 Timing Diagram #1
($\overline{FTI}$ = $\overline{FTO}$ = 0) Input registers are level-triggered (latches), output registers are transparent buffers



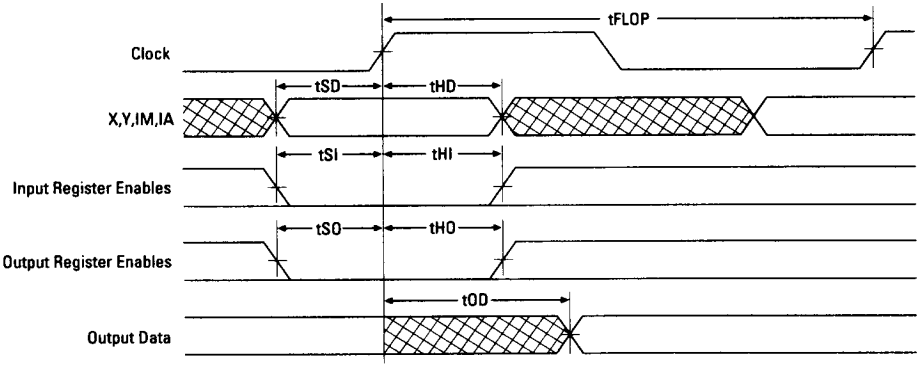
L64133 Timing Diagram #2
($\overline{FTI}$ = 1, $\overline{FTO}$ = 0) Input registers are edge-triggered (flip-flops), output registers are transparent buffers



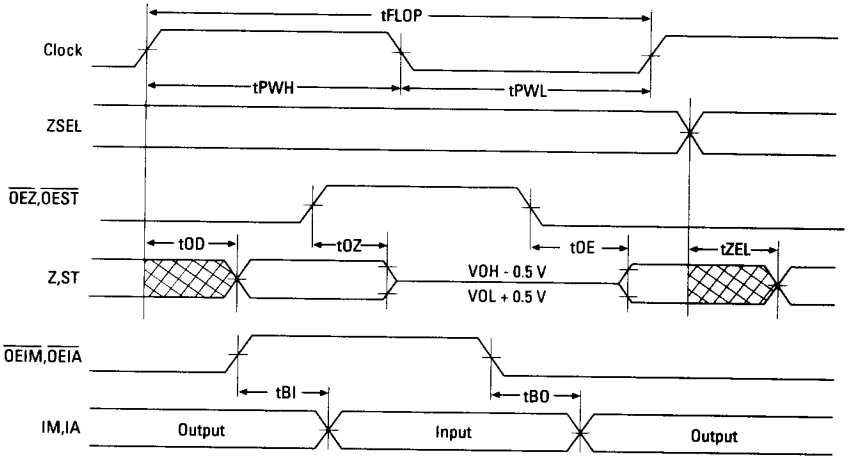
L64133 Timing Diagram #3
($\overline{FTI}$ = 0, $\overline{FTO}$ = 1) Input registers are level-triggered (latches), output registers are edge-triggered (flip-flops)



L64133 Timing Diagram #4
($\overline{FTI}$ = $\overline{FTO}$ = 1) Both input and output registers are edge-triggered (flip-flops)



L64133 Timing Diagram #5
General timing for all I/O modes (Clock applies when appropriate)



Operating Characteristics

Absolute Maximum Ratings (Referenced to GND)

Parameter	Symbol	Limits	Unit
DC supply voltage	VDD	-0.3 to + 7	V
Input voltage	VIN	-0.3 to VDD + 0.3	V
DC input current	IIN	±10	mA
Storage temperature range	TSTG	-65 to + 150	°C

Recommended Operating Conditions

Parameter	Symbol	Limits	Unit
DC supply voltage	VDD	+3 to + 6	V
Operating ambient Temperature range Military	TA	-55 to +125	°C
Commercial range	TA	0 to +70	°C

DC Characteristics: Specified at VDD = 5 V over the specified temperature and voltage ranges [1]

Symbol	Parameter	Condition			Min	Typ	Max	Units
VIL	LOW level input voltage						0.8	V
VIH	HIGH level input voltage Commercial temperature range Military temperature range				2.0 2.25			V V
IIN	Input current	VIN = VDD			-100	-30	-8	µA
VOH	HIGH level output voltage		Comm	Mil				
		IOH =	-4 mA	-3.2 mA	2.4	4.5		V
VOL	LOW level output voltage		Comm	Mil				
		IOL =	4 mA	3.2 mA		0.2	0.4	V
IOZ	3-State output leakage current	VOH = VSS or VDD			-10	±1	10	µA
IOS	Output short circuit current[2]	VDD = Max, VO = VDD			15		130	mA
		VDD = Max, VO = OV			-5		-100	mA
IDDQ	Quiescent supply current	VIN = VDD or VSS					1	mA
IDD	Operating supply current	tCYCLE = 80 ns				200		mA
CIN	Input capacitance	Any input				5		pF
COUT	Output capacitance	Any output				10		pF

Notes:
1. Military temperature range is -55°C to + 125°C, ±10% power supply; commercial temperature range is 0°C to 70°C, ±5% power supply.
2. Not more than one output should be shorted at a time. Curation of short circuit test must not exceed one second.

Applications Examples

Multiply-Accumulate (a x b) + (c x d) + (e x f)
Fully Clocked Operation $\overline{FTI} = \overline{FTO} = 1$

Clock	Instruction Inputs		Data Inputs		Register Contents								Outputs
Cycle	IM	IA	X	Y	IM	IA	P	Q	B	C	M	A	Z,ST
0	MUL P, Q		a	b	–	–	–	–	–	–	–		
1	MUL P, Q	PASS M	c	d	MUL P, Q	–	a	b	–	–	–		
2	MUL P, Q	ADD A, M	e	f	MUL P, Q	PASS M	c	d	–	–	a x b		
3	–	ADD A, M			MUL P, Q	ADD A, M	e	f	–	–	c x d	(a x b)	(a x b)
4	–	–				ADD A, M	–	–	–	–	e x f	(a x b) + (c x d)	(a x b) + (c x d)
5	–	–					–	–	–	–	–	(a x b) + (c x d) + (e x f)	(a x b) + (c x d) + (e x f)

4 x 4 Transformation

$$\begin{bmatrix} a11 & a12 & a13 & a14 \\ a21 & a22 & a23 & a24 \\ a31 & a32 & a33 & a34 \\ a41 & a42 & a43 & a44 \end{bmatrix} \quad \begin{bmatrix} x \\ y \\ z \\ w \end{bmatrix} = \begin{bmatrix} x' \\ y' \\ z' \\ w' \end{bmatrix}$$

Clock	Instruction Inputs		Data Inputs		Register Contents								Outputs
Cycle	IM	IA	X	Y	IM	IA	P	Q	B	C	M	A	Z,ST
0	MUL B, C		a11	X									
1	MUL B, Q	PASS M	a12	Y	MUL B, C				a11	X			
2	MUL B, C	ADD M, A	a13	Z	MUL B, Q	PASS M		y	a12		a11 x X		
3	MUL B, C	ADD M, A	a14	W	MUL B, C	ADD M, A			a13	Z	a12 x Y	a11 x X	
4	MUL B, C	ADD M, A	a21	X	MUL B,C	ADD M, A			a14	W	a13 x Z	(a11 x X) + (a12 x Y)	
5	MUL B, Q	PASS M	a22		MUL B, C	ADD M, A			a21	X	a14 x W	(a11 x X) + (a12 x Y) + (a13 x Z)	
6	MUL B, C	ADD M, A	a23	Z	MUL B, Q	PASS M			a22		a21 x X	(a11 x X) + (a12 x Y) + (a13 x Z) + (a14 x W)	X'
7	MUL B, C	ADD M, A	a24	W	MUL B, C	ADD M, A			a23	Z	a22 x Y	a21 x X	
8	MUL B, C	ADD M, A	a31	X	MUL B, C	ADD M, A			a24	W	a23 x Z	(a21 x X) + (a22 x Y)	
9	MUL B, Q	PASS M	a32		MUL B, C	ADD M, A			a31	X	a24 x W	(a21 x X) + (a22 x Y) + (a23 x Z)	
10	MUL B, C	ADD M, A	a33	Z	MUL B, Q	PASS M			a32		a31 x X	(a21 x X) + (a22 x Y) + (a23 x Z) + (a24 x W)	Y'
11	MUL B, C	ADD M, A	a34	W	MUL B, C	ADD M, A			a33	Z	a32 x Y	a31 x X	
12	MUL B, C	ADD M, A	a41	X	MUL B, C	ADD M, A			a34	W	a32 x Z	(a31 x X) + (a32 x Y)	
13	MUL B, Q	PASS M	a42		MUL B, C	ADD M, A			a41	X	a34 x W	(a31 x X) + (a32 x Y) + (a33 x Z)	
14	MUL B, C	ADD M, A	a43	Z	MUL B, Q	PASS M			a42		a41 x X	(a31 x X) + (a32 x Y) + (a33 x Z) + (a34 x W)	Z'
15	MUL B, C	ADD M, A	a43	W	MUL B, C	ADD M, A			a43	Z	a42 x Y	a41 x X	
16					MUL B, C	ADD M, A			a44	W	a43 x Z	(a41 x X) + (a42 x Y)	
17					MUL B, C	ADD M, A			a41		a44 x W	(a41 x X) + (a42 x Y) + (a43 x Z)	
18												(a41 x X) + (a42 x Y) + (a43 x Z) + (a44 x W)	W'

Applications Examples
(Continued)

Complex Multiply (a + jb) (c + jd)

Clock	Instruction Inputs		Data Inputs		Register Contents								Outputs
Cycle	IM	IA	X	Y	IM	IA	P	Q	B	C	M	A	Z,ST
0	MUL P, Q		a	c	–	–	–	–	–	–	–	–	
1	MUL B, C	PASS M	b	d	MUL P, Q	–	a	c	–	–	–	–	
2	MUL P, C	SUB A, M			MUL B, C	PASS M	a	c	b	d	a x c	–	
3	MUL Q, B	PASS, M			MUL P, C	SUB A, M	a	c	b	d	b x d	a x c	
4		ADD A, M			MUL Q, B	PASS, M	–	c	b	–	a x d	(a x c) - (b x d)	(a x c) - (b x d) (real part)
5	–	–				ADD A, M					b x c	a x d	
6	–	–									b x c	(a x d) + (b x c)	(a x d) + (b x c) (imaginary part)

Complex Multiply-Accumulate
(a + jb) (c + jd) (e + jf) (g + jh) (k + jl) (m + jn)

Clock	Instruction Inputs		Data Inputs		Register Contents								Outputs
Cycle	IM	IA	X	Y	IM	IA	P	Q	B	C	M	A	Z,ST
0	MUL P, Q		a	c									
1	MUL B, C	PASS M	b	d	MUL P, Q		a	c					
2	MUL P, Q	SUB A, M	e	g	MUL B, C	PASS M	a	c	b	d	a x c		
3	MUL B, C	ADD A, M	f	h	MUL P, C	SUB A, M	e	g	b	d	b x d	a x c	
4	MUL P, Q	SUB A, M	k	m	MUL B, C	ADD A, M	e	g	f	h	e x g	(a x c) - (b x d)	
5	MUL B, C	ADD A, M	l	n	MUL P, C	SUB A, M	k	m	f	h	f x h	(a x c) - (b x d) + (e x g)	
6	MUL P, Q	SUB A, M	a	d	MUL B, C	ADD A, M	k	m	l	n	k x m	(a x c) - (b x d) + (e x g) - (f x h)	
7	MUL B, C	PASS M	b	c	MUL P, Q	SUB A, M	a	d	l	n	l x n	(a x c) - (b x d) + (e x g) - (f x h) + (k x m)	
8	MUL P, Q	ADD A, M	e	h	MUL B, C	PASS M	a	d	b	c	a x d	(a x c) - (b x d) + (e x g) - (f x h) + (k x m) - (l x n)	(a x c) - (b x d) + (e x g) - (f x h) + (k x m) - (l x n) (real part)
9	MUL B, C	ADD A, M	f	g	MUL P, Q	ADD A, M	e	h	b	c	b x c	a x d	
10	MUL P, Q	ADD A, M	k	n	MUL B, C	ADD A, M	e	h	f	g	e x h	(a x d) + (b x c)	
11	MUL B, C	ADD A, M	l	m	MUL P, Q	ADD A, M	k	n	f	g	f x g	(a x d) + (b x c) + (e x h)	
12		ADD A, M			MUL B, C	ADD A, M	k	n	l	m	k x n	(a x d) + (b x c) + (e x h) + (f x g)	
13						ADD A, M			l	m	l x m	(a x d) + (b x c) + (e x h) + (f x g) + (k x n) + (l x m)	(a x d) + (b x c) + (e x h) + (f x g) + (k x n) + (l x m) (imaginary part)

L64133 Floating-Point Processor Bonding Diagram–144-Pin CPGA

Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	Y17	Y13	Y9	Y8	Y6	Y2	Y1	X31	X29	X28	X25	X22	X20	X17	X15
B	Y19	Y16	Y12	Y10	Y7	Y4	Y3	X30	X26	X24	X21	X18	X16	X14	X11
C	Y22	Y18	Y15	Y14	Y11	Y5	Y0	VDD	X27	X23	X19	GND	X13	X10	X7
D	Y24	Y20	GND	X	← Orientation Pin								X12	X8	X6
E	Y27	Y23	Y21										X9	X5	X4
F	Y30	Y26	Y25										X3	X2	X0
G	Y31	Y28	Y29										$\overline{ENB}$	X1	$\overline{ENP}$
H	$\overline{ENC}$	$\overline{ENQ}$	CLK										TEST	NC	$\overline{FTI}$
J	IM5	IM3	$\overline{ENIM}$										IA5	IA4	$\overline{ENIA}$
K	IM4	IM2	IM1										IA1	IA2	IA6
L	IM0	$\overline{OEIM}$	ST5										RND1	$\overline{OEIA}$	IA3
M	ZSEL	$\overline{OEST}$	ST2										GND	$\overline{ENA}$	IA0
N	OEZ	ST4	ST1	VDD	Z28	Z24	Z20	VDD	GND	Z11	Z5	Z2	Z1	$\overline{FTO}$	RND0
P	ST3	ST0	Z31	Z29	Z26	Z23	Z21	Z17	Z13	Z12	Z9	Z6	Z4	Z0	$\overline{ENM}$
Q	GND	Z30	Z27	Z25	Z22	Z19	Z18	Z16	Z15	Z14	Z10	Z8	Z7	Z3	VDD

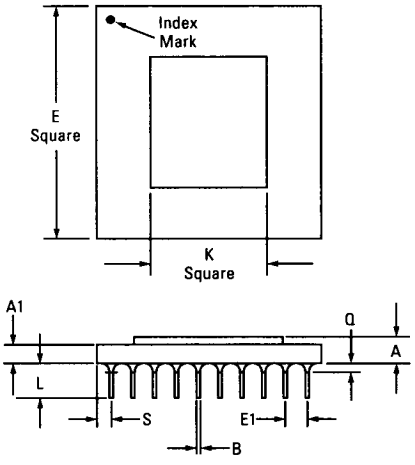
L64133 Ordering Information

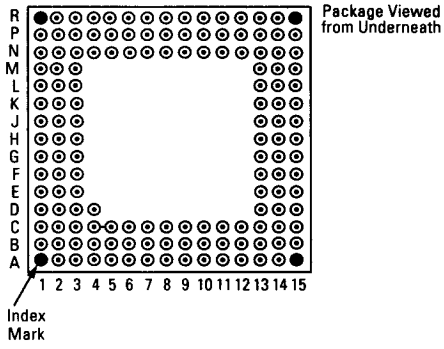
L64133 G M -XX

- **-XX** — Cycle Time
  - 50 = 50 ns
  - 80 = 80 ns
  - 10 = 100 ns
- **M** — Temperature Range/Flow Option
  - C = Commercial (0°C to 70°C)
  - M = Military (-55°C to + 125°C) Full MIL-STD-883C Level B
- **G** — Package Code
  - G = 144-Pin Ceramic Pin Grid Array
- **L64133** — Device Type
  - 32-Bit Floating-Point Processor

Packaging

144-Pin Ceramic Pin Grid Array





Note:
PGA pin numbering is with respect to the pins facing the viewer.

Dimensions		Inches (mm)
A	Max	0.115 (2.921)
A1	Ref	0.080 (2.032)
B	Min	0.016 (0.406)
	Max	0.020 (0.508)
E	Min	1.555 (39.50)
	Max	1.595 (40.51)
E1	Min	0.095 (2.413)
	Max	0.105 (2.667)
L	Min	0.170 (4.318)
	Max	0.190 (4.826)
Q	Ref	0.050 (1.270)
S	Ref	0.088 (2.235)
K	Ref	0.850 (21.59)