Integrated Device Technology, Inc.

CMOS SERIAL-TO-PARALLEL FIFO
2048 x 9-BIT
4096 x 9-BIT

IDT72132
IDT72142

T-46-35

FEATURES:

- 35ns parallel port access time, 45ns cycle time
- 50MHz serial port shift rate
- Expandable in depth and width with no external components
- Programmable word lengths including 8, 9, 16-18, and 32-36 bit using Flexshift™ serial input without using any additional components
- Multiple status flags: Full, Almost-Full (1/8 from full), Half-Full, Almost Empty (1/8 from empty), and Empty
- Asynchronous and simultaneous read and write operations
- Dual-port zero fall-through architecture
- Retransmit capability in single device mode
- Produced with high-performance, low-power CEMOS™ technology
- Available in a 28-pin ceramic, plastic DIP and 32-pin plastic leaded chip carrier (PLCC) packages
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

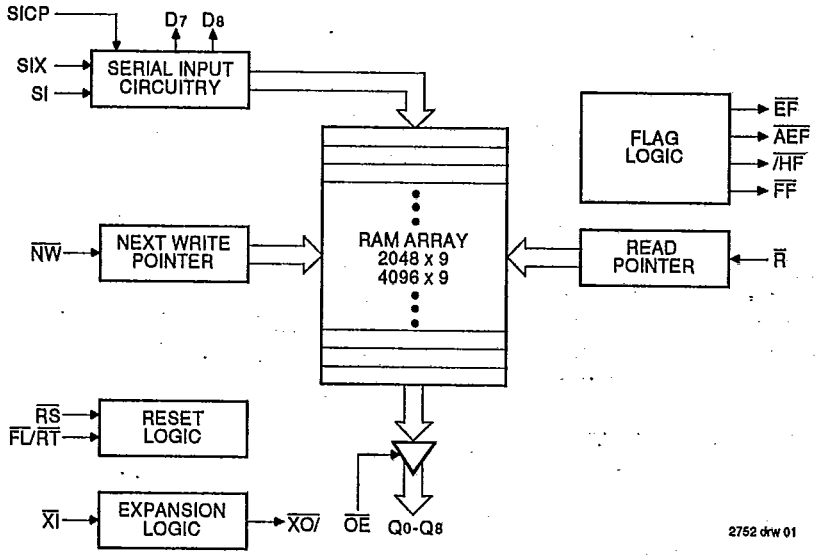
The IDT72132/72142 are high-speed, low-power serial-to-parallel FIFOs. These FIFOs are ideally suited to serial communications applications, tape/disk controllers, and local area networks (LANs). The IDT72132/72142 can be configured with the IDTs parallel-to-serial FIFOs (IDT72131/72141) for bidirectional serial data buffering.

The FIFO has a serial input port and a 9-bit parallel output port. Wider and deeper serial-to-parallel data buffers can be built using multiple IDT72132/72142 chips. IDTs unique Flexshift serial expansion logic (SIX, $\overline{NW}$) makes width expansion possible with no additional components. These FIFOs will expand to a variety of word widths including 8, 9, 16, and 32 bits. The IDT72132/142 can also be directly connected for depth expansion.

Five flags are provided to monitor the FIFO. The full and empty flags prevent any FIFO data overflow or underflow conditions. The Almost-Full (7/8), Half-Full, and Almost Empty (1/8) flags signal memory utilization within the FIFO.

The IDT72132/72142 is fabricated using IDTs high-speed submicron CEMOS technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



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PIN DESCRIPTIONS

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Symbol	Name	I/O	Description
SI	Serial Input	I	Serial data is shifted in least significant bit first. In the serial cascade mode, the Serial Input (SI) pins are tied together and SIX plus D7, D8 determine which device stores the data.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set low, internal READ and WRITE pointers are set to the first location of the RAM array. $\overline{HF}$ and $\overline{FF}$ go high, and $\overline{AEF}$, and $\overline{EF}$ go low. A reset is required before an initial WRITE after power-up. $\overline{R}$ must be high during an $\overline{RS}$ cycle.
$\overline{NW}$	Next Write	I	To program the Serial In word width , connect $\overline{NW}$ with one of the Data Set pins (D7, D8).
SICP	Serial Input Clock	I	Serial data is read into the serial input register on the rising edge of SICP. In both Depth and Serial Word Width Expansion modes, all of the SICP pins are tied together.
$\overline{R}$	Read	I	When READ is low, data can be read from the RAM array sequentially, independent of SICP. In order for READ to be active, $\overline{EF}$ must be high. When the FIFO is empty ($\overline{EF}$-low), the internal READ operation is blocked and Q0-Q8 are in a high impedance condition.
$\overline{FL/RT}$	First Load/ Retransmit	I	This is a dual purpose input. In the single device configuration ($\overline{XI}$ grounded), activating retransmit ($\overline{FL/RT}$-low) will set the internal READ pointer to the first location. There is no effect on the WRITE pointer. $\overline{R}$ must be high and SICP must be low before setting $\overline{FL/RT}$ low. Retransmit is not possible in depth expansion. In the depth expansion configuration, $\overline{FL/RT}$ grounded indicates the first activated device.
$\overline{XI}$	Expansion In	I	In the single device configuration, $\overline{XI}$ is grounded. In depth expansion or daisy chain expansion, $\overline{XI}$ is connected to $\overline{XO}$ (expansion out) of the previous device.
SIX	Serial Input Expansion	I	In the Expansion mode, the SIX pin of the least significant device is tied high. The SIX pin of all other devices is connected to the D7 or D8 pin of the previous device. For single device operation, SIX is tied high.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is set low, the parallel output buffers receive data from the RAM array. When $\overline{OE}$ is set high, parallel three state buffers inhibit data flow.
Q0–Q8	Output Data	O	Data outputs for 9-bit wide data.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ goes low, the device is full and data must not be clocked by SICP. When $\overline{FF}$ is high, the device is not full. See the diagram on page 7 for more details.
$\overline{EF}$	Empty Flag Almost-Full Flag	O	When $\overline{EF}$ goes low, the device is empty and further READ operations are inhibited. When $\overline{EF}$ is high, the device is not empty.
$\overline{AEF}$	Almost-Empty/ Half-Full Flag	O	When $\overline{AEF}$ is low, the device is empty to 1/8 full or 7/8 to completely full. When $\overline{AEF}$ is high, the device is greater than 1/8 full, but less than 7/8 full.
$\overline{XO/HF}$	Expansion Out/	O	This is a dual purpose output. In the single device configuration ($\overline{XI}$ grounded), the device is more than half full when $\overline{HF}$ is low. In the depth expansion configuration ($\overline{XO}$ connected to $\overline{XI}$ of the next device), a pulse is sent from $\overline{XO}$ to $\overline{XI}$ when the last location in the RAM array is filled.
D7, D8	Data Set	O	The appropriate Data Set pin (D7, D8) is connected to $\overline{NW}$ to program the Serial In data word width. For example: D7 - $\overline{NW}$ programs a 8-bit word width, D8 - $\overline{NW}$ programs a 9-bit word width, etc.
Vcc	Power Supply		Single Power Supply of 5V.
GND	Ground		Three grounds at 0V.

2752 tbl 01

STATUS FLAGS

Number of Words In FIFO					
IDT72132	IDT72142	$\overline{FF}$	$\overline{AEF}$	$\overline{HF}$	$\overline{EF}$
0	0	H	L	H	L
1-255	1-511	H	L	H	H
256-1024	512-2048	H	H	H	H
1025-1792	2049-3584	H	H	L	H
1793-2047	3585-4095	H	L	L	H
2048	4096	L	L	L	H

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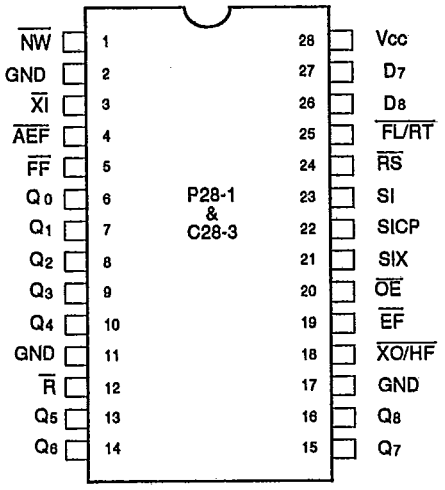
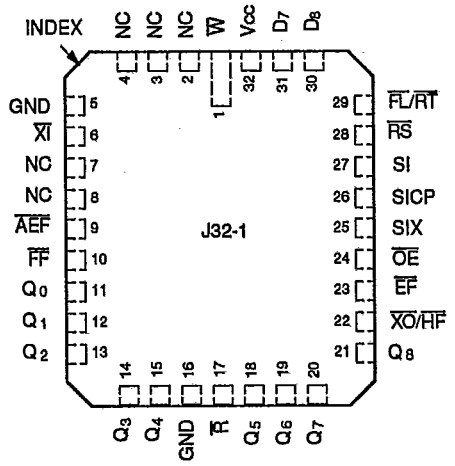
PIN CONFIGURATIONS



DIP
TOP VIEW

2752 drw 02



PLCC
TOP VIEW

2752 drw 02b

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2752 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	—	—	V
V_{IH}	Input High Voltage Military	2.2	—	—	V
V_{IL}(1)	Input Low Voltage	—	—	0.8	V

NOTE: 2752 tbl 04
1. 1.5V undershoots are allowed for 10ns once per cycle.

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CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE: 2752 tbl 05
1. This parameter is sampled and not 100% tested.

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DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	IDT72132/IDT72142 Commercial			IDT72132/IDT72142 Military			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{IL}(1)	Input Leakage Current (Any Input)	-1	—	1	-10	—	10	µA
I_{OL}(2)	Output Leakage Current	-10	—	10	-10	—	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OUT} = -2mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage, I_{OUT} = 8mA	—	—	0.4	—	—	0.4	V
I_{CC1}(3)	Power Supply Current	—	90	140	—	100	160	mA
I_{CC2}(3)	Average Standby Current ($\overline{R}$ = $\overline{RS}$ = $\overline{FL/RT}$ = V_{IH}) (SICP = V_{IL})	—	8	12	—	12	25	mA
$I_{CC3(L)}$(3,4)	Power Down Current	—	—	2	—	—	4	mA
$I_{CC3(S)}$(3,4)	Power Down Current	—	—	8	—	—	12	mA

NOTES: 2752 tbl 06
1. Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}.
2. R ≤ V_{IL}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. Icc measurements are made with outputs open.
4. RS = FL/RT = R = V_{CC} -0.2V; SICP ≤ 0.2V; all other inputs ≥ V_{CC} -0.2V or ≤ 0.2V.

AC ELECTRICAL CHARACTERISTICS

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(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	Commercial IDT72132x35 IDT72142x35		Military IDT72132x40 IDT72142x40		Mil. and Com'l. IDT72132x50 IDT72142x50		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_S	Parallel Shift Frequency	—	22.2	—	20	—	15	MHz
f_{SICP}	Serial-InShift Frequency	—	50	—	50	—	40	MHz
PARALLEL OUTPUT TIMINGS								
t_A	Access Time	—	35	—	40	—	50	ns
t_{RR}	Read Recovery Time	10	—	10	—	15	—	ns
t_{RPW}	Read Pulse Width	35	—	40	—	50	—	ns
t_{RC}	Read Cycle Time	45	—	50	—	65	—	ns
t_{RLZ}	Read Pulse Low to Data Bus at Low Z[1]	5	—	5	—	10	—	ns
t_{RHZ}	Read Pulse High to Data Bus at High Z[1]	—	20	—	25	—	30	ns
t_{DV}	Data Valid from Read Pulse High	5	—	5	—	5	—	ns
t_{OEHZ}	Output Enable to High-Z (Disable)[1]	—	15	—	15	—	15	ns
t_{OELZ}	Output Enable to Low-Z (Enable)[1]	5	—	5	—	5	—	ns
t_{AOE}	Output Enable to Data Valid (Q_{0-8})	—	20	—	20	—	22	ns
SERIAL INPUT TIMINGS								
t_{SIS}	Serial Data In Set-Up Time to SICP Rising Edge	12	—	12	—	15	—	ns
t_{SIH}	Serial Data In Hold Time to SICP Rising Edge	0	—	0	—	0	—	ns
t_{SIX}	SIX Set-Up Time to SICP Rising Edge	5	—	5	—	5	—	ns
t_{SICW}	Serial-In Clock Width High/Low	8	—	8	—	10	—	ns
FLAG TIMINGS								
t_{SICEF}	SICP Rising Edge (Last Bit - First Word) to $\overline{EF}$ High	—	45	—	50	—	65	ns
t_{SICFF}	SICP Rising Edge (Bit 1 - Last Word) to $\overline{FF}$ Low	—	30	—	35	—	40	ns
t_{SICF}	SICP Rising Edge to $\overline{HF}$, $\overline{AEF}$	—	45	—	50	—	65	ns
t_{RFFSI}	Recovery Time SICP After $\overline{FF}$ Goes High	15	—	15	—	15	—	ns
t_{REF}	Read Low to $\overline{EF}$ Low	—	30	—	35	—	45	ns
t_{RFF}	Read High to $\overline{FF}$ High	—	30	—	35	—	45	ns
t_{RF}	Read High to Transitioning $\overline{HF}$ and $\overline{AEF}$	—	45	—	50	—	65	ns
t_{RPE}	Read Pulse Width After $\overline{EF}$ High	35	—	40	—	50	—	ns
RESET TIMINGS								
t_{RSC}	Reset Cycle Time	45	—	50	—	65	—	ns
t_{RS}	Reset Pulse Width	35	—	40	—	50	—	ns
t_{RSS}	Reset Set-up Time	35	—	40	—	50	—	ns
t_{RSR}	Reset Recovery Time	10	—	10	—	15	—	ns
t_{RSF1}	Reset to $\overline{EF}$ and $\overline{AEF}$ Low	—	45	—	50	—	65	ns
t_{RSF2}	Reset to $\overline{HF}$ and $\overline{FF}$ High	—	45	—	50	—	65	ns
t_{RSDL}	Reset to D Low	20	—	20	—	35	—	ns
t_{POI}	SICP Rising Edge to D	5	17	5	17	5	20	ns
RETRANSMIT TIMINGS								
t_{RTC}	Retransmit Cycle Time	45	—	50	—	65	—	ns
t_{RT}	Retransmit Pulse Width	35	—	40	—	50	—	ns
t_{RTS}	Retransmit Set-up Time	35	—	40	—	50	—	ns
t_{RTR}	Retransmit Recovery Time	10	—	10	—	15	—	ns
DEPTH EXPANSION MODE TIMINGS								
t_{XOL}	Read/Write to $\overline{XO}$ Low	—	40	—	45	—	50	ns
t_{XOH}	Read/Write to $\overline{XO}$ High	—	40	—	45	—	50	ns
t_{XI}	$\overline{XI}$ Pulse Width	35	—	40	—	50	—	ns
t_{XIR}	$\overline{XI}$ Recovery Time	10	—	10	—	10	—	ns
t_{XIS}	$\overline{XI}$ Set-up Time	16	—	15	—	15	—	ns

NOTE:
1. Guaranteed by design minimum times, not tested

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AC ELECTRICAL CHARACTERISTICS (Continued)

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(Commercial: Vcc = 5.0V ± 10%, TA = 0°C to +70°C; Military: Vcc = 5.0V ± 10%, TA = -55°C to +125°C)

		Military and Commercial						
		IDT72132x65 IDT72142x65		IDT72132x80 IDT72142x80		IDT72132x120 IDT72142x120		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
tS	Parallel Shift Frequency	—	12.5	—	10	—	7	MHz
tSOCP	Serial-Out Shift Frequency	—	33	—	28	—	25	MHz
PARALLEL OUTPUT TIMINGS								
tA	Access Time	—	65	—	80	—	120	ns
tRR	Read Recovery Time	15	—	20	—	20	—	ns
tRPW	Read Pulse Width	65	—	80	—	120	—	ns
tRC	Read Cycle Time	80	—	100	—	140	—	ns
tRLZ	Read Pulse Low to Data Bus at Low Z[1]	10	—	10	—	10	—	ns
tRHZ	Read Pulse Highto Data Bus at High Z[1]	—	30	—	35	—	35	ns
tDV	Data Valid from Read Pulse High	5	—	5	—	5	—	ns
tOEHZ	Output Enable to High-Z (Disable)[1]	—	20	—	25	—	30	ns
tOELZ	Output Enable to Low-Z (Enable)[1]	5	—	5	—	5	—	ns
tAOE	Output Enable to Data Valid (Q_{0-8})	—	25	—	30	—	35	ns
SERIAL INPUT TIMINGS								
tSIS	Serial Data In Set-Up Time to SICP Rising Edge	15	—	20	—	20	—	ns
tSIH	Serial Data In Hold Time to SICP Rising Edge	0	—	5	—	5	—	ns
tSIX	SIX Set-Up Time to SICP Rising Edge	5	—	5	—	5	—	ns
tSICW	Serial-In Clock Width High/Low	10	—	15	—	15	—	ns
FLAG TIMINGS								
tSICEF	SICP Rising Edge (Last Bit - First Word) to $\overline{EF}$ High	—	80	—	80	—	80	ns
tSICFF	SICP Rising Edge (Bit 1 - Last Word) to $\overline{FF}$ Low	—	50	—	60	—	60	ns
tSICF	SICP Rising Edge to $\overline{HF}$, $\overline{AEF}$	—	80	—	80	—	80	ns
tRFFSI	Recovery Time SICP After $\overline{FF}$ Goes High	15	—	20	—	20	—	ns
tREF	Read Low to $\overline{EF}$ Low	—	60	—	60	—	60	ns
tRFF	Read High to $\overline{FF}$ High	—	60	—	60	—	60	ns
tRF	Read High to Transitioning $\overline{HF}$ and $\overline{AEF}$	—	80	—	100	—	140	ns
tRPE	Read Pulse Width After $\overline{EF}$ High	65	—	80	—	120	—	ns
RESET TIMINGS								
tRSC	Reset Cycle Time	80	—	100	—	140	—	ns
tRS	Reset Pulse Width	65	—	80	—	120	—	ns
tRSS	Reset Set-up Time	65	—	80	—	120	—	ns
tRSR	Reset Recovery Time	15	—	20	—	20	—	ns
tRSF1	Reset to $\overline{EF}$ and $\overline{AEF}$ Low	—	80	—	100	—	140	ns
tRSF2	Reset to $\overline{HF}$ and $\overline{FF}$ High	—	80	—	100	—	140	ns
tRSDL	Reset to D Low	50	—	65	—	105	—	ns
tPOI	SICP Rising Edge to D	5	25	5	30	5	35	ns
RETRANSMIT TIMINGS								
tRTC	Retransmit Cycle Time	80	—	100	—	140	—	ns
tRT	Retransmit Pulse Width	65	—	80	—	120	—	ns
tRTS	Retransmit Set-up Time	65	—	80	—	120	—	ns
tRTR	Retransmit Recovery Time	15	—	20	—	20	—	ns
DEPTH EXPANSION MODE TIMINGS								
tXOL	Read/Write to $\overline{XO}$ Low	—	65	—	80	—	120	ns
tXOH	Read/Write to $\overline{XO}$ High	—	65	—	80	—	120	ns
tXI	$\overline{XI}$ Pulse Width	65	—	80	—	120	—	ns
tXIR	$\overline{XI}$ Recovery Time	10	—	10	—	10	—	ns
tXIS	$\overline{XI}$ Set-up Time	15	—	15	—	15	—	ns

NOTE:
1. Guaranteed by design minimum times, not tested.

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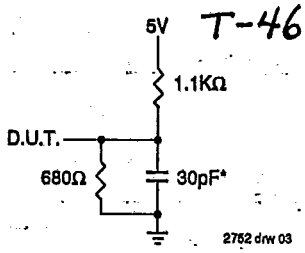
AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure A

2752 tbl 09



or equivalent circuit

Figure A. Output Load

*Includes jig and scope capacitances

FUNCTIONAL DESCRIPTION

Serial Data Input

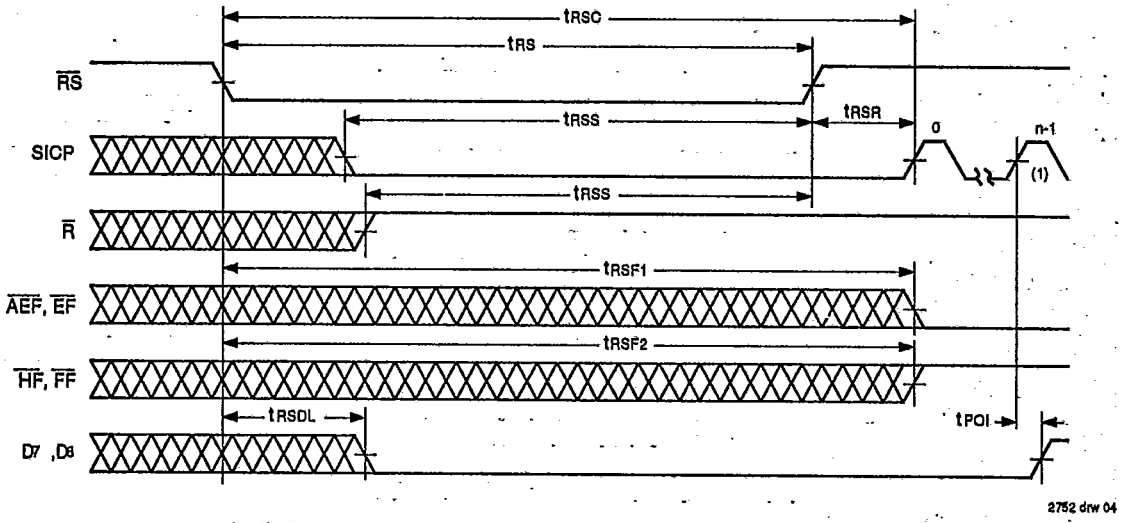
The serial data is input on the SI pin. The data is clocked in on the rising edge of SICP providing the Full Flag ($\overline{FF}$) is not asserted. If the Full Flag is asserted then the next parallel data word is inhibited from moving into the RAM array. NOTE: SICP should not be clocked once the last bit of the last word has been shifted in, as indicated by $\overline{NW}$ high and $\overline{FF}$ low. If it is, then then the input data will be lost.

The serial word is shifted in Least Significant Bit first. Thus, when the FIFO is read, the Least Significant Bit will come out on Q_0 and the second bit is on Q_1 and so on. The serial word width must be programmed by connecting the appropriate Data Set line (D_7, D_8) to the $\overline{NW}$ input. The data set lines are taps off a digital delay line. Selecting one of these taps programs the width of the serial word to be written in.

Parallel Data Output

A read cycle is initiated on the falling edge of Read ($\overline{R}$) provided the Empty Flag is not set. The output data is accessed on a first-in/first-out basis, independent of the ongoing write operations. The data is available t_A after the falling edge of $\overline{R}$ and the output bus Q goes into high impedance after $\overline{R}$ goes HIGH.

Alternately, the user can access the FIFO by keeping $\overline{R}$ LOW and enabling data on the bus by asserting Output Enable ($\overline{OE}$). When $\overline{R}$ is LOW, the $\overline{OE}$ signal enables data on the output bus. When $\overline{R}$ is LOW and $\overline{OE}$ is HIGH, the output bus is three-stated. When $\overline{R}$ is HIGH, the output bus is disabled irrespective of $\overline{OE}$.



NOTE:
1. Input bits are numbered 0 to n-1. D_7 and D_8 correspond to n=8 and n=9 respectively

Figure 1. Reset

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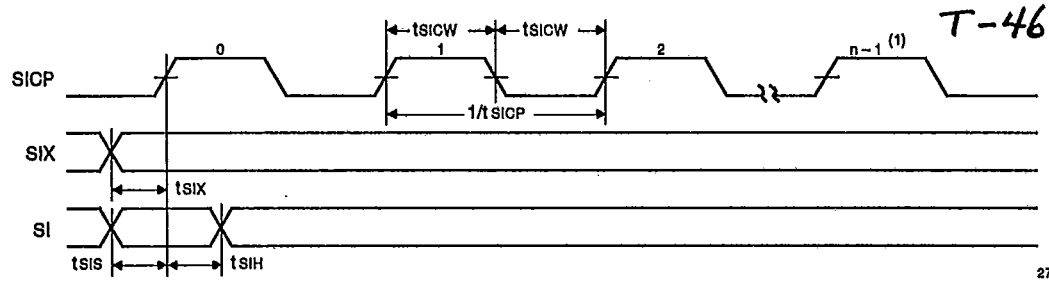


Figure 2. Write Operation

NOTE:
1. Input bits are numbered 0 to n-1.

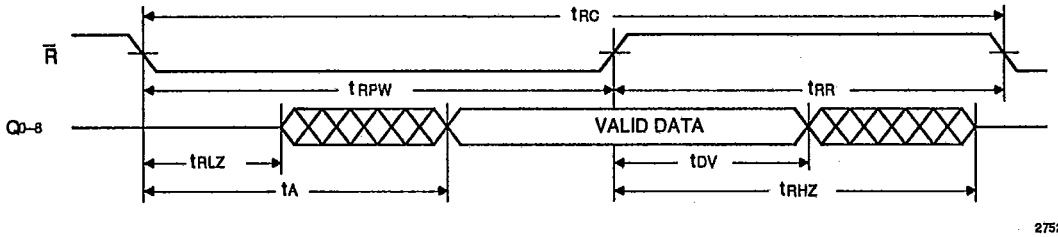


Figure 3. Read Operation

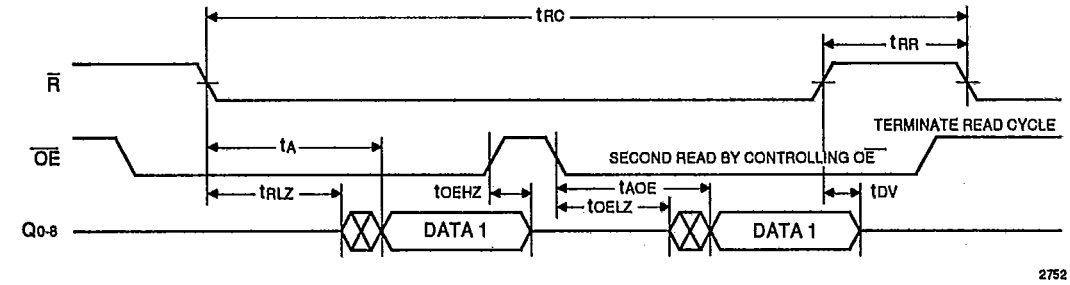
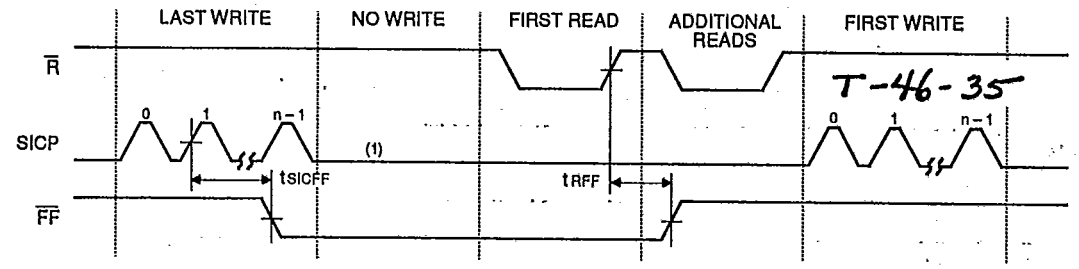


Figure 4. Output Enable Timings



NOTE:
1. SICP should not be clocked until $\overline{FF}$ goes high.

Figure 5. Full Flag from Last Write to First Read

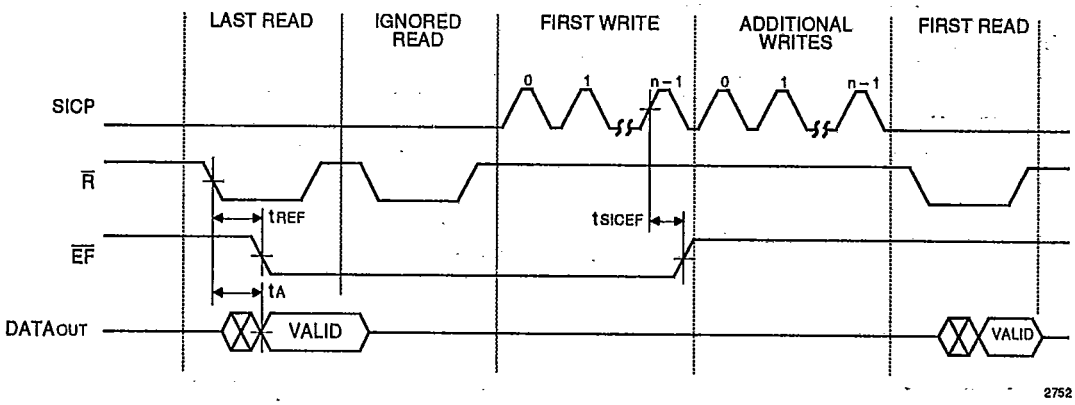


Figure 6. Empty Flag from Last Read to First Write

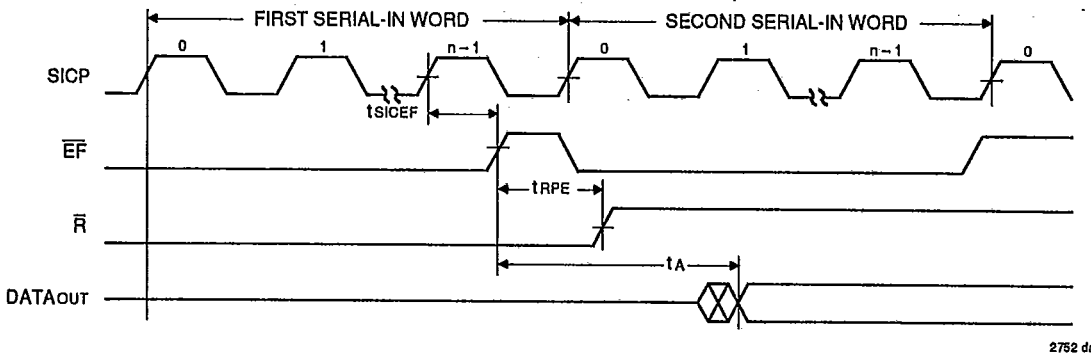


Figure 7. Empty Boundry Condition Timing

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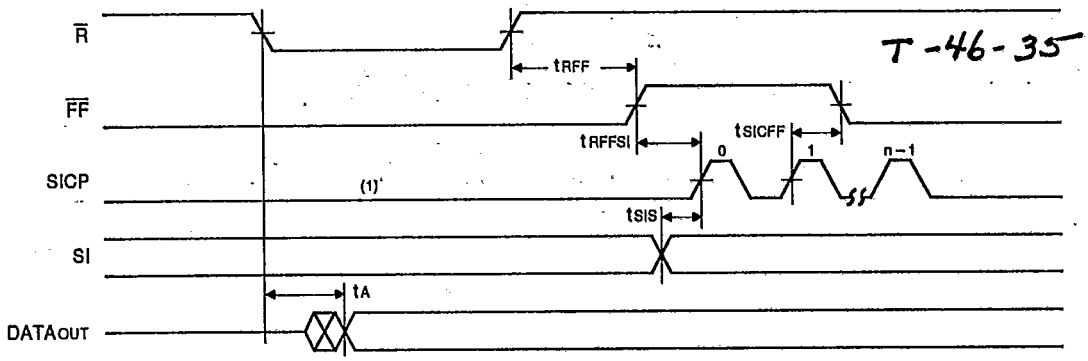

NOTE:
1. SICP should remain low until after FF goes high.

2752 drw 11

Figure 8. Full Boundry Condition Timing

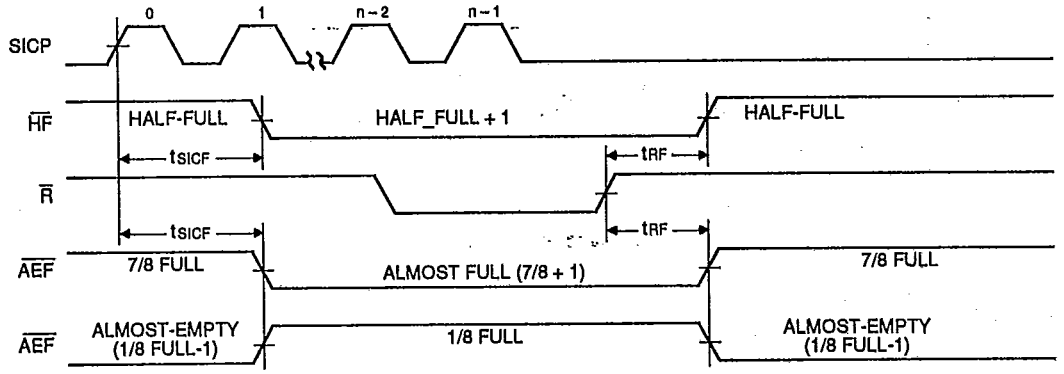

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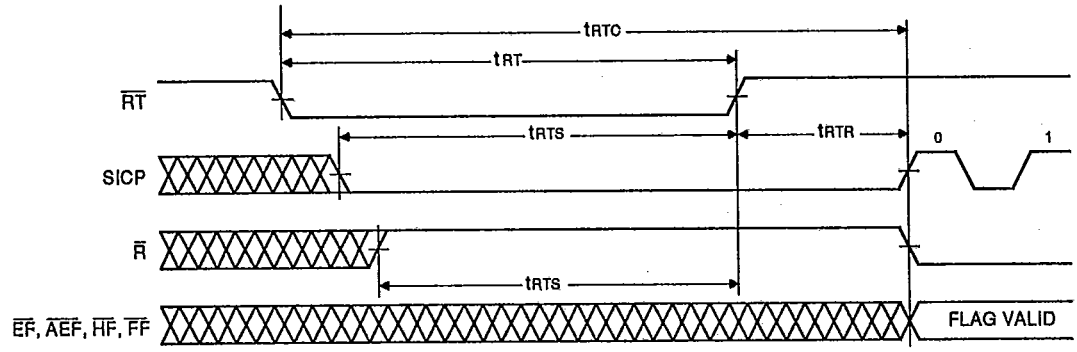
Figure 9. Half Full, Almost Full and Almost Empty Timings



2752 drw 13

NOTE:
1. EF, AEF, HF and FF may change status during Retransmit, but flags will be valid at tRTC.

Figure 10. Retransmit

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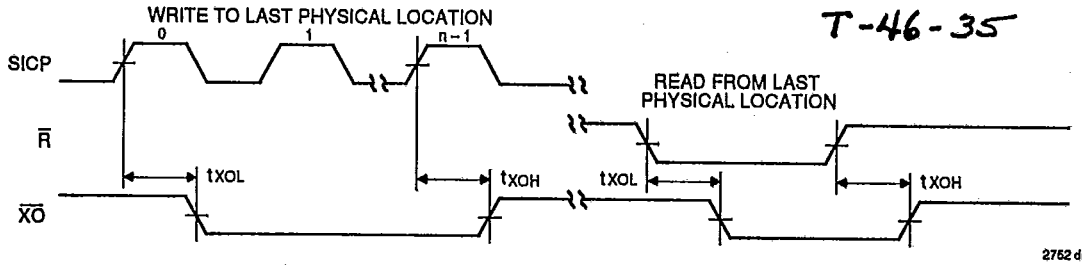

Figure 11. Expansion-Out

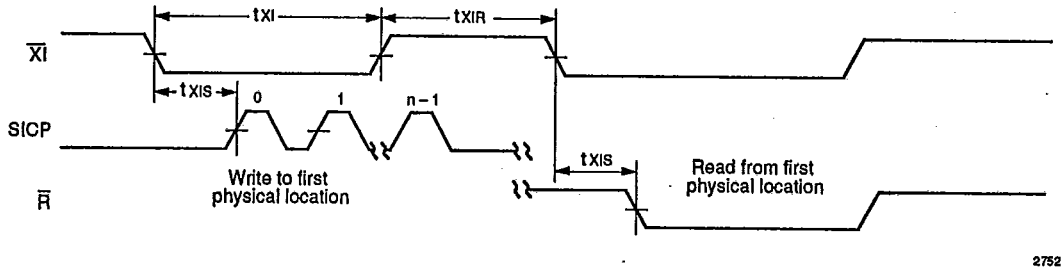

Figure 12. Expansion-In

OPERATING CONFIGURATIONS

Single Device Configuration

In the standalone case, the SIX line is tied HIGH and not used. On the first LOW-to-HIGH of the SICP clock, both of the Data Set lines (D7, D8) go low and a new serial word is started. The Data Set lines then go high on the equivalent SICP clock pulse. This continues until the D line connected to $\overline{NW}$ goes high completing the serial word. The cycle is then repeated with the next LOW-to-HIGH transition of SICP.

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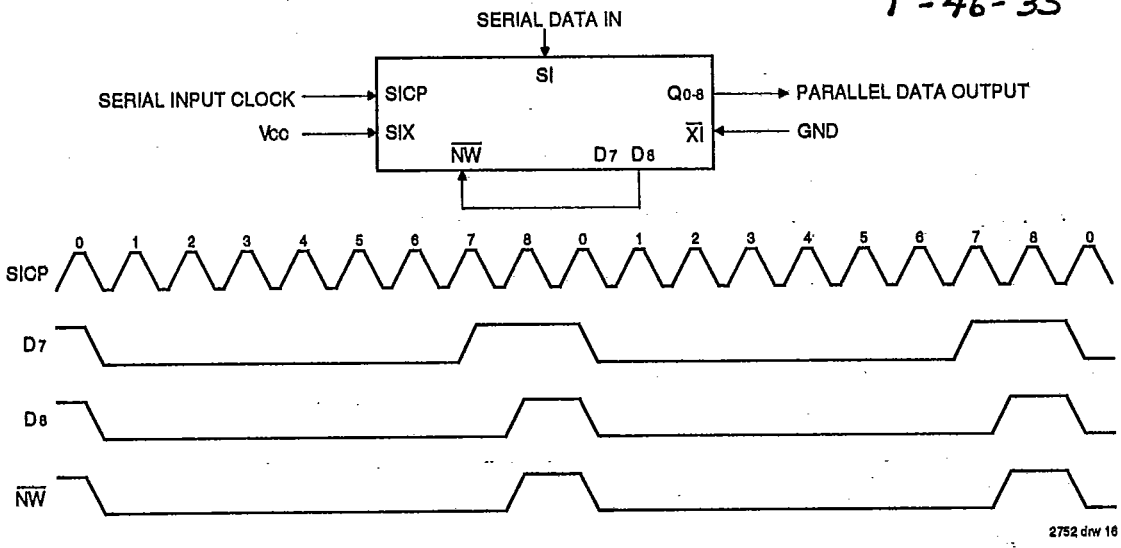

Figure 13. Nine-Bit Word Single Device Configuration

TRUTH TABLES

TABLE 1: RESET AND RETRANSMIT — SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{AEF}$, $\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment(1)	Increment(1)	X	X	X

NOTE:
1. Pointer will increment if appropriate flag is HIGH.

Width Expansion Configuration

In the cascaded case, word widths of more than 9 bits can be achieved by using more than one device. By tying the SIX line of the least significant device HIGH and the SIX of the subsequent devices to the appropriate Data Set lines of the previous devices, a cascaded serial word is achieved.

On the first LOW-to-HIGH clock edge of SICP, both the Data Set lines go LOW. Just as in the standalone case, on each corresponding clock cycle, the equivalent Data Set line goes HIGH in order of least to most significant.

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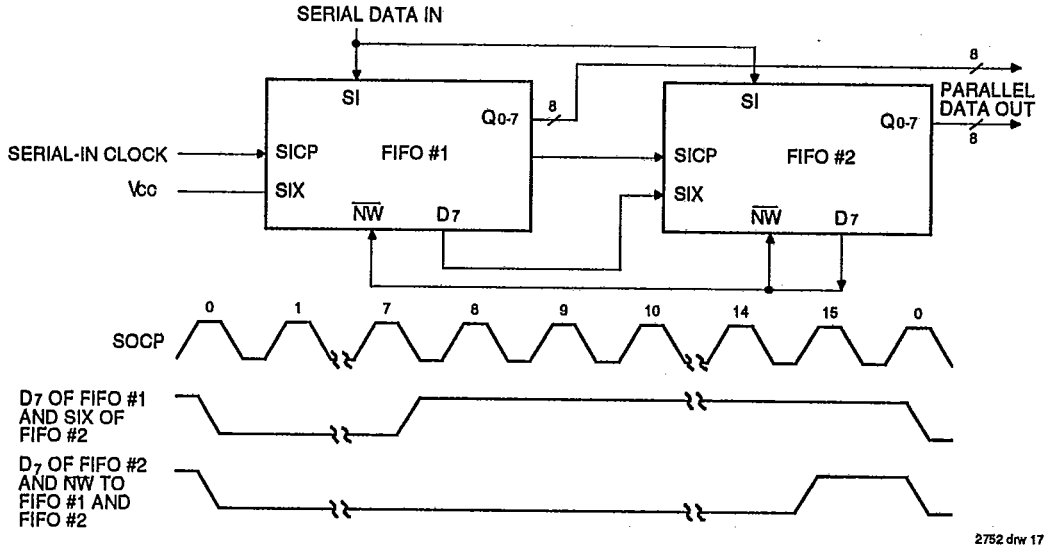

Figure 14. Serial-In to Parallel-Out Data of 16 Bits

Depth Expansion (Daisy Chain) Mode

The IDT72132/42 can be easily adapted to applications where the requirements are for greater than 2048/4096 words. Figure 15 demonstrates Depth Expansion using three IDT72132/42. Any depth can be attained by adding additional IDT72132/42 operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin and Expansion In ($\overline{XI}$) pin of each device must be tied together.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the OR-ing of all $\overline{EF}$s and OR-ing of all $\overline{FF}$s (i.e., all must be set to generate the correct composite ($\overline{FF}$) or ($\overline{EF}$).
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion mode.

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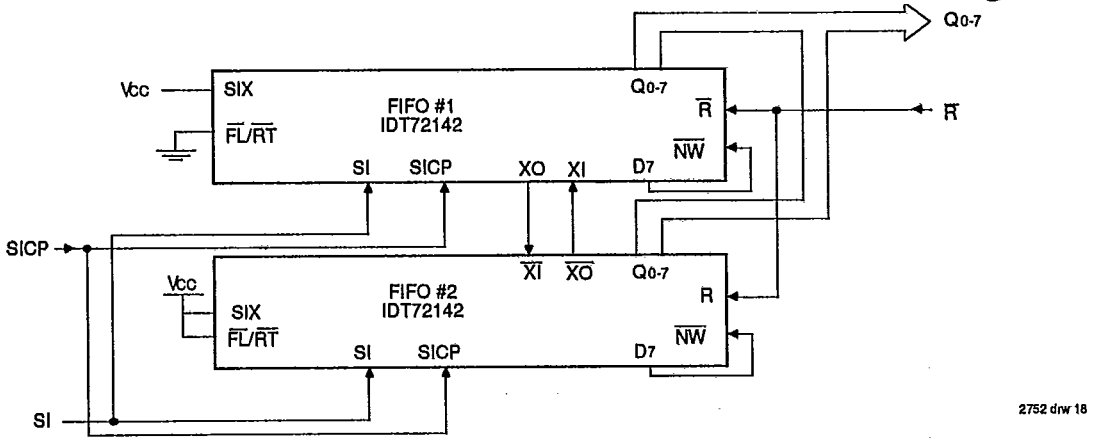

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Figure 15. An 8K x 8 Serial-In Parallel-Out FIFO

TABLE 2: RESET AND FIRST LOAD TRUTH TABLE — DEPTH EXPANSION/COMPOUND EXPANSION MODE

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset-First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset all Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTES:
1. $\overline{XI}$ is connected to $\overline{XO}$ of the previous device.
2. $\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Ouput, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input.

SERIAL INPUT WITH WIDTH AND DEPTH EXPANSION

T-46-35

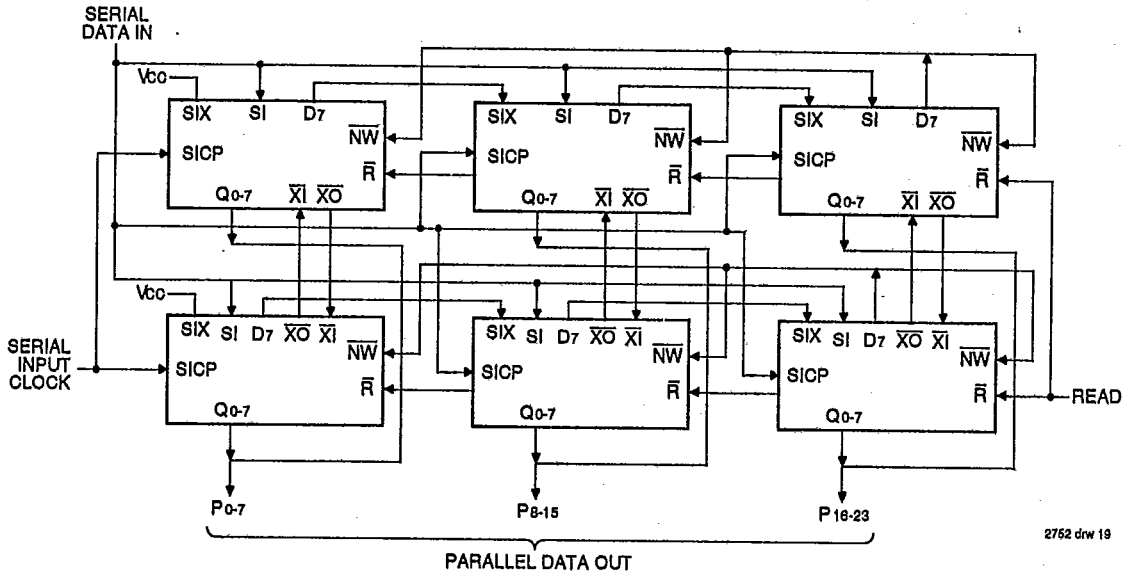

Figure 16. An 8K x 24 Serial-In, Parallel-Out FIFO Using Six IDT72142s