# Mini-Motherboard Clock Generator

## Description

The **ICS1694A** Mini-Motherboard Clock Generator has been developed to give designers a unique, efficient (cost, size, and power) means of generating the various clocks required in a digital system. The initial patterns being offered as standards are summarized in Table 1.

The low cost and small size of the **ICS1694A** allow the designer to use multiple devices (different patterns) in a system in order to generate the clock signals physically close to the requirement, instead of having long PCB board traces transmitting (and radiating) the signals.

The **ICS1694A** contains all the passive components required for a crystal oscillator or it may be driven by a clock signal. In some applications, one of the outputs of one **ICS1694A** will be used as the clock input of a second or third **ICS1694A**, thus requiring only one quartz crystal for the system and, in the process, synchronizing all the clock signals to the crystal oscillator.

The **ICS1694A** contains a single PLL. Therefore all output frequencies, other than the buffered crystal oscillator, must be the result of an integer division of the PLL frequency. For instance, if the PLL operates at 120 MHz, the outputs could be a selection of three of any of the following: 120 MHz, 60 MHz, 40 MHz, 30 MHz, 24 MHz, 20 MHz, 15 MHz, 12 MHz, 10 MHz, 8 MHz, 6 MHz, etc. More detail concerning the options is given in the section titled PATTERNS.

## Features

- Low Cost Motherboard Clock Generator
- Small Footprint, space-saving package
- Very Flexible Architecture
- Advanced PLL design
- Upgraded the ICS1694 to include Output Enable and higher frequency capabilities
- Many standard patterns available

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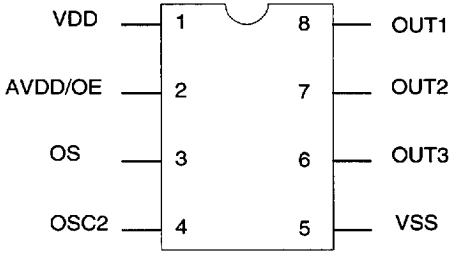
## Applications

- Any design requiring clocking signals or count down chains derived from a clock signal
- Memory refresh
- Keyboard
- Serial port
- Floppy Disk
- Hard Disk
- CPU
- Co-processor




**8-Pin DIP or SOIC**
**K-3, K-6**



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## Options

Pin 2 may be bonded to serve as either AVDD (analog positive supply) or OE (output enable). The outputs (OUT1, OUT2, and OUT3) will be enabled when OE is held high. OE has internal pull-up so it may be allowed to float.

If particularly stable outputs are required, the option with pin 2 bonded as AVDD is recommended. AVDD should be driven by the system's analog supply, if available. In some applications where only a digital supply is available, AVDD can be driven from the digital VDD supply through a simple RC decoupling circuit. The voltage drop across the series resistor should be held to less than 250 mv. It is difficult to generalize across all applications, but in the majority of cases the performance of the **ICS1694A** is completely satisfactory when used with power supplied only to pin 1 and pin 2 bonded as Output Enable.

## Patterns

A number of standard patterns will be offered which will satisfy most of the typical requirements of the PC market. New patterns are continuously being added as new applications surface. ICS welcomes suggestions for new patterns and will also fabricate custom patterns as described in the following paragraph.

The **ICS1694A** contains one PLL-VCO which is mask programmable to any frequency up to 180 MHz. The chip contains a number of counter stages which can be used to count the VCO frequency down to the desired output frequencies. The output frequencies are derived by dividing the VCO frequency by an integer.This is a limitation on the frequencies which can be generated in the same chip since each frequency must be derived from the same VCO frequency.

For instance, pattern 010 programs the VCO to 120 MHz. Then a divide by 3 yields 40 MHz; a divide by 4 yields 30 MHz; and a divide by 5 yields 24 MHz. Obviously, some of the divide chains can and are combined. An output may also be the crystal oscillator frequency or that frequency divided by an integer.

It should also be considered that the input does not have to be 14.318 MHz, but can be any fundamental mode crystal up to 25 MHz. Table 1 lists the frequencies available from the various patterns. For any of these patterns, the crystal frequency (and thus the PLL-VCO frequency) may be changed and the output frequencies will be scaled accordingly. For instance, if the crystal frequency used is one half of that listed in Table 1, the actual output frequencies will be one half those listed in the table. Also options are available which will work with an overtone crystal.

## Absolute Maximum Ratings

| | | |
|---|---|---|
| Supply Voltage | $V_{DD}$ | -0.5V to +7V |
| Input Voltage | $V_{IN}$ | -0.5V to $V_{DD}$+0.5V |
| Output Voltage | $V_{OUT}$ | -0.5V to $V_{DD}$+0.5V |
| Clamp Diode Current | $V_{IK}$ & $I_{OK}$ | +/-30mA |
| Output Current per Pin | $I_{OUT}$ | +/-50mA |
| Operating Temperature | $T_o$ | 0 °C to 70 °C |
| Storage Temperature | $T_S$ | -85 °C to +150 °C |
| Power Dissipation | $P_D$ | 300mW |

Values beyond these ratings may damage the device. This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than the maximum rated voltages. For proper operation it is recommended that $V_{IN}$ and $V_{OUT}$ be constrained to >= $V_{SS}$ and <=$V_{DD}$.



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## DC Characteristics (0°C to 70°C)

| SYMBOL | PARAMETER | MIN | MAX | UNITS | CONDITIONS |
|---|---|---|---|---|---|
| | | **5.0V ± 5% OPERATION** | | | |
| $V_{DD}$ | Operating Voltage Range | 4.75 | 5.25 | V | |
| $V_{IL}$ | Input Low Voltage | $V_{ss}$ | 0.8 | V | $V_{DD}$ = 5V |
| $V_{IH}$ | Input High Voltage | 2.0 | $V_{DD}$ | V | $V_{DD}$ = 5V |
| $I_{LH}$ | Input Leakage Current | -- | 10 | µA | $V_{IN} = V_{cc}$ |
| $V_{OL}$ | Output Low Voltage | -- | 0.4 | V | $I_{OL}$ = 4.0 mA |
| $V_{OH}$ | Output High Voltage | 2.4 | -- | V | $I_{OH}$ = 4.0 mA |
| $I_{DD}$ | Digital Supply Current | -- | 30 | mA | $V_{DD}$ = 5V, VCO = 120 MHz |
| $I_{AA}$ | Analog Supply Current | | 8 | mA | $V_{DD}$ = 5V, VCO = 120 MHz |
| $C_{in}$ | Input Pin Capacitance | -- | 8 | pF | $F_c$ = 1 MHz |
| $C_{out}$ | Output Pin Capacitance | -- | 12 | pF | $F_c$ = 1 MHz |
| | | **3.3V ± 10% OPERATION** | | | |
| $I_{DD}$ | Digital Supply Current | - | 20 | mA | $V_{DD}$ = 3.3V, VCO = 120 MHz |
| $I_{AA}$ | Analog Supply Current | - | 6 | mA | $V_{DD}$ = 3.3V, VCO = 120 MHz |

If the OE option is used, IDD will be the sum of both the digital and analog supply currents.

## AC Timing Characteristics

The following notes apply to all of the parameters presented in this section:

1. Xtal Frequency = 14.318 MHz, unless otherwise noted.
2. All units are in nanoseconds (ns).
3. Rise and fall time is between 0.8 and 2.0 VDC at 5.0V.
4. Output pin loading = 15pF
5. Duty cycle is measured at 1.4V at 5.0V.
6. Temperature Range = 0 °C to 70 °C

**5.0V ± 5% OPERATION**

| SYMBOL | PARAMETER | MIN | MAX | NOTES |
|---|---|---|---|---|
| | | MCLK AND VCLK TIMING | | |
| Tr | Rise Time | -- | 2 | |
| Tf | Fall Time | -- | 2 | |
| Dc | Duty Cycle | 45 | 55 | % |
| Fm | Maximum Frequency | | 180 | MHz |

**3.0V ± 10% OPERATION**

| SYMBOL | PARAMETER | MIN | MAX | NOTES |
|---|---|---|---|---|
| | | MCLK AND VCLK TIMING | | |
| Tr | Rise Time | -- | 3 | |
| Tf | Fall Time | -- | 3 | |
| Dc | Duty Cycle | 45 | 55 | % |
| Fm | Maximum Frequency | | 120 | MHz |



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## Standard Frequency Patterns (MHz)

**Table 1**

| PINS | FUNCTION | PATTERNS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 010 | 011 | 012 | 013 | 014 | 015 | 016 | 017 |
| 8 | OUT1 | 24 | 25 | 12 | 6 | 24 | 24 | XTAL | XTAL |
| 7 | OUT2 | 40 | 40 | 40 | 60 | 40 | XTAL | 16 | 12 |
| 6 | OUT3 | 30 | 30 | 30 | 20 | 20 | 40 | 24 | 24 |
| 5 | VSS | | | | | | | | |
| 4 | XTAL2 | 25 | 25 | 25 | 25 | 14.318 | 14.318 | 14.318 | 14.318 |
| 3 | XTAL1 | | | | | | | | |
| 2 | AVDD/OE | | | | | | | | |
| 1 | VDD | | | | | | | | |

| PINS | FUNCTION | PATTERNS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | |
| 8 | OUT1 | | | | | | | | |
| 7 | OUT2 | | | | | | | | |
| 6 | OUT3 | | | | | | | | |
| 5 | VSS | | | | | | | | |
| 4 | XTAL2 | | | | | | | | |
| 3 | XTAL1 | | | | | | | | |
| 2 | AVDD/OE | | | | | | | | |
| 1 | VDD | | | | | | | | |
| 8 | | | | | | | | | |

## Ordering Information

**ICS1694AN-XXX or ICS1694AM-XXX**

Example:

**ICS XXXX M -XXX**

- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  N=DIP (Plastic)
  M=SOIC
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV=Standard Device; GSP=Genlock Device

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