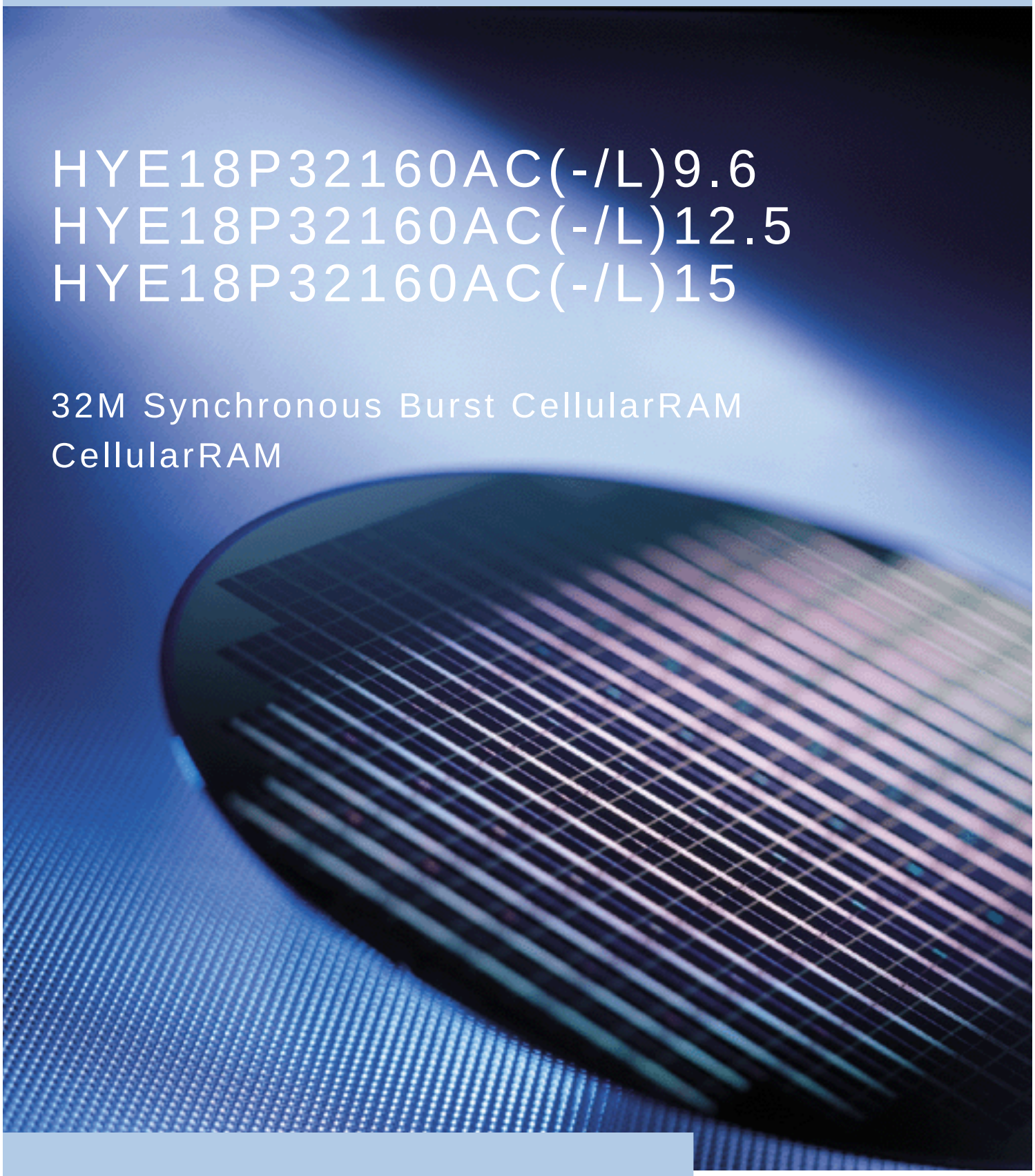
Data Sheet, V2.0, December 2003

HYE18P32160AC(-/L)9.6
HYE18P32160AC(-/L)12.5
HYE18P32160AC(-/L)15

32M Synchronous Burst CellularRAM
CellularRAM



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Revision History:	**2003-12-16**	V2.0
Previous Version:	1.8, 1.9 (Target data sheet)	

Page	Subjects (major changes since last revision)
all	converted to new datasheet template
all	Addition of part numbered **12.5** which is the combination of 70ns Asynch and 80MHz burst speed
22	change of PASR range setting : remove 3/4, then add 1/8
31-33	remove WAIT timing and parameter definition from asynchronous read
all	2nd bin of Icc2 added. Marking for low-power part puts “L” in the place of “-”
all (synch)	No negative (falling) edge of CLK configuration supported
all (synch)	$\overline{\text{ADV}}$ hold time from CLK added for burst operation
all (synch)	tACLK relaxed to 7ns for grade of 9.6
all (synch)	tHD relaxed to 1.5ns for grade of 9.6
all	tLZ, tBLZ, tOLZ are adjusted
all	S/W Register Entry mode is officially supported and specified

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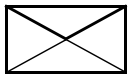

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1 Overview

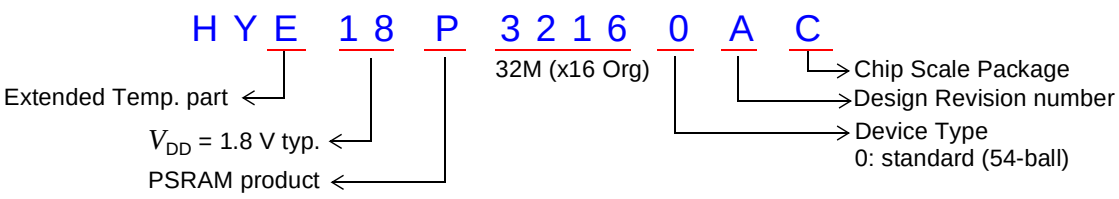
1.1 Features

- High density (1T1C-cell) Synchronous 32-Mbit Pseudo-Static RAM
- Designed for cell phone applications (CellularRAM)
- Functional-compatible (Asynchronous mode) to conventional low power asynchronous SRAM devices
- Organization 2M × 16
- Refresh-free operation
- 1.8 V single power supply (V_{DD} and V_{DDQ})
- Low power optimized design
  - $I_{STANDBY}$ = 90 µA (for L-part[1)]) or 120uA (for standard part), data retention mode
  - I_{DPD} = < 25 µA (32M), non-data retention mode
- Low power features (partly adopted from the JEDEC standardized low power SDRAM specifications)
  - Temperature Compensated Self-Refresh (TCSR)
  - Partial Array Self-Refresh (PASR)
  - Deep Power Down Mode (DPD)
- User configurable interface supporting three different access protocols (values from 9.6 part)
  - asynchronous SRAM protocol, 70 ns random access cycle time, 20 ns page mode (read only) cycle time
  - NOR-Flash burst protocol, 70 ns write cycle time, 104 MHz burst mode read cycle
  - synchronous (bi-directional) interface protocol, 70 ns random cycle time, 104 MHz burst mode read/write cycle
- In NOR-Flash burst or in synchronous mode the additional user settings are featured
  - programmable fixed burst length of 4/8/16 words or continuous burst mode
  - programmable latency modes to adjust the desired burst frequency
  - wrap mode function
  - programmable WAIT signal polarity and timing
- Byte read/write control by $\overline{UB}$/$\overline{LB}$ (Asynchronous mode and in synchronous burst read)
- Synchronous Data Input Mask function supported by $\overline{UB}$/$\overline{LB}$ in synchronous burst write mode
- Wireless operating temperature range from -25 °C to +85 °C
- P-VFBGA-54 chip-scale package (9 × 6 ball grid)

Table 1 Product Selection

HYE18P32160AC		L9.6[1)]	-9.6	L12.5[1)]	-12.5	L15[1)]	-15
Maximum Input CLK frequency (MHz)	Lat = 2	66		50		40	
	Lat = 3	104		**80**		66	
Min. Random Cycle time (t_{RC})		70 ns		**70** ns		85 ns	
Stand-by current (I_{CC2})		90µA	120µA	90µA	120µA	90µA	120µA

1) Contact Factory



1.2 General Description

The 32M Synchronous Burst CellularRAM (CellularRAM) is designed to meet the growing memory density and bandwidth demand in 3G cellular phone designs. Its high density 1T1C-cell concept, the multi-protocol interface capabilities, its highly optimized low power design and its refresh-free operation make the CellularRAM the perfect fit for 3G baseband applications.

Configured in synchronous burst mode, a peak bandwidth of > 200 Mbyte/s is achieved at the max. clock rate of 104 MHz. The burst length can be programmed and set to either fixed burst lengths of 4, 8- or 16-words[1)] or set to continuous mode. The 16-word burst mode is specially designed for cached processor designs to speed up cache re-fill operations.

In NOR-Flash, burst mode read accesses are synchronous whereas write accesses are of asynchronous nature. This is to retain compatibility to today's NOR-Flash protocols and thus to make sure that existing baseband designs do get instantly a performance gain in read direction by deploying the NOR-Flash burst protocol. The different access protocols that are supported by the CellularRAM are illustrated in **Figure 1**. Data byte control ($\overline{UB}$, $\overline{LB}$) is featured in all modes and provides dedicated lower and upper byte access.

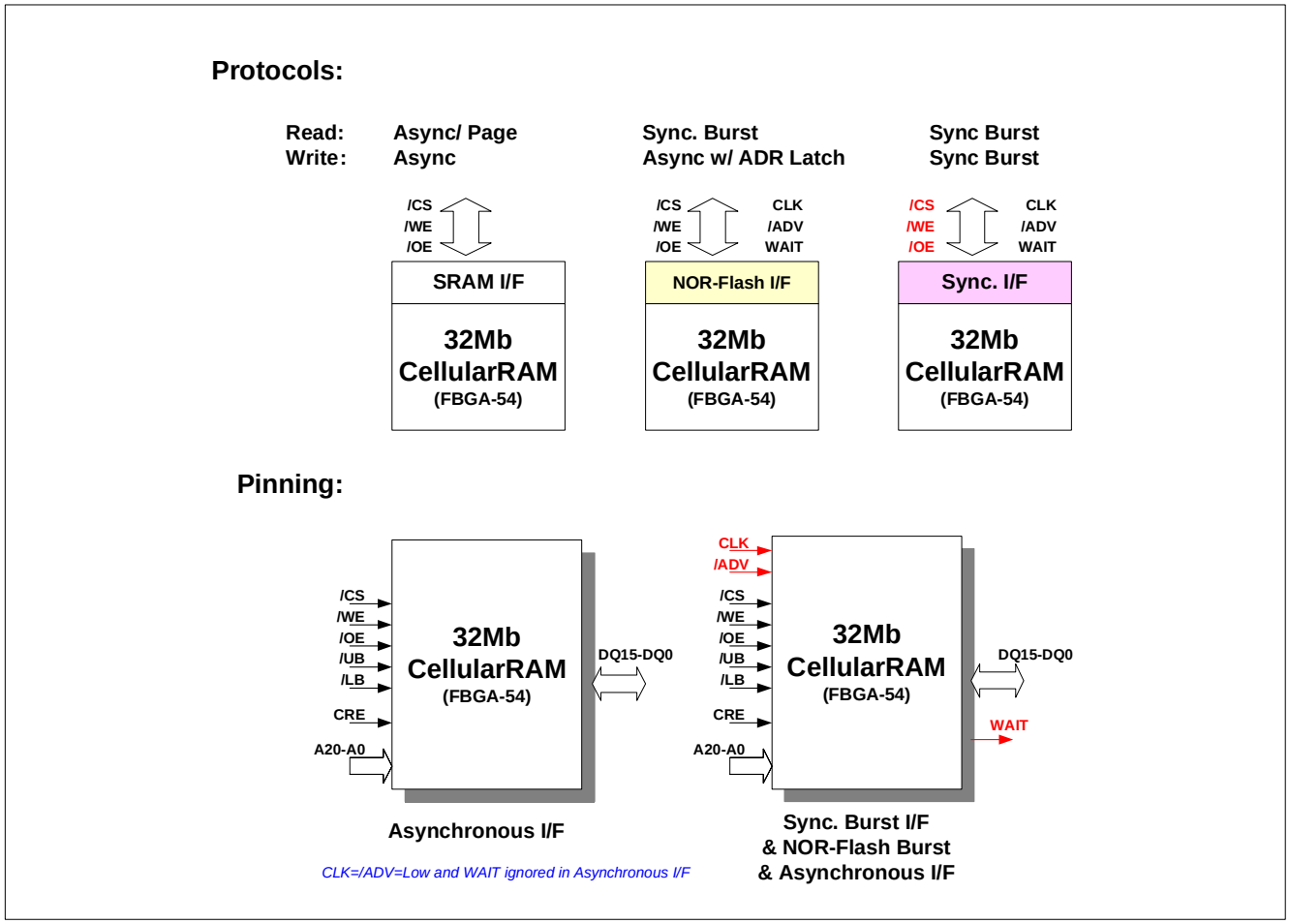


Figure 1 CellularRAM - Interface Configuration Options

The CellularRAM can be operated from a single 1.8 V power supply feeding the core and the output drivers. The chip is fabricated in Infineon Technologies advanced low power 0.14 µm process technology and comes in a P-VFBGA-54 package.

1) 1 word is equal 16 bits

1.3 HYE18P32160AC(-/L)9.6/12.5/15 Ball Configuration

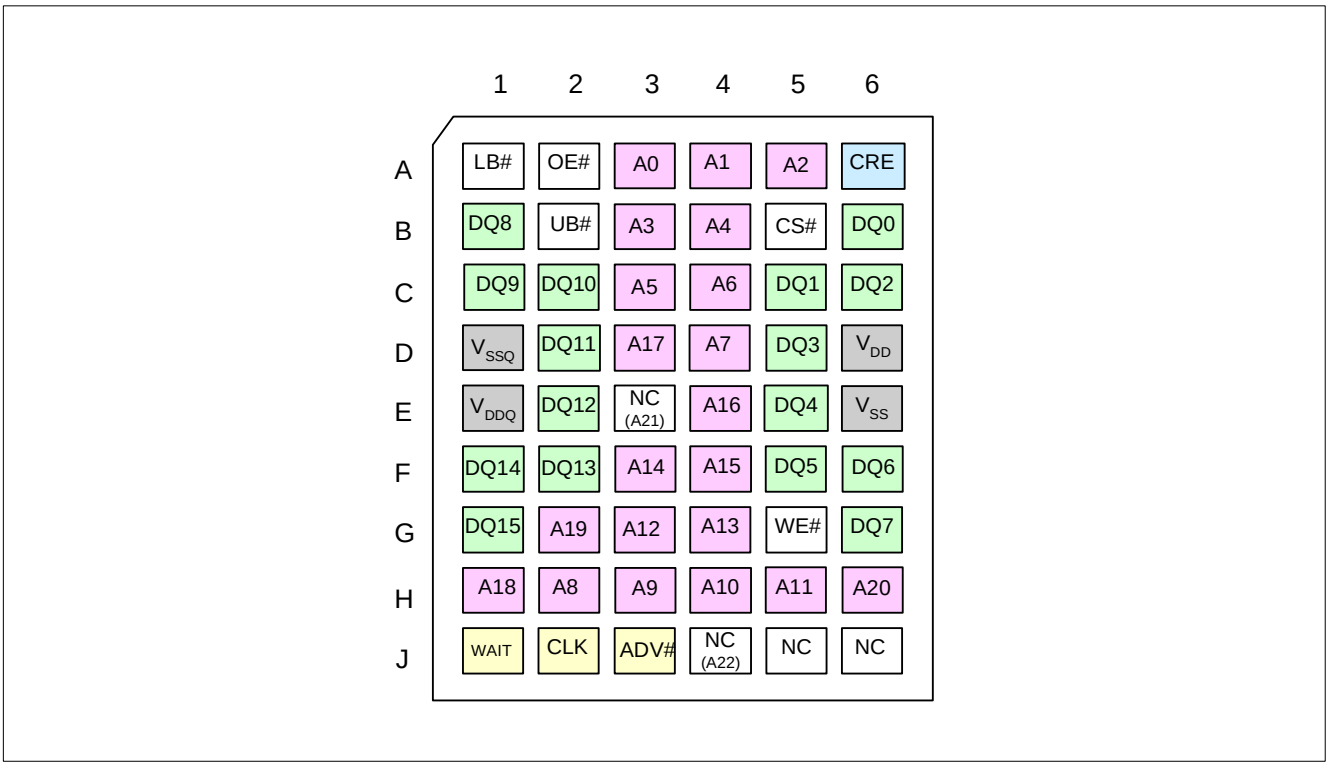


Figure 2 Standard Ballout - HYE18P32160AC(-/L)9.6/12.5/15

*Note: **Figure 2** shows top view*

1.4 HYE18P32160AC(-/L)9.6/12.5/15 Ball Definition and Description

Table 2 Ball Description - HYE18P32160AC(-/L)9.6/12.5/15

Ball	Type	Detailed Function
CLK	Input	**Clock Signal** In synchronous burst mode, address and command inputs and data are referenced to CLK. In asynchronous SRAM-type mode the clock signal is ignored. During write accesses in NOR-Flash operation mode the CLK signal must be clamped to low.
CRE	Input	**Control Register Enable** CRE set to high enables the access to the control register map. By applying the SET CONTROL REGISTER (SCR) command (see **Table 3**) the address bus is loaded into the selected control register.
$\overline{ADV}$	Input	**Address Valid** $\overline{ADV}$ signals in NOR-Flash and full synchronous mode that a valid address is present on the address bus. In NOR-Flash read mode and full synchronous mode the address is latched on the programmed clock edge while $\overline{ADV}$ is held low. In NOR-Flash write mode $\overline{ADV}$ can be used to latch the address, but can be held low as well. In asynchronous SRAM-type mode $\overline{ADV}$ needs to be active, it may be tied to active.
$\overline{CS}$	Input	**Chip Select** $\overline{CS}$ enables the command decoder when low and disables it when high. When the command decoder is disabled new commands are ignored, addresses are don't care and outputs are forced to high-Z. Internal operations, however, continue. For the details please refer to the command tables in **Chapter 1.6**.
$\overline{OE}$	Input	**Output Enable** $\overline{OE}$ controls DQ output driver. $\overline{OE}$ low drives DQ, $\overline{OE}$ high sets DQ to high-Z.
$\overline{WE}$	Input	**Write Enable** $\overline{WE}$ set to low while $\overline{CS}$ is low initiates a write command.
$\overline{UB}$, $\overline{LB}$	Input	**Upper/Lower Byte Enable** $\overline{UB}$ enables the upper byte DQ15-8 (resp. $\overline{LB}$ DQ7 … 0) during read/write operations. $\overline{UB}$ ($\overline{LB}$) deassertion prevents the upper (lower) byte from being driven during read or being written.
WAIT	Output 3-state	**Wait State Signal** In synchronous mode, WAIT signal indicates the host system when the output data is valid during read and when the input data should be asserted during write operation. In asynchronous mode, the signal has to be ignored.
A <20:0>	Input	**Address Inputs** During a Control Register Set operation by CRE access, the address inputs define the register settings.
DQ <15:0>	I/O	**Data Input/Output** The DQ signals $\overline{0}$ to $\overline{15}$ form the 16-bit data bus.
$1 \times V_{DD}$ $1 \times V_{SS}$	Power Supply	**Power Supply, Core** Power and Ground for the internal logic.
$1 \times V_{DDQ}$ $1 \times V_{SSQ}$	Power Supply	**Power Supply, I/O Buffer** Isolated Power and Ground for the output buffers to provide improved noise immunity.
$4 \times$ NC	–	**No Connect** Please do not connect. Reserved for future use, i.e. E3: A21, J4: A22, see ballout in **Figure 2** on **Page 10**.

1.5 Functional Block Diagram

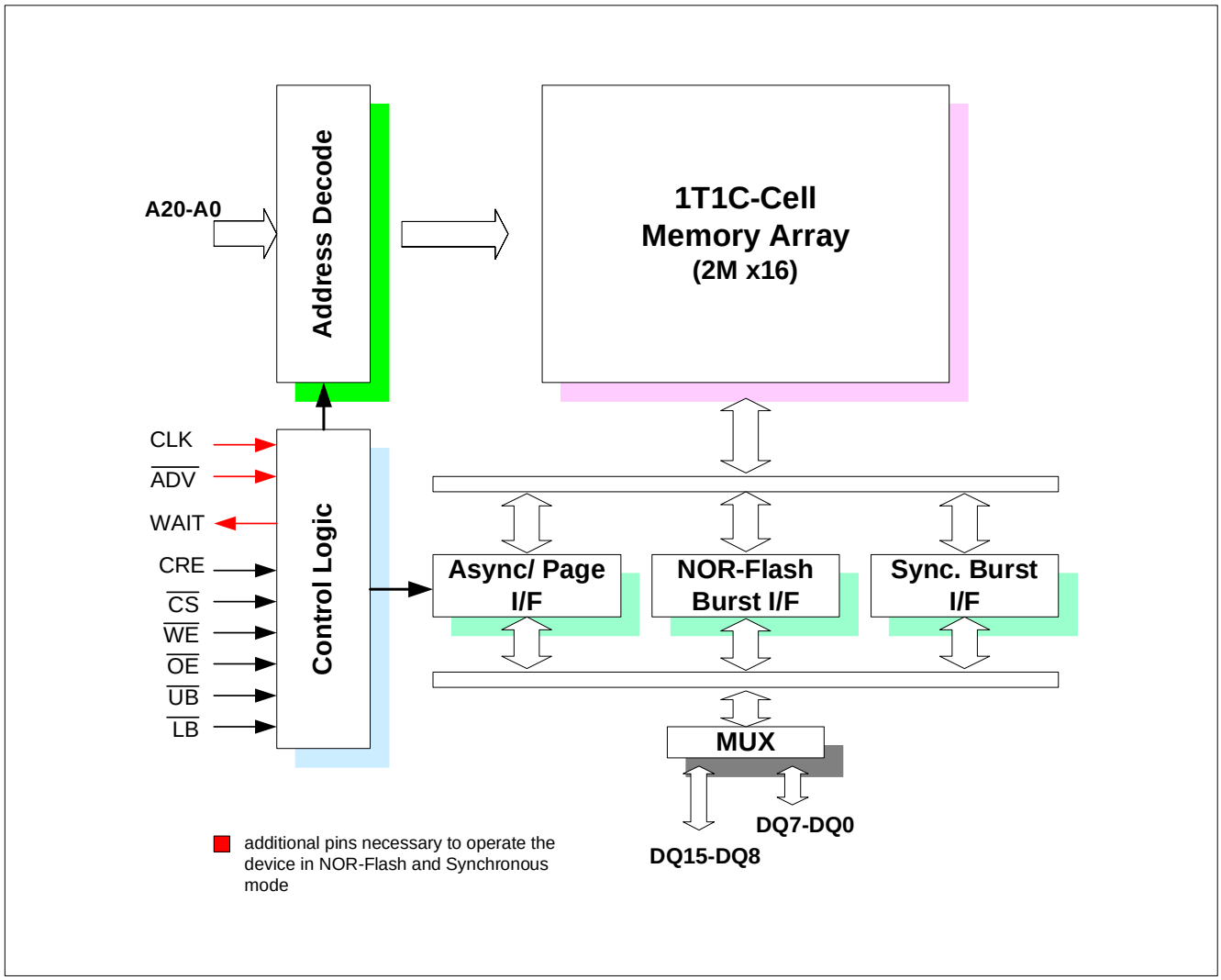


Figure 3 Functional Block Diagram

1.6 Commands

The supported command set depends on the selected operation mode. By default the CellularRAM device is reset to the asynchronous SRAM-type mode after power-up. To put the device in a different operation mode the Bus Configuration Register must be programmed first accordingly. The valid control input states and sequences are listed below for the different operation modes. Other control signal combinations are not supported.

1.6.1 Commands Supported in SRAM-Type Mode

In the SRAM-type operation mode all commands are of asynchronous nature. **Table 3** lists the asynchronous commands supported in SRAM-type mode. CLK has to be held low for entire asynchronous mode operation.

Table 3 Asynchronous Command Table (SRAM-Type Mode)

Operation Mode	Power Mode	$\overline{CS}$	$\overline{ADV}$	$\overline{WE}$	$\overline{OE}$	$\overline{UB}$/ $\overline{LB}$	CRE	A19	A20 - A0	DQ15:0
READ	Active	L	L	H	L	L[1)]	L	V	ADR	DOUT
WRITE	Active	L	L	L	X[2)]	L[1)]	L	V	ADR	DIN
SET CONTROL REGISTER	Active	L	L	L	X[2)]	X	H	L H	RCR DIN BCR DIN	X
NO OPERATION	Standby~Active[3)]	L	X	H	H	X	L	X	X	High-Z
DESELECT	Standby	H	X	X	X	X	X	X	X	High-Z
DPD[4)]	Deep Power Down	H	X	X	X	X	X	X	X	High-Z

1) **Table 3** reflects the behaviour if $\overline{UB}$ and $\overline{LB}$ are asserted to low. If only either of the signals, $\overline{UB}$ or $\overline{LB}$, is asserted to low only the corresponding data byte will be output or written ($\overline{UB}$ enables DQ15 - DQ8, $\overline{LB}$ enables DQ7 - DQ0).

2) During a write access invoked by $\overline{WE}$ set to low the $\overline{OE}$ signal is ignored.

3) Stand-by power mode applies only to the case when $\overline{CS}$ goes low from DESELECT while no address change occurs. Toggling address results in active power mode. Also, NO OPERATION from any active power mode by keeping $\overline{CS}$ low consumes the power higher than stand-by mode.

4) Deep power down is maintained until control register is re-programmed to disable DPD control bit (RCR Bit 4).

Note: 'L' represents a low voltage level, 'H' a high voltage level, 'X' represents "Don't Care", 'V' represents "Valid".

Table 4 Description of Commands (SRAM-Type Mode)

Mode	Description
READ	The READ command is used to perform an asynchronous read cycle. The signals, $\overline{UB}$ and $\overline{LB}$, define whether only the lower, the upper or the whole 16-bit word is output.
WRITE	The WRITE command is used to perform an asynchronous write cycle. The data is latched on the rising edge of either $\overline{CS}$, $\overline{WE}$, $\overline{UB}$, $\overline{LB}$, whichever comes first. The signals, $\overline{UB}$ and $\overline{LB}$, define whether only the lower, the upper or the whole 16-bit word is latched into the CellularRAM.
SET CONTROL REGISTER	The control registers are loaded via the address inputs A19, A15 - A0 performing an asynchronous write access. Please refer to the control register description for details. The SCR command can only be issued when the CellularRAM is in idle state.
NO OPERATION	The NOP command is used to perform a no operation to the CellularRAM, which is selected ($\overline{CS}$ = 0). Operations already in progress are not affected. Power consumption of this command mode varies by address change and initiating condition.

Table 4 Description of Commands (SRAM-Type Mode) (cont'd)

Mode	Description
DESELECT	The DESELECT function prevents new commands from being executed by the CellularRAM. The CellularRAM is effectively deselected. I/O signals are put to high impedance state.
DPD	DPD stops all refresh-related activities and entire on-chip circuit operation. Current consumption drops below 25 µA. Wake-up from DPD also requires 150 µs to get ready for normal operation.

1.6.2 Commands Supported in NOR-Flash-Type Mode

In NOR-Flash-type mode read commands are performed on a synchronous base whereas write commands are performed in an asynchronous way.

In synchronous read mode all operations are defined by the states of the control signals $\overline{CS}$, $\overline{ADV}$, $\overline{OE}$, $\overline{WE}$ and $\overline{UB}$, $\overline{LB}$ at the positive (default) edge of the data clock. To put the device in NOR-Flash-type mode the Bus Configuration Register must be programmed first accordingly.

Table 5 lists the truth table for the supported asynchronous write commands, while **Table 5** lists the supported synchronous read commands.

Table 5 Asynchronous Command Table (NOR-Flash-Type Mode)

Operation Mode	Power Mode	$\overline{CS}$	$\overline{ADV}$	$\overline{WE}$	$\overline{OE}$	$\overline{UB}$/$\overline{LB}$	CRE	A19	A20 - A0	DQ15:0
WRITE	Active	L	L	L	X[1]	L[2]	L	V	ADR	DIN
SET CONTROL REGISTER	Active	L	L	L	X[1]	X	H	L H	RCR DIN BCR DIN	X
NO OPERATION	Standby~Active[3]	L	H	H	H	X	L	X	X	High-Z
DESELECT	Standby	H	X	X	X	X	L	X	X	High-Z
DPD[4]	Deep Power Down	H	X	X	X	X	X	X	X	High-Z

1) During a write access invoked by $\overline{WE}$ set to low the $\overline{OE}$ signal is ignored.

2) **Table 5** reflects the behaviour if $\overline{UB}$ and $\overline{LB}$ are asserted to low. If only either of the signals, $\overline{UB}$ or $\overline{LB}$, is asserted to low only the corresponding data byte will be output or written ($\overline{UB}$ enables DQ15 - DQ8, $\overline{LB}$ enables DQ7 - DQ0).

3) Stand-by power mode applies only to the case when $\overline{CS}$ goes low from DESELECT while no address change occurs. NO OPERATION from any active power mode by keeping $\overline{CS}$ low consumes the power higher than stand-by mode.

4) Deep power down is maintained until control register is re-programmed to disable the bit for deep power down (RCR Bit 4).

Note: 'L' represents a low voltage level, 'H' a high voltage level, 'X' represents "Don't Care", 'V' represents "Valid".

Table 6 Synchronous Command Table (NOR-Flash-Type Mode)

Operation Mode	Power Mode	CLK	$\overline{CS}$	$\overline{ADV}$	$\overline{WE}$	$\overline{UB}$/$\overline{LB}$[1]	CRE	A20 - A0	DQ15:0
BURST INIT	Active	L->H	L	L	H	X	L	ADR	X
BURST READ	Active	L->H	L	H	H	L[2]	L	X	DOUT[3]
NO OPERATION	Standby~Active[4]	L->H	L	H	H	X	L	X	High-Z[5]
DESELECT	Standby	L->H	H	X	X	X	X	X	High-Z
DPD[6]	Deep Power Down	L	H	X	X	X	X	X	High-Z

1) $\overline{OE}$ does the same function to all DQ pins with $\overline{UB}$ and $\overline{LB}$ during read operation.

2) **Table 6** reflects the behaviour if $\overline{UB}$ and $\overline{LB}$ are asserted to low. If only either of the signals, $\overline{UB}$ or $\overline{LB}$, is asserted to low only the corresponding data byte will be output or written ($\overline{UB}$ enables DQ15 - DQ8, $\overline{LB}$ enables DQ7 - DQ0). If both signals are disabled the device is put in deselect mode.

3) Output driver controlled by the asynchronous $\overline{OE}$ signal
4) Stand-by power mode applies only to the case when $\overline{CS}$ goes low from DESELECT while no address change occurs. NO OPERATION from any active power mode by keeping $\overline{CS}$ low consumes the power higher than stand-by mode.
5) The asynchronous $\overline{OE}$ control signal has to be asserted to 'H'.
6) Deep power down is maintained until control register is re-programmed to disable the bit for deep power down (RCR Bit 4).

Note: 'L' represents a low voltage level, 'H' a high voltage level, 'X' represents "Don't Care", 'V' represents "Valid".

Table 7 Description of Commands in NOR-Flash Type Mode

Mode	Description
WRITE	The WRITE command is used to perform an asynchronous write cycle. While the address is latched by the rising edge of $\overline{ADV}$, the data is latched by the rising edge of either $\overline{CS}$, $\overline{WE}$, $\overline{UB}$, $\overline{LB}$, whichever comes first. The signals, $\overline{UB}$ and $\overline{LB}$, define whether only the lower, the upper or the whole 16-bit word is latched into the CellularRAM.
BURST INIT	The BURST INIT command is used to initiate a synchronous burst read access and to latch the burst start address. The burst length is determined by the $\overline{bit2}$ - $\overline{bit0}$ in the Bus Configuration Register.
BURST READ	The BURST READ command is used to perform a synchronous burst read access. The first data is output after the number of clock cycles as defined by the programmed latency mode.
SET CONTROL REGISTER	The control registers are loaded via the address inputs A19, A15 - A0 performing an asynchronous NOR-Flash type write access. Please refer to the control register description for details. The SCR command can only be issued when the CellularRAM is in idle state and no bursts are in progress.
NO OPERATION	The NOP command is used to perform a no operation to the CellularRAM, which is selected ($\overline{CS}$ = 0). Operations already in progress are not affected.
DESELECT	The DESELECT function prevents new commands from being executed by the CellularRAM. The CellularRAM is effectively deselected. I/O signals are put to high impedance state.
DPD	DPD stops all refresh-related activities and entire on-chip circuit operation. Current consumption drops below 25 µA. Wake-up from DPD also requires 150 µs to get ready for normal operation.

1.6.3 Commands Supported in Synchronous Mode

In bi-directional synchronous mode read and write operations are performed on a complete synchronous base. To put the device in full synchronous mode the Bus Configuration Register must be programmed first accordingly. **Table 8** shows the truth table for the supported synchronous read/write commands.

Table 8 Synchronous Command Table (Full Synchronous Mode)

Operation Mode	Power Mode	CLK	$\overline{CS}$	$\overline{ADV}$	$\overline{WE}$	$\overline{UB}$/ $\overline{LB}$[1]	CRE	A19	A20 - A0	DQ15:0
BURST INIT READ	Active	L->H	L	L	H	X	L	V	ADR	X
BURST READ	Active	L->H	L	H	X	L[2]	X	X	X	DOUT[3]
BURST INIT WRITE	Active	L->H	L	L	L	X	L	V	ADR	X
BURST WRITE	Active	L->H	L	H	X	L[2]	X	X	X	DIN
SET CONTROL REGISTER	Active	L->H	L	L	L	X	H	L H	RCR DIN BCR DIN	X
NO OPERATION	Standby~Active[4]	L->H	L	H	H	X	L	X	X	High-Z[5]
DESELECT	Standby	L->H	H	X	X	X	X	X	X	High-Z
DPD[6]	Deep Power Down	L	H	X	X	X	X	X	X	High-Z

1) $\overline{OE}$ does the same function to all DQ pins with $\overline{UB}$ and $\overline{LB}$ during read operation.

2) **Table 8** reflects the behaviour if $\overline{UB}$ and $\overline{LB}$ are asserted to low. If only either of the signals, $\overline{UB}$ or $\overline{LB}$, is asserted to low only the corresponding data byte will be output or written ($\overline{UB}$ enables DQ15 - DQ8, $\overline{LB}$ enables DQ7 - DQ0). If both signals are disabled the device is put in deselect mode.

3) Output driver controlled by the asynchronous $\overline{OE}$ control signal

4) Stand-by power mode applies only to the case when $\overline{CS}$ goes low from DESELECT while no address change occurs. NO OPERATION from any active power mode by keeping $\overline{CS}$ low consumes the power higher than stand-by mode.

5) The asynchronous $\overline{OE}$ control signal has to be asserted to ‘H’.

6) Deep power down is maintained until control register is re-programmed to disable the bit for deep power down (RCR Bit 4).

Note: ‘L’ represents a low voltage level, ‘H’ a high voltage level, ‘X’ represents “Don’t Care”, ‘V’ represents “Valid”.

Table 9 Description of Commands in Synchronous Mode

Mode	Description
BURST INIT	The BURST INIT command is used to initiate a synchronous burst access and to latch the burst start address. The burst length is determined by the setting in the Bus Configuration Register.
BURST READ	The BURST READ command is used to perform a synchronous burst read access. The first data is output after the number of clock cycles as defined by the programmed latency mode.
BURST WRITE	The BURST WRITE command is used to perform a synchronous burst write access. The point of time when the first data is written is indicated by the WAIT signal. It varies with the selected clock frequency and the occurrence of a refresh cycle.
SET CONTROL REGISTER	The control registers are loaded via the address inputs A19, A15 - A0 performing a single word burst. Please refer to the control register description for details. The SCR command can only be issued when the CellularRAM is in idle state and no bursts are in progress.
NO OPERATION	The NOP command is used to perform a no operation to the CellularRAM, which is selected ($\overline{CS}$ = 0). Operations already in progress are not affected.

Table 9 Description of Commands in Synchronous Mode (cont'd)

Mode	Description
DESELECT	The DESELECT function prevents new commands from being executed by the CellularRAM. The CellularRAM is effectively deselected. I/O signals are put to high impedance state.
DPD	DPD stops all refresh-related activities and entire on-chip circuit operation. Current consumption drops below 25 µA. Wake-up from DPD also requires 150 µs to get ready for normal operation.

2 Functional Description

2.1 Power-Up and Initialization

The power-up and initialization sequence guarantees that the device is preconditioned to the user's specific needs. Like conventional DRAMs, the CellularRAM must be powered up and initialized in a predefined manner. V_{DD} and V_{DDQ} must be applied at the same time to the specified voltage while the input signals are held in "DESELECT" state ($\overline{CS}$ = High).

After power on, an initial pause of 150 µs is required prior to the control register access or normal operation. Failure to follow these steps may lead to unpredictable start-up modes.

Please note the default operation mode after power up is the asynchronous SRAM I/F mode (see **Chapter 2.4**).

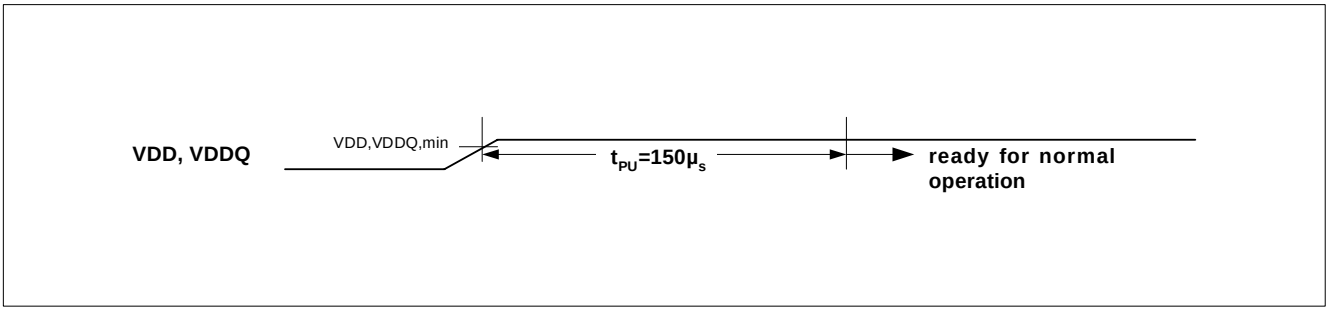


Figure 4 Power Up Sequence

2.2 Access To The Control Register Map

Write-only access to the control register map is enabled by applying the SCR command asserting the CRE-pin to high. In combination with CRE set to high, Pin A19 designates the operation to one of either control registers. Pin A19 set to low selects the Refresh Control Register (RCR), Pin A19 set to high addresses the Bus Configuration Register (BCR).

Write and read access to the control registers is also available at S/W entry method. For details, please refer to **"Appendix B: S/W Register Entry Mode ("4-cycle method")" on Page 51**.

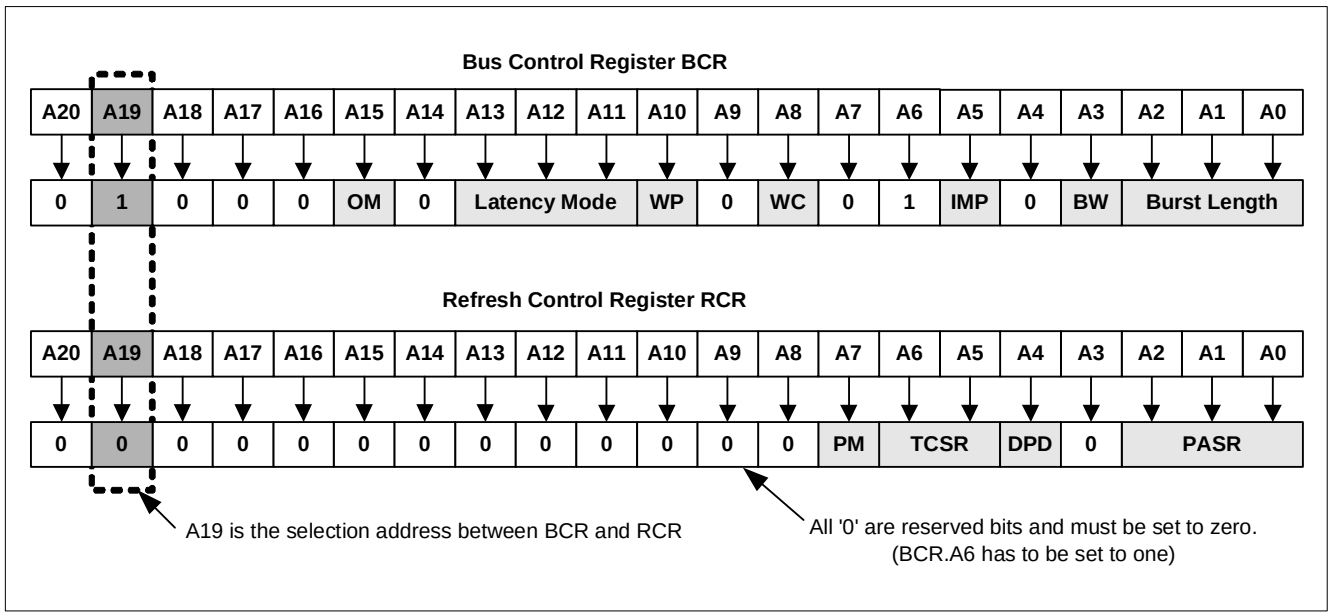


Figure 5 The two Control Registers

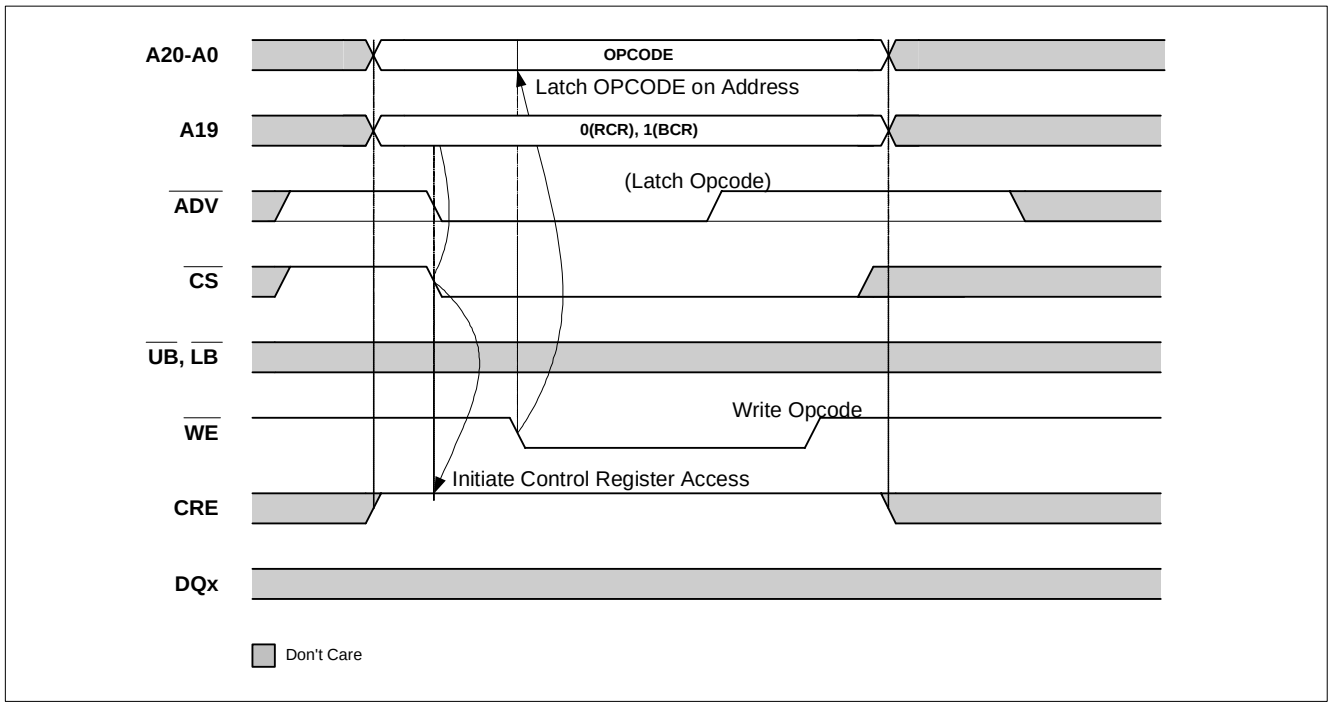


Figure 6 Control Register Write in SRAM-Type Mode

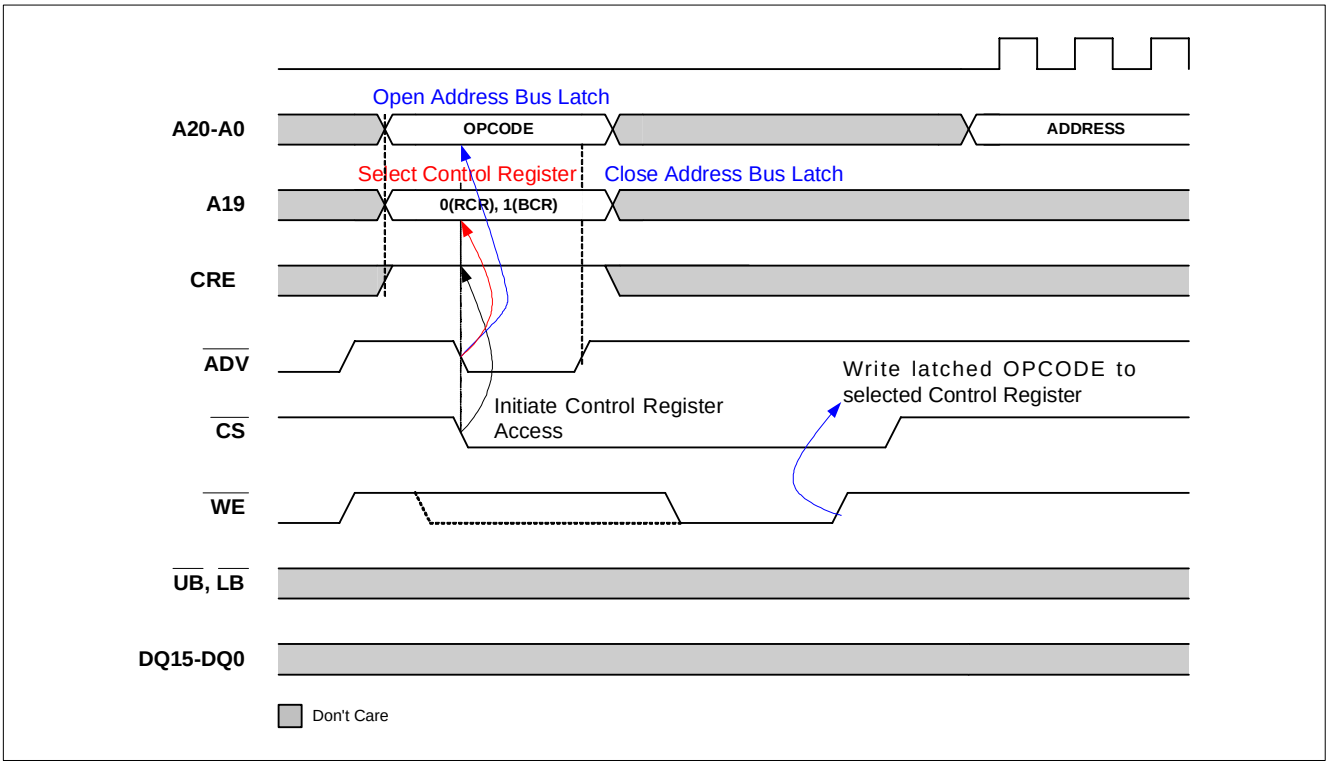


Figure 7 Control Register Write in NOR-Flash-Type Mode

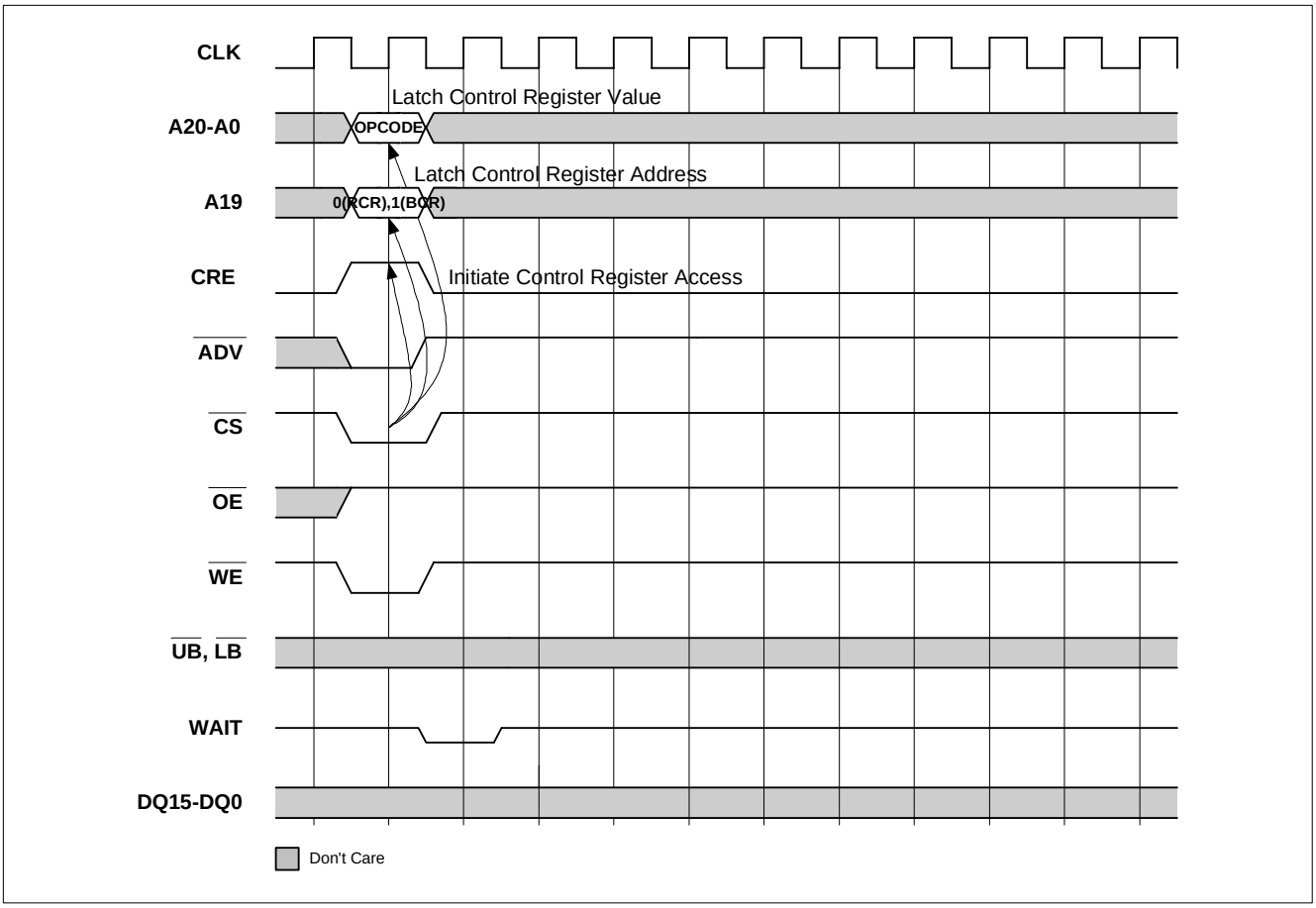


Figure 8 Control Register Write in Synchronous Mode

2.3 Refresh Control Register

The Refresh Control Register (RCR) allows to save stand-by power additionally by making use of the Temperature-Compensated Self Refresh (TCSR), Partial-Array Self Refresh (PASR) and Deep Power Down (DPD) features. The Refresh Control Register is programmed via the Control Register Set command (with CRE = 1 and A19 = 0) and retains the stored information until it is reprogrammed or the device loses power.

Please note that the RCR contents can only be set or changed when the CellularRAM is in idle state.

RCR
Refresh Control Register **(CRE, A19 = 10_B)**

A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	**RS**	**0**											**PM**	**TCSR**		**DPD**	**0**	**PASR**		

Field	Bits	Type[1)]	Description
RS	19	w	**Register Select** 0 set to 0 to select this RCR (= 1 to select BCR).
PM	7	w	**Page Mode Enable/Disable** In asynchronous operation mode the user has the option to toggle A0 - A3 in a random way at higher rate (20 ns vs. 70 ns) to lower access times of subsequent reads with 16-word boundary. In synchronous mode this option has no effect. The max. page length is 16 words. Please note that as soon as page mode is enabled the $\overline{CS}$ low time restriction applies. This means that the $\overline{CS}$ signal must not be kept low longer than t_{CSL} = 10 µs. Please refer to **Figure 15**. 0 page mode disabled (default) 1 page mode enabled
TCSR	[6:5]	w	**Temperature Compensated Self Refresh** The 2-bit wide TCSR field features four different temperature ranges to adjust the refresh period to the actual case temperature. Since DRAM technology requires higher refresh rates at higher temperature this is a second method to lower power consumption in case of low or medium temperatures. 11 +85 °C (default) 00 +70 °C 01 +45 °C 10 +15 °C
DPD	4	w	**Deep Power Down Enable/Disable** The DPD control bit puts the CellularRAM device in an extreme low power mode cutting current consumption to less than 25 µA. Stored memory data is not retained in this mode. Though the settings of both control registers RCR and BCR are also stored during DPD. 0 DPD enabled 1 DPD disabled (default)

Field	Bits	Type[1)]	Description
PASR	[2:0]	w	**Partial Array Self Refresh** The 3-bit PASR field is used to specify the active memory array. The active memory array will be kept periodically refreshed whereas the disabled parts will be excluded from refresh and previously stored data will get lost. The normal operation still can be executed in disabled array, but stored data is not guaranteed. This way the customer can dynamically adapt the memory capacity in steps of 8 Mbit (4Mbit at lowest) to one's need without paying a power penalty. Please refer to **Figure 9**. 000 entire memory array (default) 001 lower 1/2 of the memory array (16 Mb) 010 lower 1/4 of the memory array (8 Mb) 011 lower 1/8 of the memory array (4 Mb) 100 zero 101 upper 1/2 of the memory array (16 Mb) 110 upper 1/4 of the memory array (8 Mb) 111 upper 1/8 of the memory array (4 Mb)
Res	20, [18:8], 3	w	**Reserved** must be set to '0'

1) w: write-only access

2.3.1 Partial Array Self Refresh (PASR)

By applying PASR the user can dynamically customize the memory capacity to one's actual needs in normal operation mode and standby mode. With the activation of PASR there is no longer a power penalty paid for the larger CellularRAM memory capacity in case only e.g. 8 Mbits are used by the host system.

Bit2 down to bit0 specify the active memory array and its location (starting from bottom or top). The memory parts not used are powered down immediately after the mode register has been programmed. Advice for the proper register setting including the address ranges is given in **Figure 9**.

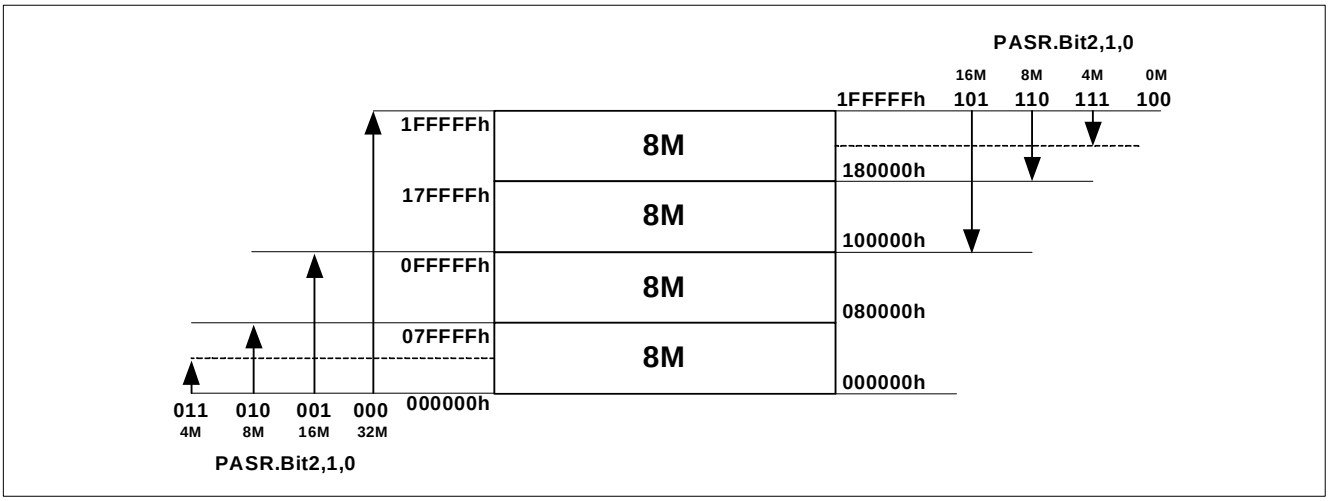


Figure 9 PASR Programming Scheme

PASR is effective in normal operation and standby mode as soon as it has been configured by register programming. Default setting is the entire memory array.

Figure 10 shows an exemplary PASR configuration where it is assumed that the application uses max. 8 Mbit out of 32 Mbit.

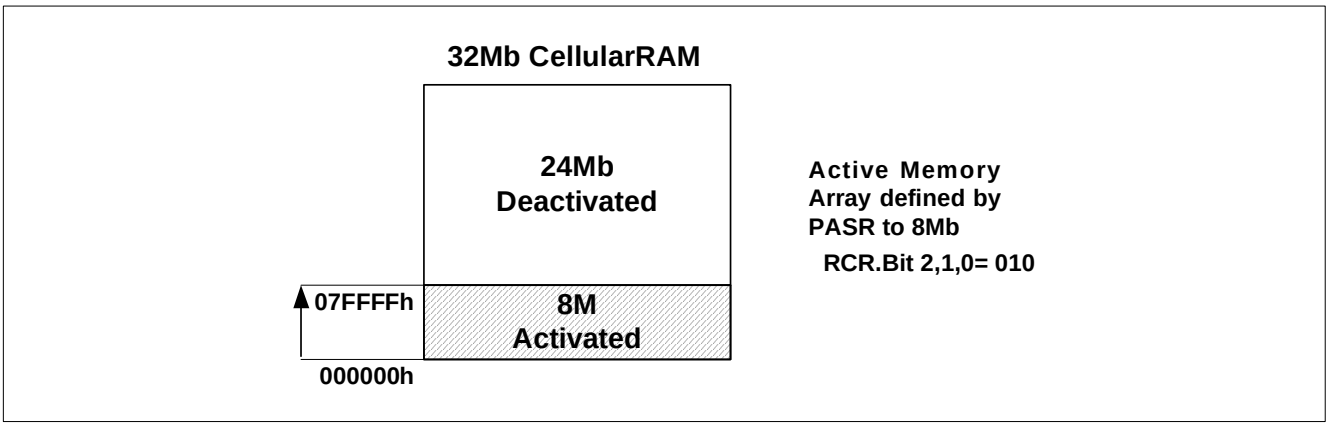


Figure 10 PASR Configuration Example

2.3.2 Deep Power Down Mode

To put the device in deep power down mode the DPD control bit must be asserted to low. Once set into this extreme low power mode current consumption is cut down to less than 25 µA.

All internal voltage generators inside the CellularRAM are switched off and the internal self-refresh is stopped. This means that all stored memory information will be lost by entering DPD. Only the register values of BCR and RCR are kept valid during DPD. To leave the Deep Power Down mode again the Refresh Configuration Register has to be accessed and the DPD bit has to be programmed to high level voltage.

A guard time of at least 150 µs has to be met where no commands beside a NOP must be applied to re-enter again standby or idle mode.

2.3.3 Temperature Compensated Self Refresh (TCSR)

The 2-bit wide TCSR field features four different temperature ranges to adjust the refresh period to the actual case temperature. DRAM technology requires higher refresh rates at higher temperature. At low temperature the refresh rate can be reduced, which reduces as well the standby current of the chip. This feature can be used in addition to PAR to lower power consumption in case of low or medium temperatures. Please refer to **Table 10**.

2.3.4 Power Saving Potential in Standby When Applying PASR, TCSR or DPD

Table 10 demonstrates the currents in standby mode when PASR, TCSR or DPD is applied.

Table 10 Standby Currents When Applying PASR, TCSR or DPD

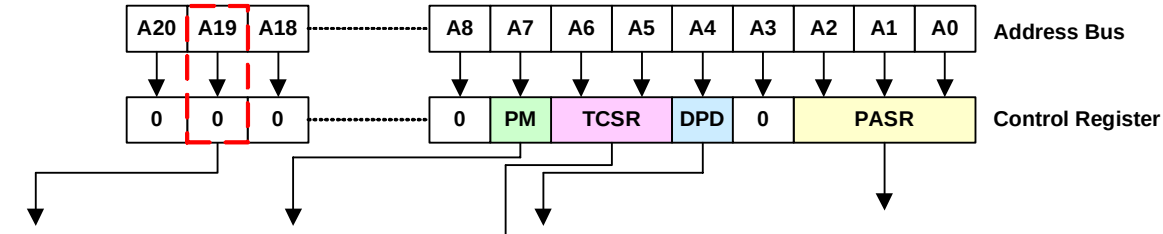
Operation Mode	Power Mode	PASR	Bit Controlled	Wake-Up Phase	Active Array	Standby [µA]			
NO OPERATION/ DESELECT	STANDBY	TCSR	RCR.Bit6-5	–	–	85°	70°	45°	15°
		PASR	RCR.Bit2-0	–	Full 1/2 1/4 1/8 0	90(120) 80(105) 70(90) 60(75) 50(60)	75(100) 68(90) 62(80) 55(70) 50(60)	60(80) 56(75) 53(70) 52(65) 50(60)	50(60) 50(60) 50(60) 50(60) 50(60)
DPD	DEEP POWER DOWN	DPD	RCR.Bit4	~150 µs	0	25.0			

2.3.5 Page Mode Enable/Disable

In asynchronous operation mode, the user has the option to enable page mode to toggle A0 - A3 in random way at higher cycle rate (20 ns vs. 70 ns) to lower access times of subsequent reads within 16-word boundary. Write operation is not supported in the manner of page mode access. In synchronous mode, this option has no effect. The max. page length is 16 words, so which A0 - A3 is regarded as page-mode address. If the access needs to cross the boundary of 16-word (any difference in A20 - A4), then it should start over new random access cycle, which is the same as asynchronous read operation.

Please note that as soon as page mode is enabled the $\overline{CS}$ low time restriction applies. This means that the $\overline{CS}$ signal must not kept low longer than t_{CSL} = 10 µs. Please refer to **Figure 15**.

Refresh Control Register (RCR)



Control Register Select

A19	control reg
0	RCR
1	BCR

Page Mode Bit

A7	page mode
0	disabled (def.)
1	enabled

Deep Power Down Mode

A4	power down
0	enabled
1	disabled (def.)

Partial Array Self Refresh

A2	A1	A0	refreshed memory area
0	0	0	entire memory array (def.)
0	0	1	lower 1/2 of memory array
0	1	0	lower 1/4 of memory array
0	1	1	lower 1/8 of memory array
1	0	0	zero
1	0	1	upper 1/2 of memory array
1	1	0	upper 1/4 of memory array
1	1	1	upper 1/8 of memory array

Temperature-Compensated Self-Refresh

A6	A5	max. case temp.
1	1	+85°C (def.)
0	0	+70°C
0	1	+45°C
1	0	+15°C

A20, A18....A8, A3: reserved, must be set to '0'.

2.4 Bus Control Register

The Bus Control Register (BCR) specifies the interface configurations. For the various configuration options please refer to the register description below. The Bus Control Register is programmed via the Control Register Set command (with CRE = 1 and A19 = 1) and retains the stored information until it is reprogrammed or the device loses power.

Please note that the BCR contents can only be set or changed when the CellularRAM is in idle state.

Note: Bit 9 must be set to "0" and bit 6 to "1" for proper operation.

BCR
Bus Control Register **(CRE, A19 = 11_B)**

A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	**1**	**0**			**OM**	**0**	**Latency Mode**			**WP**	**0**	**WC**	**0**	**1**	**IMP**	**0**	**BW**	**Burst Length**		

Field	Bits	Type[1)]	Description
RS	19	w	**Register Select** 1 set to 1 to select this BCR (= 0 to select RCR).
OP-MODE	15	w	**Operation Mode** The CellularRAM supports three different interface access protocols, • the SRAM-type protocol with asynchronous read and write accesses • the NOR-FLASH-type protocol with synchronous read and asynchronous write accesses • the FULL SYNCHRONOUS mode with synchronous read and synchronous write accesses Operating the device in synchronous mode maximizes bandwidth. The NOR-Flash type mode is the recommended mode for legacy baseband systems which are not able to run the synchronous write protocol. The OPMODE bit defines whether the device is operating in synchronous (fully or partially) mode or asynchronous mode. 0 NOR-FLASH-type mode read: synchronous burst mode write: asynchronous access mode 0 FULL SYNCHRONOUS mode read: synchronous burst mode write: synchronous burst mode The mode of write operation, NOR-FLASH or FULL SYNCHRONOUS, is adaptively detected: This is done by detecting a rising clock edge during ADV valid. If a rising clock edge occurs within ADV valid, FULL SYNCHRONOUS write is detected. If there is no rising clock edge then NOR FLASH write is detected. Please refer to **Figure 22** on **Page 40** for asynchronous write and to **Figure 25** on **Page 43** for synchronous write. 1 SRAM-type mode (default) read: asynchronous access mode write: asynchronous access mode
LAT	[13:11}	w	**Latency Mode** The latency mode has to be adjusted to the desired burst frequency. Depending on the programmed latency, driving 1st data output is delayed by the number of clock cycles as specified in this field counting from the address valid strobe signal, $\overline{ADV}$. 010 latency code 2, max 66 MHz burst clock frequency 011 latency code 3 (default), max 104 MHz burst clock frequency *Note: All others reserved.*

Field	Bits	Type[1)]	Description
WP	10	w	**WAIT Polarity** The WAIT polarity control bit allows the user to define the polarity of the WAIT output signal. The WAIT output line is used during a synchronous read burst to signal when the output data is invalid. 0 active low 1 active high (default)
WC	8	w	**WAIT Configuration** The WAIT signal configuration control bit specifies whether the WAIT signal is asserted at the time of the delay or whether it is asserted one clock cycle in advance. 0 WAIT is asserted during the delay 1 WAIT is asserted one data cycle before the delay (default)
IMP	5	w	**Output Impedance** For adaptation to different system characteristics the output impedance can be configured. 0 Full drive for 50 Ω systems (default) 1 Quarter drive
BW	3	w	**Burst Wrap** The burst wrap control bit defines whether there is a wrap around within a burst access or not. In case of fixed 8-word burst length, this means that after word7, word0 is going to be output in wrap mode. In case of continuous burst mode the internal address counter will wrap from the last address, $1FFFFF_H$ to 000000_H regardless of the setting. Please note this setting is only used for burst read mode, since burst write mode is always continuous. 0 wrap 1 no wrap (default)
BL	[2:0]	w	**Burst Length (Burst Read only)** Via the burst length field the user can select between fixed burst lengths of 4, 8, and 16 and any arbitrary burst length by choosing the continuous mode option. In continuous mode the burst length is controlled by the active low period of the read control lines CS and OE. Please note this setting is only used for burst read mode. Burst write mode is always continuous independent of this register setting. 001 4-word burst 010 8-word burst 011 16-word burst 111 continuous (default)
Res	20, [18:16], 14, 9, 7, 4	w	**Reserved** must be set to ‘0’

1) w: write-only access

2.4.1 Latency Modes

The latency mode defines the number of clock cycles which pass before the first output data is valid within a read burst access (counting from the clock edge where $\overline{ADV}$ was detected low). The number of inserted wait cycles increases along with the input clock frequency. Please refer to **Table 11** for the proper setting.

Please note that the first access delay might be extended by another 1-3 wait cycles in case the burst read or write access collides with an ongoing self-refresh operation.

Table 11 Latency Mode Configuration

Latency Mode	Max. Input Clock Frequency [MHz]		
	-9.6	**-12.5**	**-15**
0	reserved	reserved	reserved
1	reserved	reserved	reserved
2	66	50	40
3	104	80	66

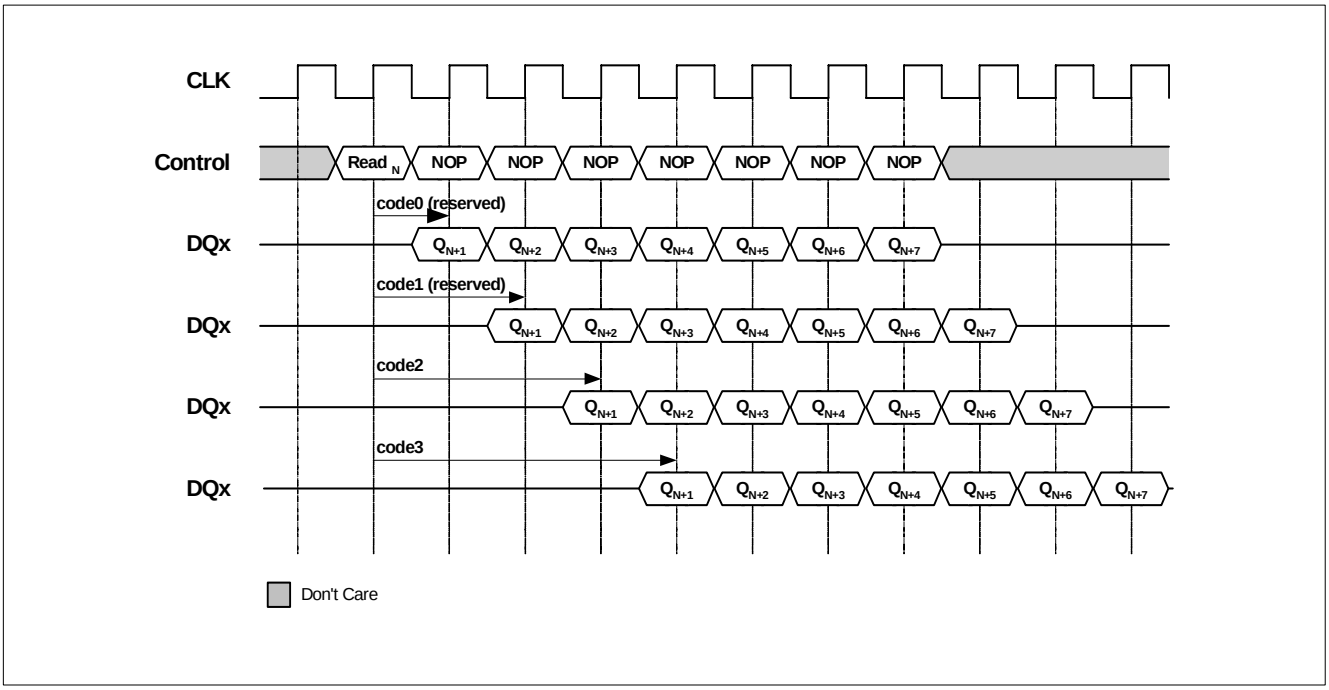


Figure 11 Latency Mode - Functional Diagram

2.4.2 Read Burst Configurations/Sequences

The numbers of words that are read during a burst read access is defined by the burst length field which is programmed in the Bus Control Register. The user can either program fixed burst lengths of 4-words, 8-words or 16-words or operate the device in continuous mode operation. The burst start address is latched by ADV set to low. An internal address counter then increments automatically the address with respect to the programmed burst length.

Continuous burst operation does not stop automatically though a row boundary has been reached. In other words, unlike with fixed burst lengths, a continuous burst goes on until it is actively terminated by bringing CS to high sampled at the valid edge of CLK.

The wrap mode option specifies whether the burst address overflows and restarts at address 0 (A3 - A0) or keeps incrementing. In continuous burst mode, the internal address counter wraps to 000000_H if the operation goes on past the last address, $1FFFFF_H$ regardless of wrap mode setting. For the several possible burst sequences please refer to **Table 12**.

The burst length is only configurable for burst read while burst write uses always continuous burst mode, independent of the burst length setting in the burst control register BCR. Same for burst wrap, in burst write there is always the default - no wrap - used, independent on read burst register setting.

Table 12 Burst Sequences

Burst Length	Starting Address (A3 A2 A1 A0)	Sequential Burst Addressing Scheme (decimal)	
		Wrap On	Wrap Off
4	xx00 xx01 xx10 xx11	0 1 2 3 1 2 3 0 2 3 0 1 3 0 1 2	0 1 2 3 1 2 3 4 2 3 4 5 3 4 5 6
8	x000 x001 x010 x011 x100 x101 x110 x111	0 1 2 3 4 5 6 7 1 2 3 4 5 6 7 0 2 3 4 5 6 7 0 1 3 4 5 6 7 0 1 2 4 5 6 7 0 1 2 3 5 6 7 0 1 2 3 4 6 7 0 1 2 3 4 5 7 0 1 2 3 4 5 6	0 1 2 3 4 5 6 7 1 2 3 4 5 6 7 8 2 3 4 5 6 7 8 9 3 4 5 6 7 8 9 10 4 5 6 7 8 9 10 11 5 6 7 8 9 10 11 12 6 7 8 9 10 11 12 13 7 8 9 10 11 12 13 14
16	0000 0001 0010 … … 1101 1110 1111	0 1 2 … 13 14 15 1 2 3 … 14 15 0 2 3 4 … 15 0 1 … … 13 14 15 … 10 11 12 14 15 0 … 11 12 13 15 0 1 … 12 13 14	0 1 2 … 13 14 15 1 2 3 … 14 15 16 2 3 4 … 15 16 17 … … 13 14 15 … 26 27 28 14 15 16 … 27 28 29 15 16 17 … 28 29 30
Continuous	n	Cn, Cn+1, Cn+2, … Cmax[1], 0, 1, … (default, write burst)	

1) Cmax = $1FFFFF_H$

2.4.3 WAIT Signal in Synchronous Burst Mode

The WAIT signal is used in synchronous burst read mode to indicate to the host system when the output data is invalid. Periods of invalid output data within a burst access might be caused either by first access delays, by delays induced by row boundary crossings or by self-refresh cycles.

To match with the Flash interfaces of different microprocessor types the polarity and the timing of the WAIT signal can be configured. The polarity can be programmed to either active low or active high logic. The timing of the WAIT signal can be adjusted as well. Depending on the BCR setting the WAIT signal will be either asserted at the same time the data becomes invalid or it will be set active already one clock period in advance.

In asynchronous read mode including page mode, the WAIT signal is not used but always stays asserted as BCR bit 10 is specified. In this case, system should ignore WAIT state, since it does not reflect any valid information of data output status.

2.4.4 Hold Data Out Mode

The configuration of Hold Data Out mode is not supported.

Please note that valid data is held always for one clock cycle.

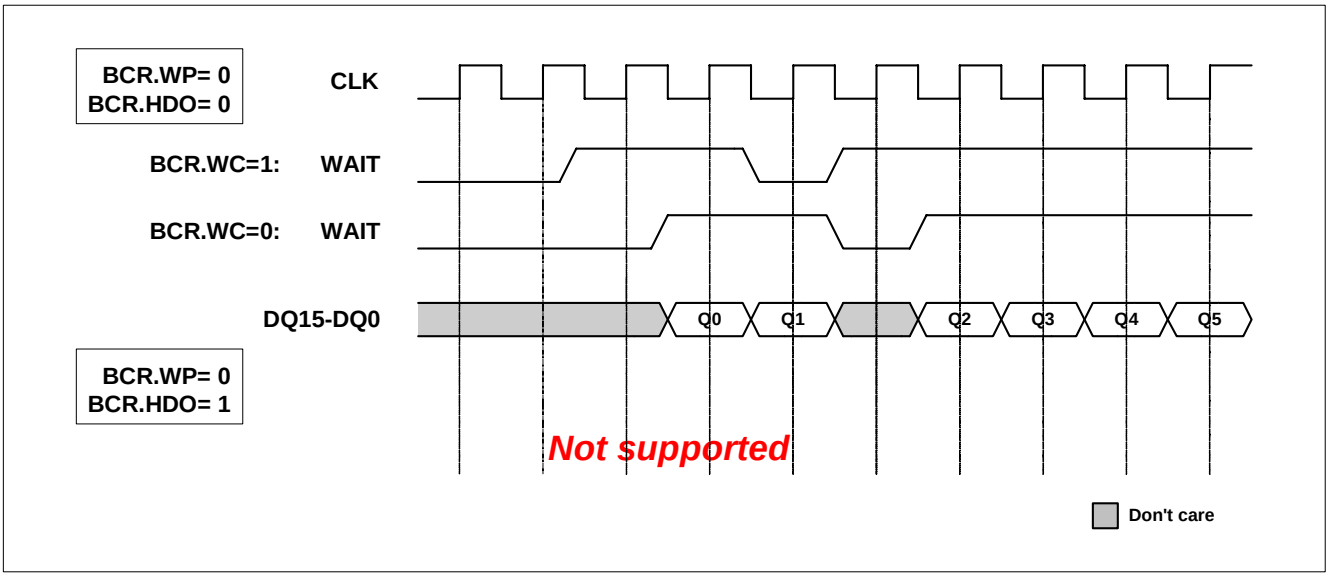
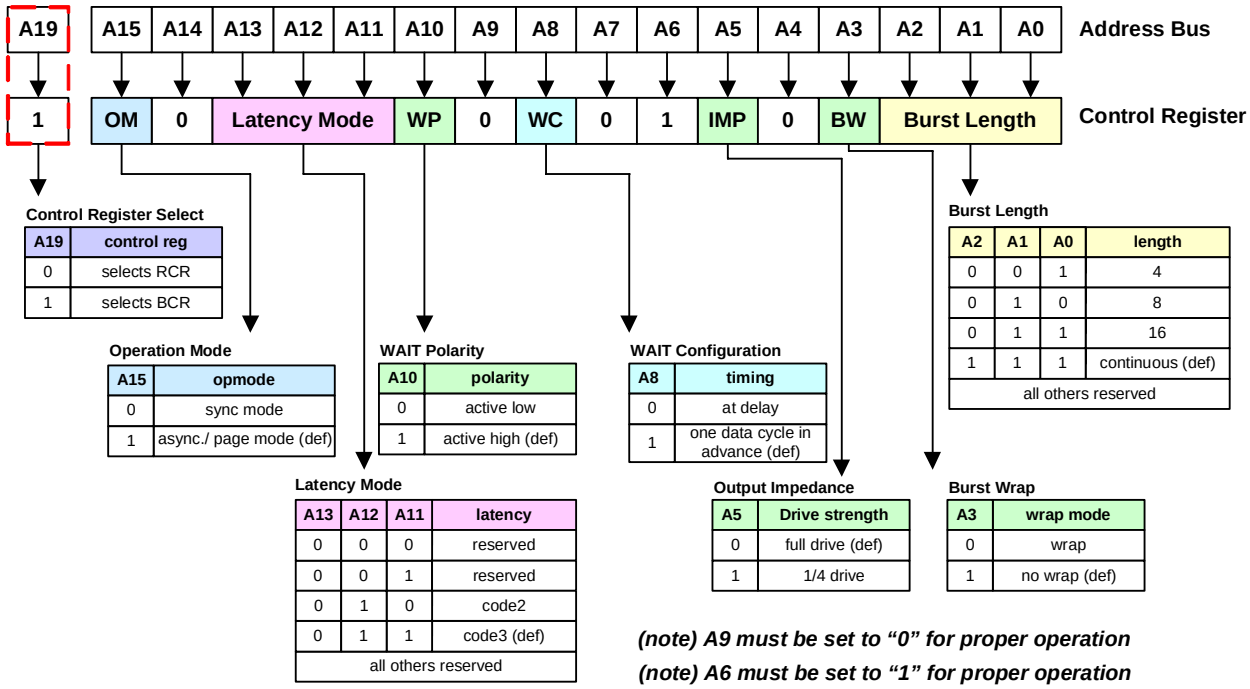


Figure 12 Data Out Configuration

2.5 Self-Refresh

The CellularRAM relieves the host system from triggering and commanding refresh-operations like it is the case with conventional DRAMs by performing automatic self-refresh. Self-refresh operations are autonomously scheduled and performed by the CellularRAM device.

Bus Control Register (BCR)



Control Register Select

A19	control reg
0	selects RCR
1	selects BCR

Operation Mode

A15	opmode
0	sync mode
1	async./ page mode (def)

WAIT Polarity

A10	polarity
0	active low
1	active high (def)

WAIT Configuration

A8	timing
0	at delay
1	one data cycle in advance (def)

Burst Length

A2	A1	A0	length
0	0	1	4
0	1	0	8
0	1	1	16
1	1	1	continuous (def)
all others reserved			

Latency Mode

A13	A12	A11	latency
0	0	0	reserved
0	0	1	reserved
0	1	0	code2
0	1	1	code3 (def)
all others reserved			

Output Impedance

A5	Drive strength
0	full drive (def)
1	1/4 drive

Burst Wrap

A3	wrap mode
0	wrap
1	no wrap (def)

(note) A9 must be set to "0" for proper operation

(note) A6 must be set to "1" for proper operation

2.6 SRAM-Type Mode

In SRAM-type mode the CellularRAM applies the standard asynchronous SRAM protocol to perform read and write accesses.

2.6.1 Asynchronous Read

After power-up the CellularRAM operates per default in asynchronous SRAM-type mode. The synchronous clock line, CLK has to be held low, while address latch signal, $\overline{ADV}$ can be held low for entire read and write operation in this mode or toggled to latch valid address input (refer to **"Asynchronous Write with Address Latch (ADV) Control" on Page 40** for details). WAIT is always asserted as BCR. Bit 10 is programmed, so that the controller should ignore WAIT during asynchronous mode operation.

Reading from the device in asynchronous mode is accomplished by asserting the Chip Select ($\overline{CS}$) and Output Enable ($\overline{OE}$) signals to low while forcing Write Enable ($\overline{WE}$) to high. If the Upper Byte ($\overline{UB}$) control line is set active low then the upper word of the addressed data is driven on the output lines, DQ15 to DQ8. If the Lower Byte ($\overline{LB}$) control line is set active low then the lower word of the addressed data is driven on the output lines, DQ7 to DQ0.

The access time is determined by the triggering input - slowest one in low-going transition - among valid address (t_{AA}), $\overline{CS}$(t_{CO}), $\overline{OE}$(t_{OE}), $\overline{UB}$ or $\overline{LB}$(t_{BA}), or $\overline{ADV}$(t_{AADV}).

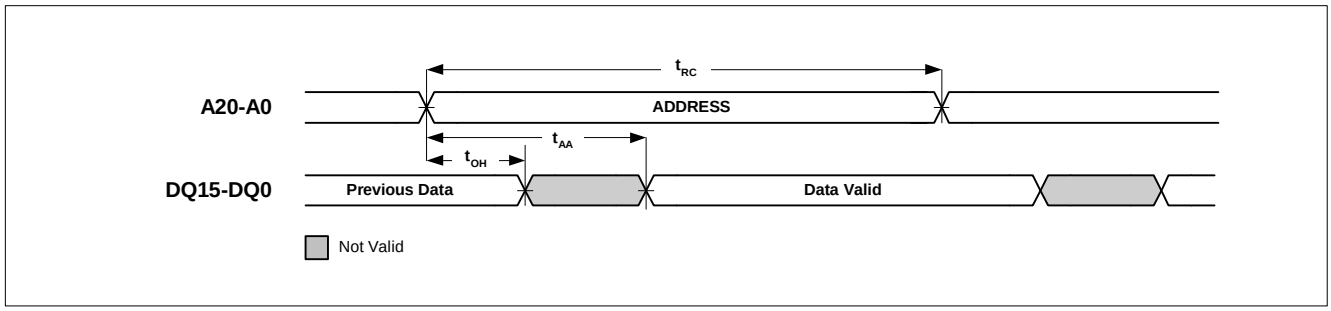


Figure 13 Asynchronous Read - Address Controlled ($\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, $\overline{UB}$ and/or $\overline{LB}$ = V_{IL}, CRE = V_{IL}, $\overline{ADV}$ = V_{IL})

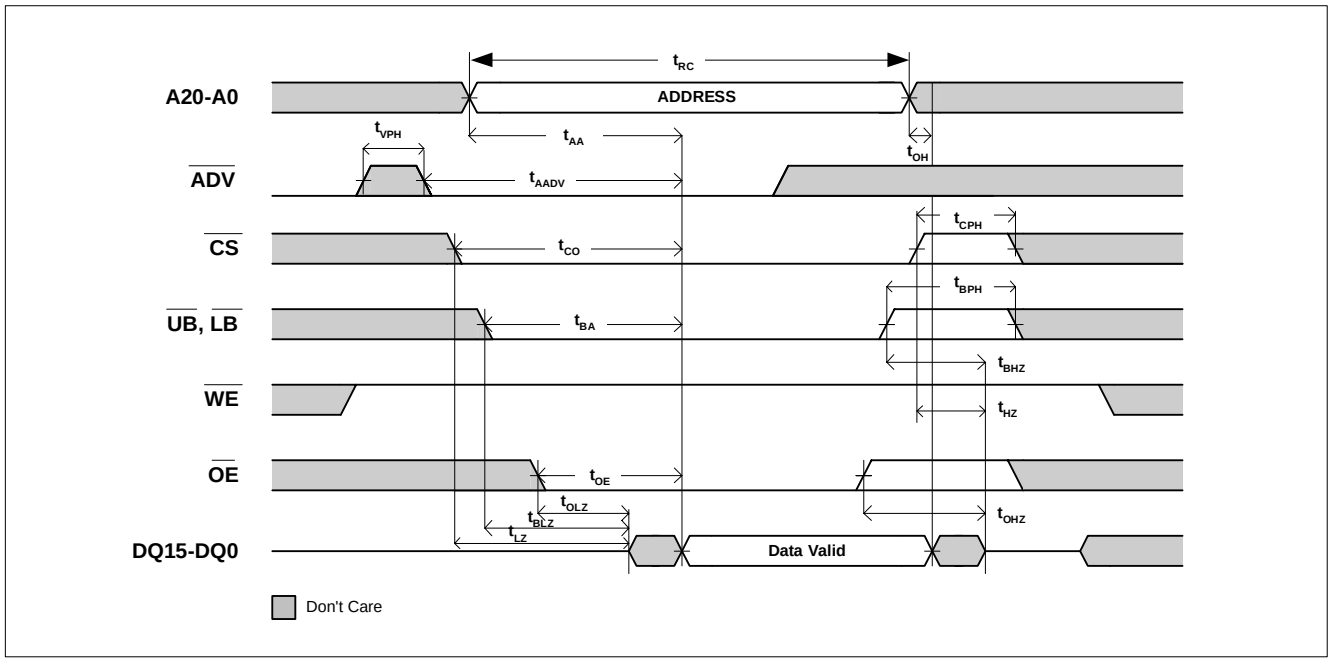


Figure 14 Asynchronous Read ($\overline{WE}$ = V_{IH}, CRE = V_{IL})

2.6.2 Page Mode

If activated by RCR.Bit7 page mode allows to toggle the four lower address bits (A3 to A0) to perform subsequent random read accesses (max. 16-words by A3 - A0) at much faster speed than 1st read access. Page mode operation supports only read access in CellularRAM. As soon as page mode is activated, $\overline{CS}$ low time restriction (t_{CSL}) applies. In case of $\overline{CS}$ staying low longer than t_{CSL} limit, then it is alternative way to toggle non-page address (A20 - A4) no later than $t_{CSL,max}$. Therefore the usage of page mode is only recommended in systems which can respect this limitation. $\overline{ADV}$ has to be held low for entire page operation.

Please see also application note on **Page 50**.

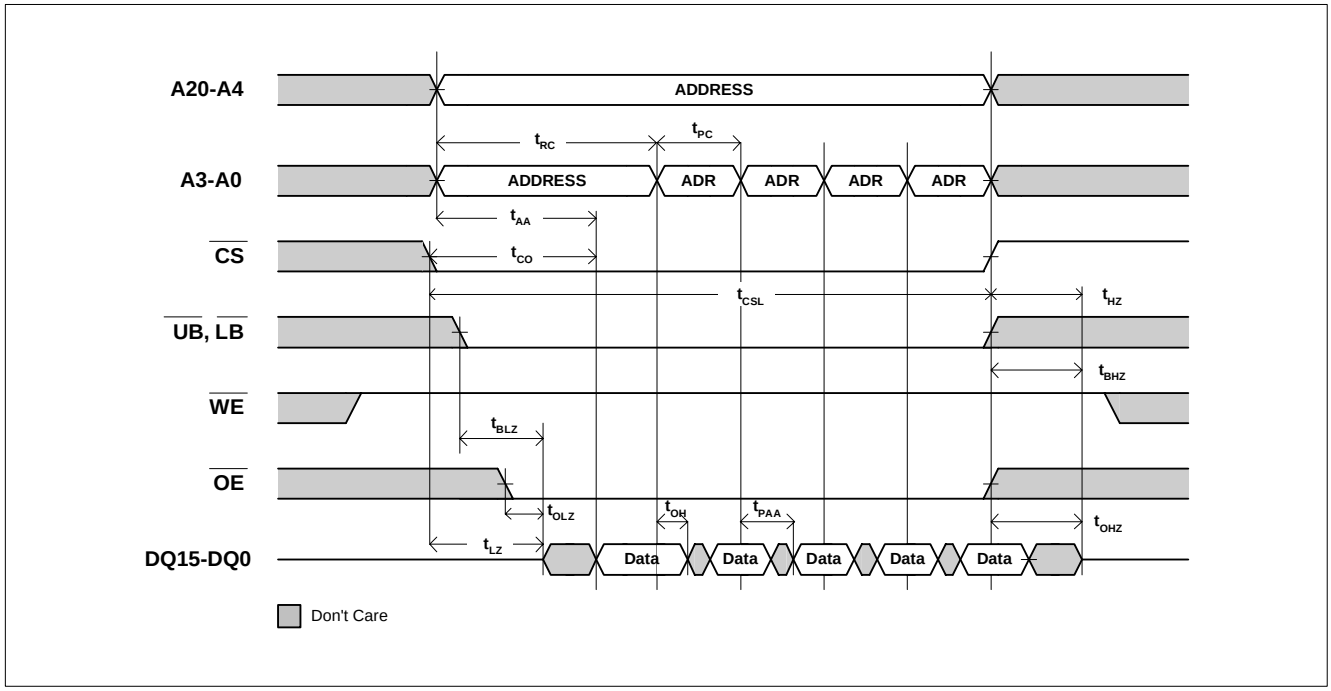


Figure 15 Asynchronous Page Read Mode (CRE = V_{IL}, $\overline{ADV}$ = V_{IL})

Table 13 Timing Parameters - Asynchronous Read

Parameter	Symbol	9.6, 12.5		15		Unit	Notes
		Min.	Max.	Min.	Max.		
Read cycle time	t_{RC}	70	–	85	–	ns	–
Address access time	t_{AA}	–	70	–	85	ns	–
ADV access time	t_{AADV}	–	70	–	85	ns	–
ADV high time	t_{VPH}	5	–	7	–	ns	–
Page address cycle time	t_{PC}	20	–	25	–	ns	–
Page address access time	t_{PAA}	–	20	–	25	ns	–
Output hold from address change	t_{OH}	5	–	6	–	ns	–
Chip select access time	t_{CO}	–	70	–	85	ns	–
$\overline{UB}$, $\overline{LB}$ access time	t_{BA}	–	70	–	85	ns	–
$\overline{OE}$ to valid output data	t_{OE}	–	20	–	25	ns	–
Chip select pulse width low time	t_{CSL}	–	10	–	10	µs	–
Chip select to output active	t_{LZ}	6	–	6	–	ns	–
Chip select disable to high-Z output	t_{HZ}	–	8	–	8	ns	–
$\overline{UB}$, $\overline{LB}$ enable to output active	t_{BLZ}	6	–	6	–	ns	–
$\overline{UB}$, $\overline{LB}$ disable to high-Z output	t_{BHZ}	–	8	–	8	ns	–
Output enable to output active	t_{OLZ}	3	–	3	–	ns	–
Output disable to high-Z output	t_{OHZ}	–	6	–	8	ns	–
$\overline{CS}$ high time when toggling	t_{CPH}	10	–	15	–	ns	–
$\overline{UB}$, $\overline{LB}$ high time when toggling	t_{BPH}	10	–	15	–	ns	–

2.6.3 Asynchronous Write

Writing to the device in asynchronous SRAM mode is accomplished by asserting the Chip Select ($\overline{CS}$) and Write Enable ($\overline{WE}$) signals to low. $\overline{ADV}$ can be used to latch the address (refer to **"Asynchronous Write with Address Latch (ADV) Control" on Page 40** for details) or simply held low for entire write operation. If the Upper Byte ($\overline{UB}$) control line is set active low then the upper word (DQ15 to DQ8) of the data bus is written to the specified memory location. If the Lower Byte ($\overline{LB}$) control line is set active low then the lower word (DQ7 to DQ0) of the data bus is written to the specified memory location. Write operation takes place when either one or both $\overline{UB}$ and $\overline{LB}$ is asserted low. The data is latched by the rising edge of either $\overline{CS}$, $\overline{WE}$, or $\overline{UB}$/$\overline{LB}$ whichever signal comes first.

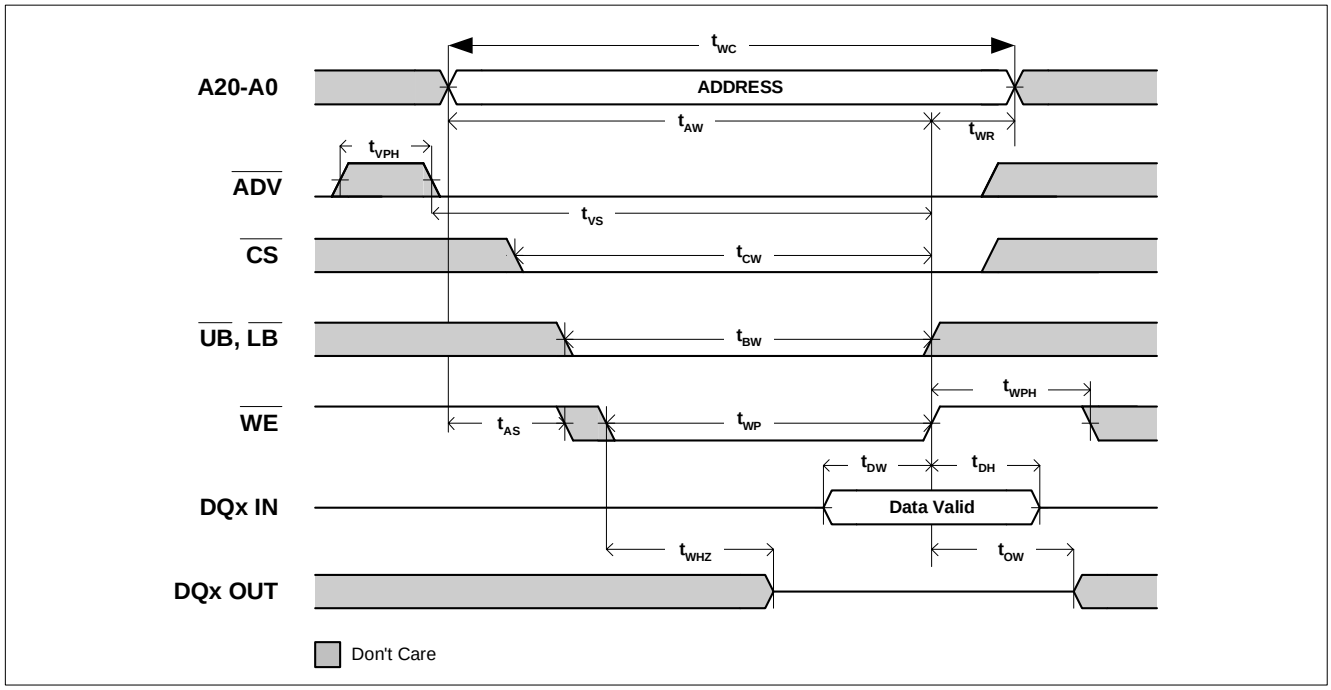


Figure 16 Asynchronous Write - $\overline{WE}$ Controlled ($\overline{OE}$ = V_{IH} or V_{IL}, CRE = V_{IL})

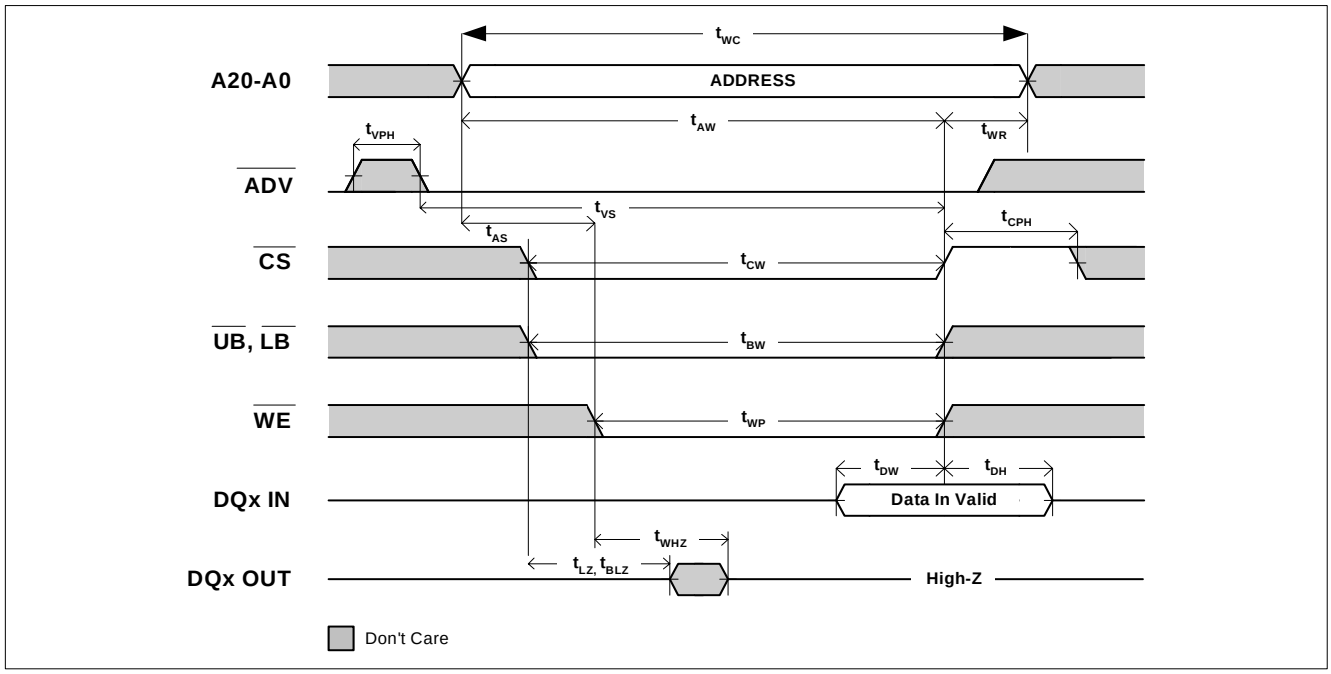


Figure 17 Asynchronous Write - $\overline{CS}$ Controlled ($\overline{OE}$ = V_{IH} or V_{IL}, CRE = V_{IL})

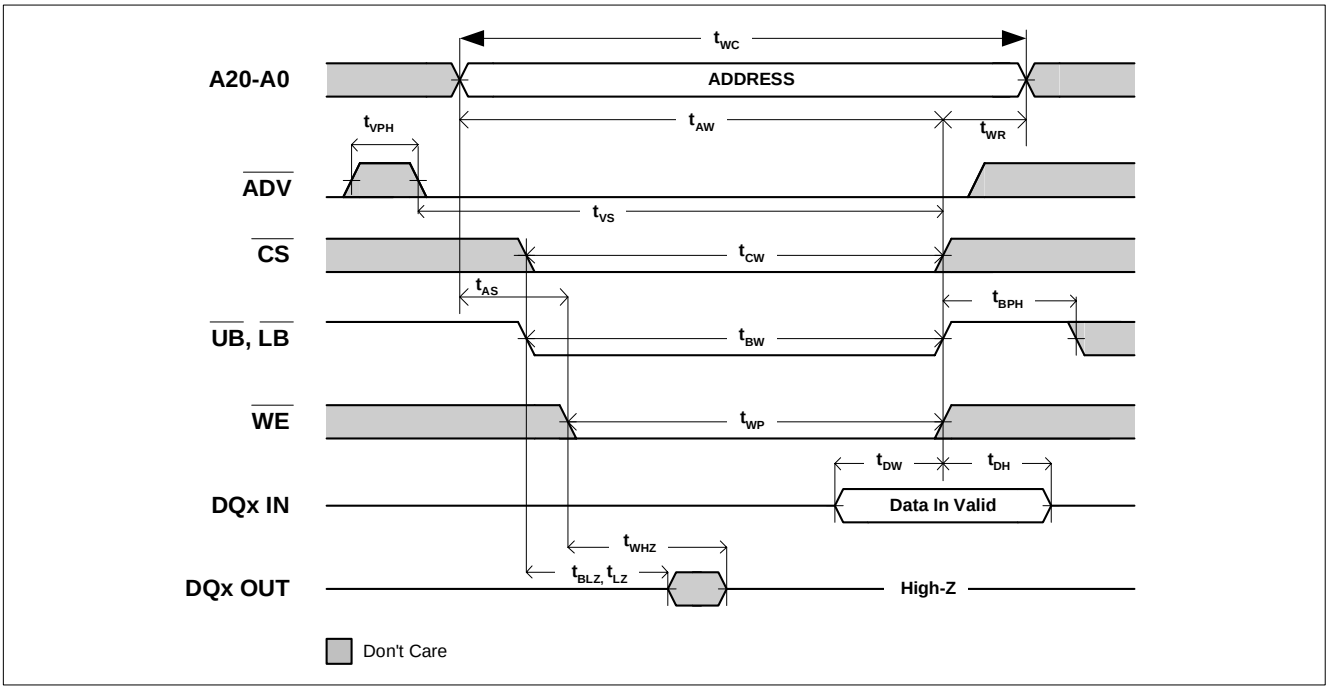


Figure 18 Asynchronous Write - $\overline{UB}$, $\overline{LB}$ Controlled ($\overline{OE}$ = V_{IH} or V_{IL}, CRE = V_{IL})

The programming of control register in SRAM-type mode is performed in the similar manner as asynchronous write except CRE being held high during the operation. Note that CRE has to meet set-up (t_{CRES}) and hold time (t_{CREH}) of valid state (= High) in reference to $\overline{WE}$ falling and rising edge, respectively. $\overline{ADV}$ may be kept low for entire operation. $\overline{CS}$ should toggle at the end of the operation to get ready for following access.

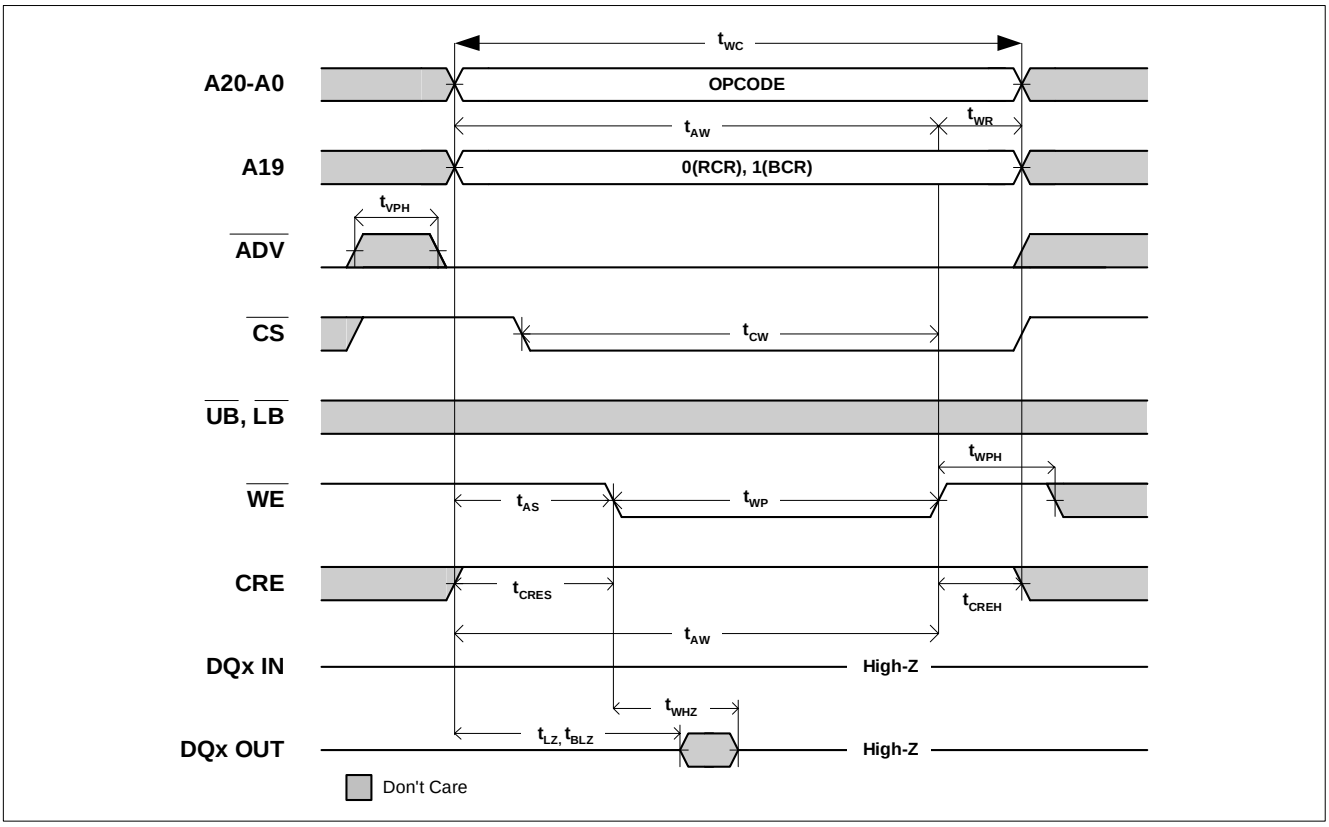


Figure 19 Asynchronous Write to Control Register ($\overline{OE}$ = V_{IH} or V_{IL})

Table 14 Timing Parameters - Asynchronous Write

Parameter	Symbol	9.6, 12.5		15		Unit	Notes
		Min.	Max.	Min.	Max.		
Write cycle time	t_{WC}	70	–	85	–	ns	–
Address (incl. CRE) set-up time	t_{AS}	0	–	0	–	ns	–
Address valid to end of write	t_{AW}	70	–	85	–	ns	–
Write recovery time	t_{WR}	0	–	0	–	ns	–
Chip select pulse width low time	t_{CSL}	–	10	–	10	µs	–
Chip select to end of write	t_{CW}	70	–	85	–	ns	–
ADV high time	t_{VPH}	5	–	7	–	ns	–
ADV setup to end of write	t_{VS}	70	–	85	–	ns	–
Byte control valid to end of write	t_{BW}	70	–	85	–	ns	–
Write pulse width	t_{WP}	40	–	45	–	ns	–
Write pulse pause	t_{WPH}	10	–	15	–	ns	–
$\overline{CS}$ high time when toggling	t_{CPH}	10	–	15	–	ns	–
$\overline{UB}$, $\overline{LB}$ high time when toggling	t_{BPH}	10	–	15	–	ns	–
Write to output disable	t_{WHZ}	–	8	–	10	ns	–
End of write to output enable ($\overline{OE}$ = low)	t_{OW}	3	–	3	–	ns	–
Write data setup time	t_{DW}	20	–	20	–	ns	–
Write data hold time	t_{DH}	0	–	0	–	ns	–
CRE setup time (to $\overline{WE}$ = $\overline{CE}$ = low)	t_{CRES}	5	–	5	–	ns	–
CRE hold time (from $\overline{WE}$ high)	t_{CREH}	0	–	0	–	ns	–

2.7 NOR-Flash-Type Mode

In NOR-Flash mode the CellularRAM applies the NOR-Flash protocol to perform read and write accesses to the memory. Read accesses can be executed in synchronous burst mode, while write accesses are executed in asynchronous mode using $\overline{ADV}$ as address latch strobe signal.

2.7.1 Synchronous Read Mode

[Disclaimer]

WAIT signal of all synchronous timings below is shown in the case of WC=0 (at delay) and WP=0 (active low) though it is not default state.

In synchronous read mode all operations are referred to the rising or falling clock signal edge. Refresh cycles or page boundary crossings are indicated by the WAIT output signal which stalls the processor for this period.

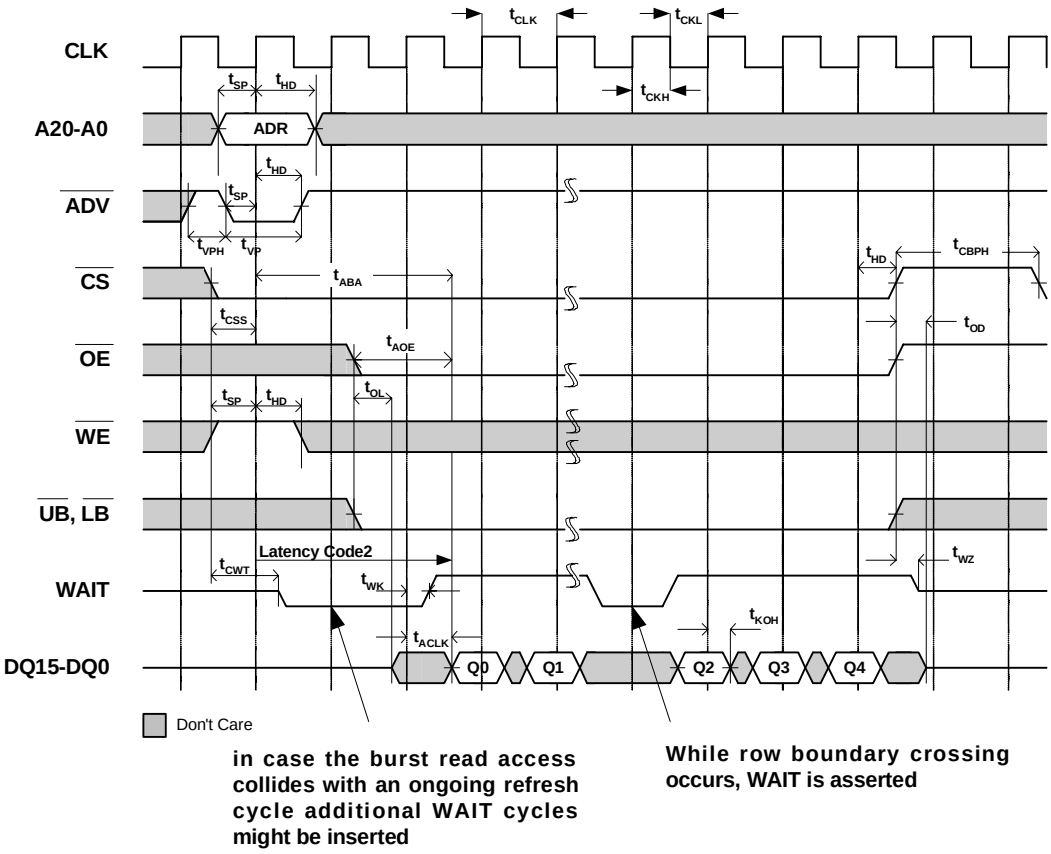


Figure 20 Synchronous Read Burst

2.7.2 Burst Suspend

While in synchronous burst operation, the bus interface may need to be assigned to other memory transaction sharing the same bus. Burst suspend mode is used to fulfill this operation. Keeping $\overline{CS}$ low (WAIT stays asserted indicating valid data output on DQ pins, though they are tri-stated), burst suspend can be initiated with halted CLK. CLK can stay at either high or low state.

As specified, duration of keeping $\overline{CS}$ low can not exceed t_{CSL} maximum, which is 10 µs, so that internal refresh operation is able to run properly. In this event of exceeding t_{CSL} maximum, termination of burst by bringing $\overline{CS}$ to high is strongly recommended instead of using burst suspend mode, then reissuing of the discontinued burst command is required.

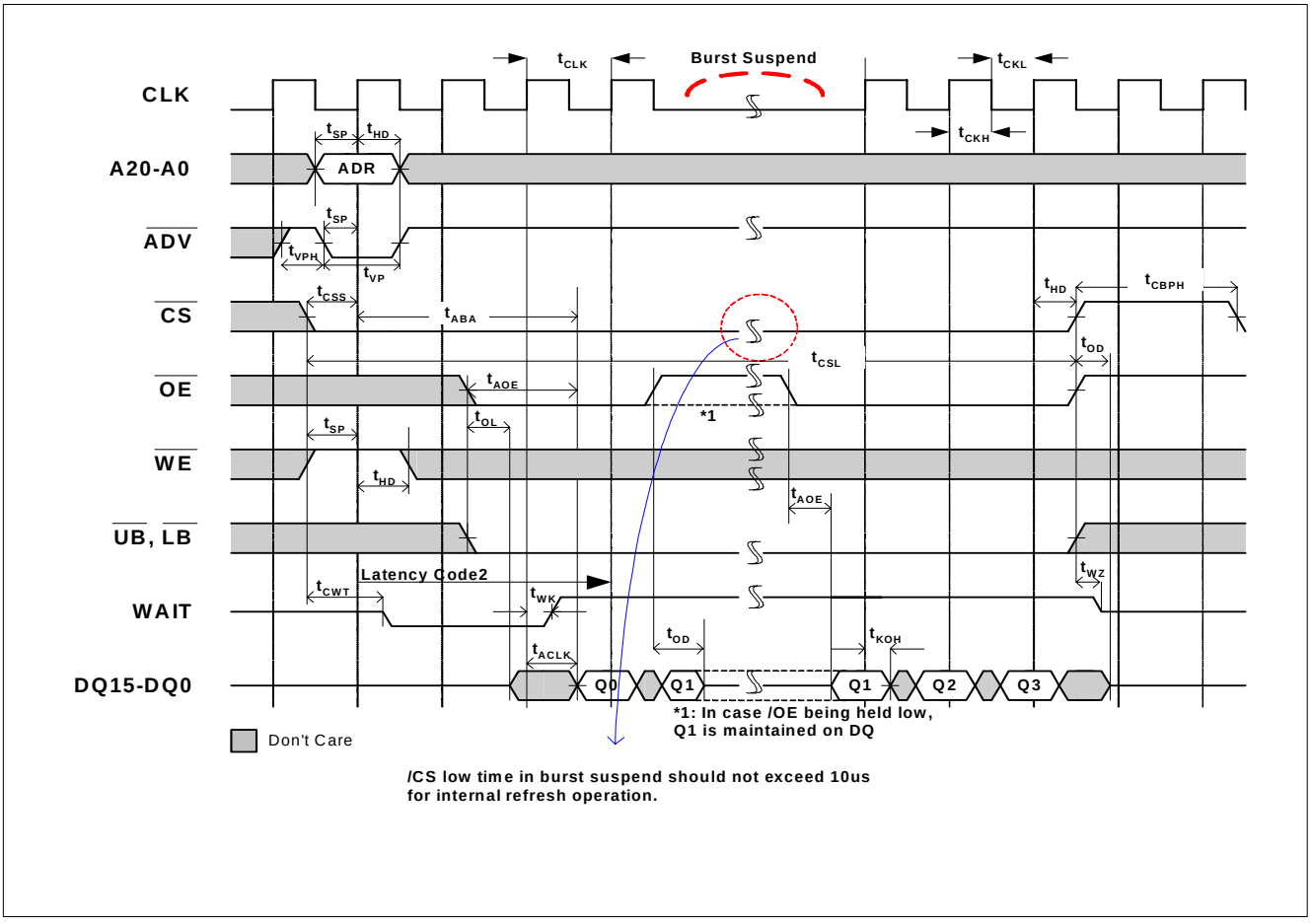


Figure 21 Burst Suspend

Table 15 Timing Parameters - Synchronous Read Burst

Parameter		Symbol	9.6		12.5		15		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
Clock period frequency	Lat = 3	f_{CLK3}	–	104	–	80	–	66	MHz	–
	Lat = 2	f_{CLK2}	–	66	–	50	–	40	MHz	–
Clock period	Lat = 3	t_{CLK3}	9.6	–	12.5	–	15	–	ns	–
	Lat = 2	t_{CLK2}	15	–	20	–	25	–	ns	–
Clock high time		t_{CKH}	3	–	3.5	–	4	–	ns	–
Clock low time		t_{CKL}	3	–	3.5	–	4	–	ns	–
Clock rise/fall time		t_T	–	1.8	–	2	–	2	ns	–
Input setup time to CLK (except $\overline{CS}$)		t_{SP}	3	–	3.5	–	4	–	ns	–
Input hold time from CLK		t_{HD}	1.5	–	2	–	2	–	ns	–
$\overline{ADV}$ pulse width high		t_{VPH}	5	–	5	–	7	–	ns	1)
$\overline{ADV}$ pulse width low		t_{VP}	4	–	4	–	6	–	ns	–
Burst read 1st access delay from CLK		t_{ABA}	–	35	–	46.5	–	54	ns	2)
$\overline{CS}$ low setup to CLK		t_{CSS}	3.5	20	4	20	4	20	ns	3)
Chip select pulse width low time		t_{CSL}	–	10	–	10	–	10	µs	–
$\overline{CS}$ pulse width high		t_{CBPH}	5	–	6	–	8	–	ns	–
$\overline{OE}$ or $\overline{LB}$/$\overline{UB}$ low to output low-Z		t_{OL}	3	–	3	–	3	–	ns	–
$\overline{CS}$, $\overline{OE}$, or $\overline{LB}$/$\overline{UB}$ high to output high-Z		t_{OD}	0	6	0	8	0	8	ns	–
$\overline{OE}$ low to output delay		t_{AOE}	–	20	–	20	–	25	ns	–
$\overline{CS}$ low to WAIT valid		t_{CWT}	–	7	–	9	–	11	ns	–
$\overline{CS}$ high to WAIT high-Z		t_{WZ}	0	7	0	8	0	8	ns	–
CLK to WAIT valid		t_{WK}	–	7	–	9	–	11	ns	–
CLK to output delay		t_{ACLK}	–	7	–	9	–	11	ns	–
Output hold from CLK		t_{KOH}	2	–	2	–	3	–	ns	–

1) $\overline{ADV}$ low for new burst command can not be issued while the previous burst is in burst_init cycle (within latency).

2) In case of refresh collision to the first access, more WAIT cycles will be added.

3) For proper synchronous burst operation, t_{CSSmax} should be met. Otherwise, it is strongly recommended to use CellularRAM in asynchronous mode of operation, instead.

2.7.3 Asynchronous Write with Address Latch ($\overline{ADV}$) Control

In asynchronous write mode, the synchronous clock is switched off and CLK has to be held low. The access protocol is shown with $\overline{ADV}$-latching scheme and it can be applied to write operation in SRAM-type mode.

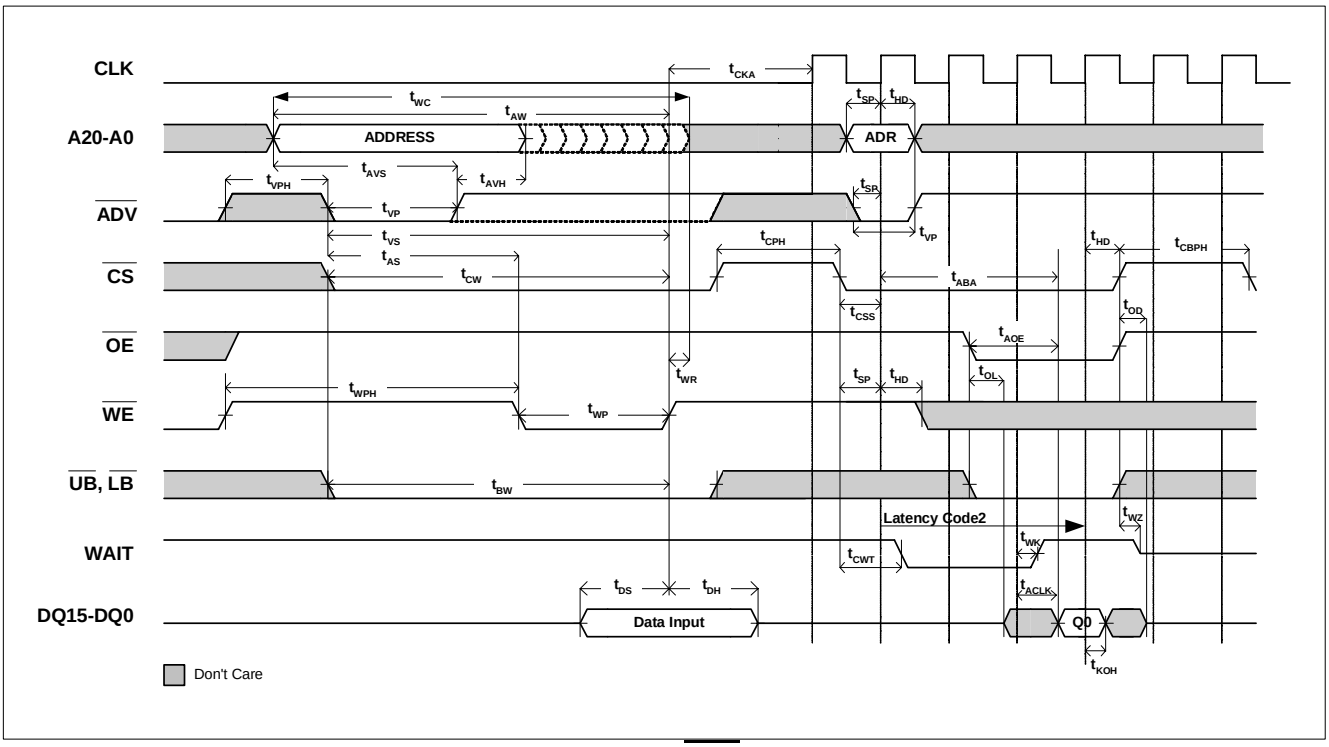


Figure 22 Asynchronous Write with Address Latch ($\overline{ADV}$) Control (followed by single-burst read)

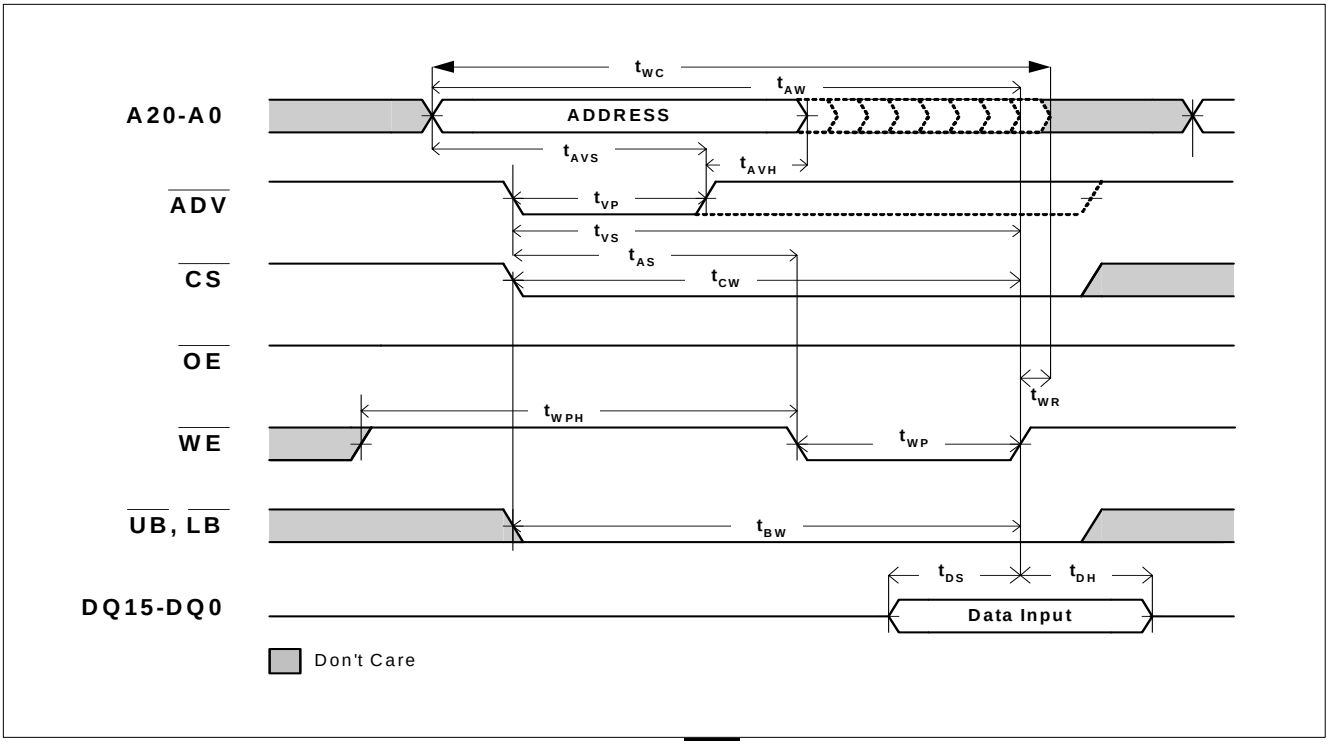


Figure 23 Asynchronous Write with Address Latch ($\overline{ADV}$) Control

The programming of control register in NOR-Flash-type mode is performed in the similar manner as asynchronous write with $\overline{ADV}$ control except CRE being held high during the code input operation. Note that CRE has to meet set-up (t_{CRS}) and hold time (t_{CRH}) of valid state (= High) in reference to $\overline{ADV}$ rising edge. $\overline{ADV}$ may be kept low for entire operation or go high to latch valid control register information at its rising edge.

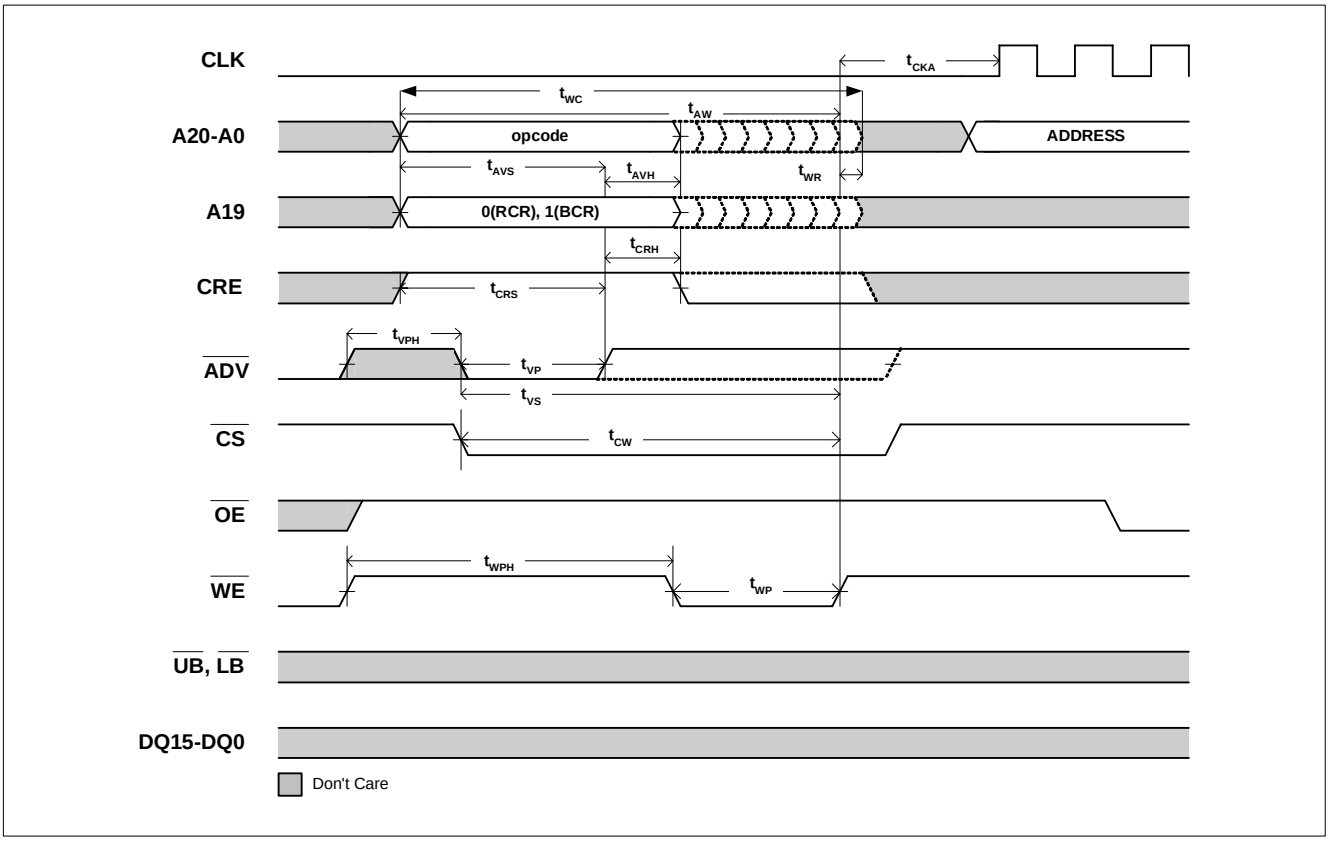


Figure 24 Asynchronous Write To Control Register in NOR-Flash Mode

Table 16 Timing Parameters - Asynchronous Write With $\overline{ADV}$ Control

Parameter	Symbol	9.6, 12.5		15		Unit	Notes
		Min.	Max.	Min.	Max.		
$\overline{WE}$ high to CLK valid	t_{CKA}	25	–	35	–	ns	–
Write cycle time	t_{WC}	70	–	85	–	ns	–
Address setup time to write start	t_{AS}	0	–	0	–	ns	–
Address setup to $\overline{ADV}$ high	t_{AVS}	10	–	10	–	ns	–
Address hold from $\overline{ADV}$ high	t_{AVH}	5	–	5	–	ns	–
Address to end of write	t_{AW}	70	–	85	–	ns	–
$\overline{ADV}$ pulse width high	t_{VPH}	8	–	10	–	ns	–
$\overline{ADV}$ pulse width low	t_{VP}	8	–	10	–	ns	–
$\overline{ADV}$ setup to end of write	t_{VS}	70	–	85	–	ns	–
$\overline{CS}$ to end of write	t_{CW}	70	–	85	–	ns	–
$\overline{UB}$/$\overline{LB}$ to end of write	t_{BW}	70	–	85	–	ns	–
Write pulse width low	t_{WP}	40	–	45	–	ns	–
Write pulse width high	t_{WPH}	10	–	15	–	ns	–
$\overline{CS}$ high time (synch_read)	t_{CBPH}	5	–	8	–	ns	–

Table 16 Timing Parameters - Asynchronous Write With $\overline{\text{ADV}}$ Control (cont'd)

Parameter	Symbol	9.6, 12.5		15		Unit	Notes
		Min.	Max.	Min.	Max.		
$\overline{\text{CS}}$ high time (asynch_write, mixed)	t_{CPH}	10	–	15	–	ns	–
Write recovery time	t_{WR}	0	–	0	–	ns	1
Data setup to $\overline{\text{WE}}$ high	t_{DS}	20	–	20	–	ns	–
Data hold from $\overline{\text{WE}}$ high	t_{DH}	0	–	0	–	ns	–
CRE setup to $\overline{\text{ADV}}$ high	t_{CRS}	10	–	10	–	ns	–
CRE hold from $\overline{\text{ADV}}$ high	t_{CRH}	5	–	5	–	ns	–

Note: 1. t_{WR} is valid only when $\overline{ADV}$ latch of address does not take place until the end of write.

2.8 Synchronous Mode

[Disclaimer]

WAIT signal of all synchronous timings below is shown in the case of WC=0 (at delay) and WP=0 (active low) though it is not default state.

In synchronous mode, read and write operations are synchronized to the clock. Refresh cycles or page boundary crossings are indicated to the host system by asserting the WAIT signal which in turn stalls the processor. WAIT polarity, WAIT timing, synchronicity to the falling/rising clock edge, the burst length and further options are user configurable and can be programmed via the bus configuration register (BCR).

2.8.1 Synchronous Read Mode Including Burst Suspend

Refer to **Section 2.7.1** and **Section 2.7.2**. All the timing and parameters are same as described in read operation for NOR-Flash-Type mode.

2.8.2 Synchronous Write Mode

In synchronous write mode, $\overline{UB}$ and $\overline{LB}$ are used as byte control of data input mask. At the rising edge of CLK, their state is sampled and determined whether the coupled byte (DQ15-8 for $\overline{UB}$ and DQ7-0 for $\overline{LB}$) is updated by input data. Proper set-up time and hold time to CLK should be met. As discussed in **Section 2.4**, synchronous burst write is always configured as continuous and no wrap, so that it has to be terminated by $\overline{CS}$ high state after the burst fulfills required length of cycles.

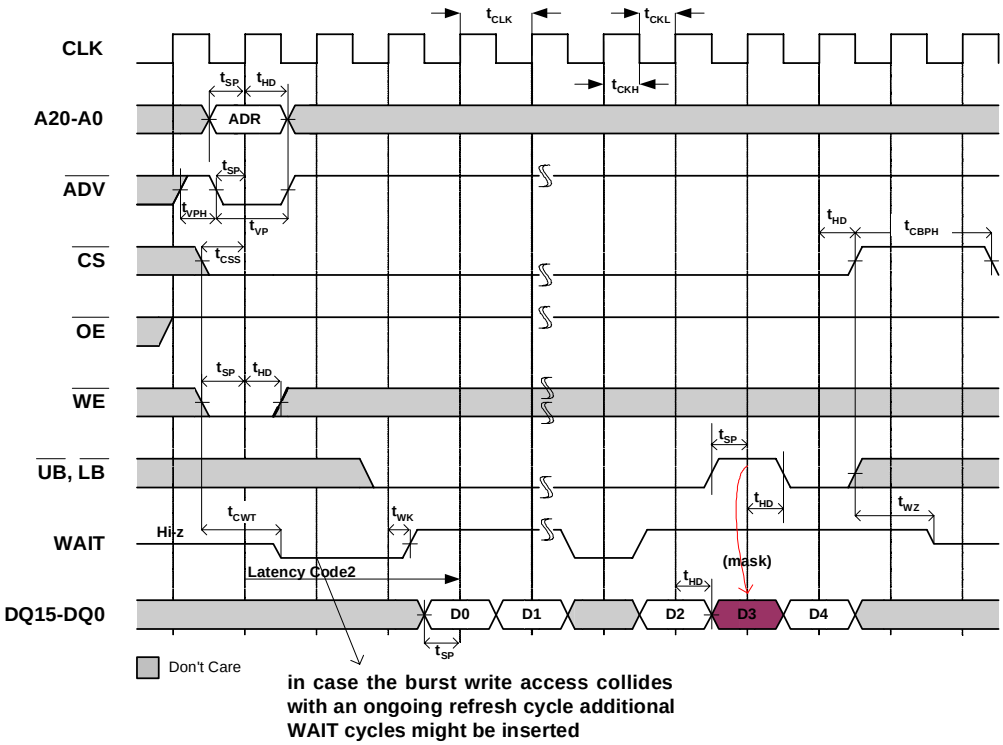


Figure 25 Synchronous Write Burst

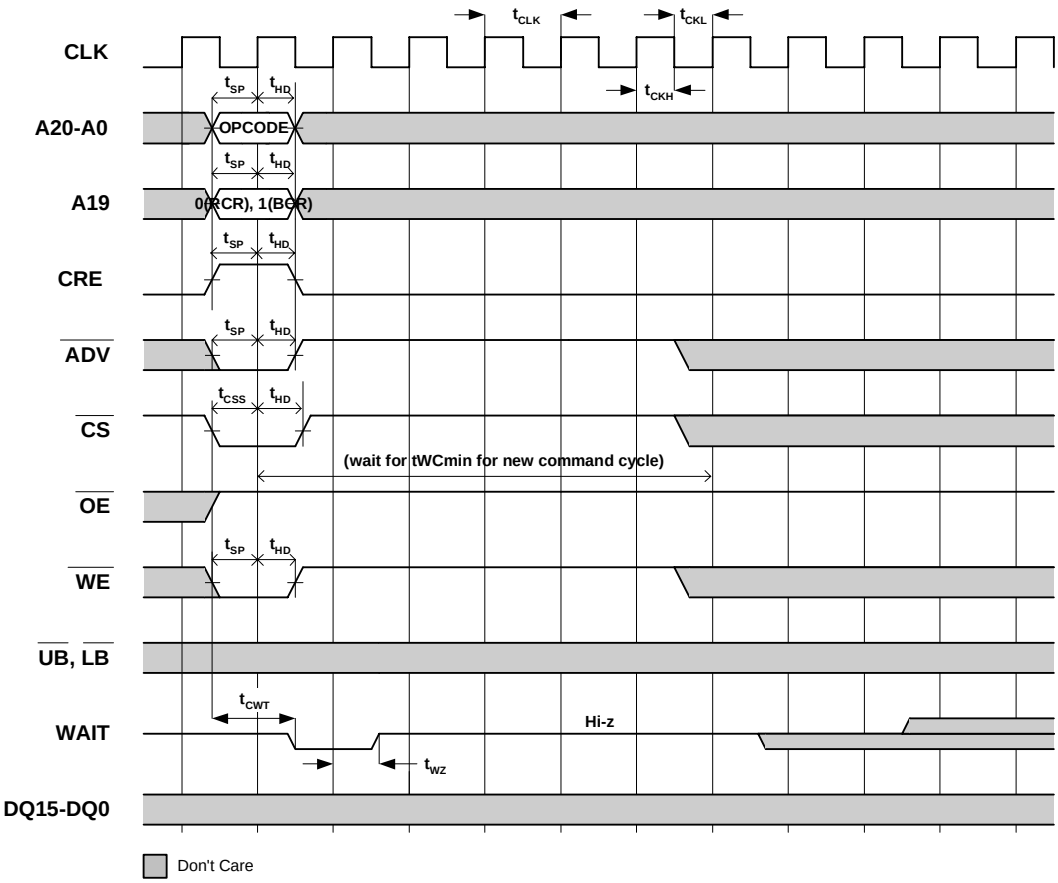


Figure 26 Synchronous Write to Control Register

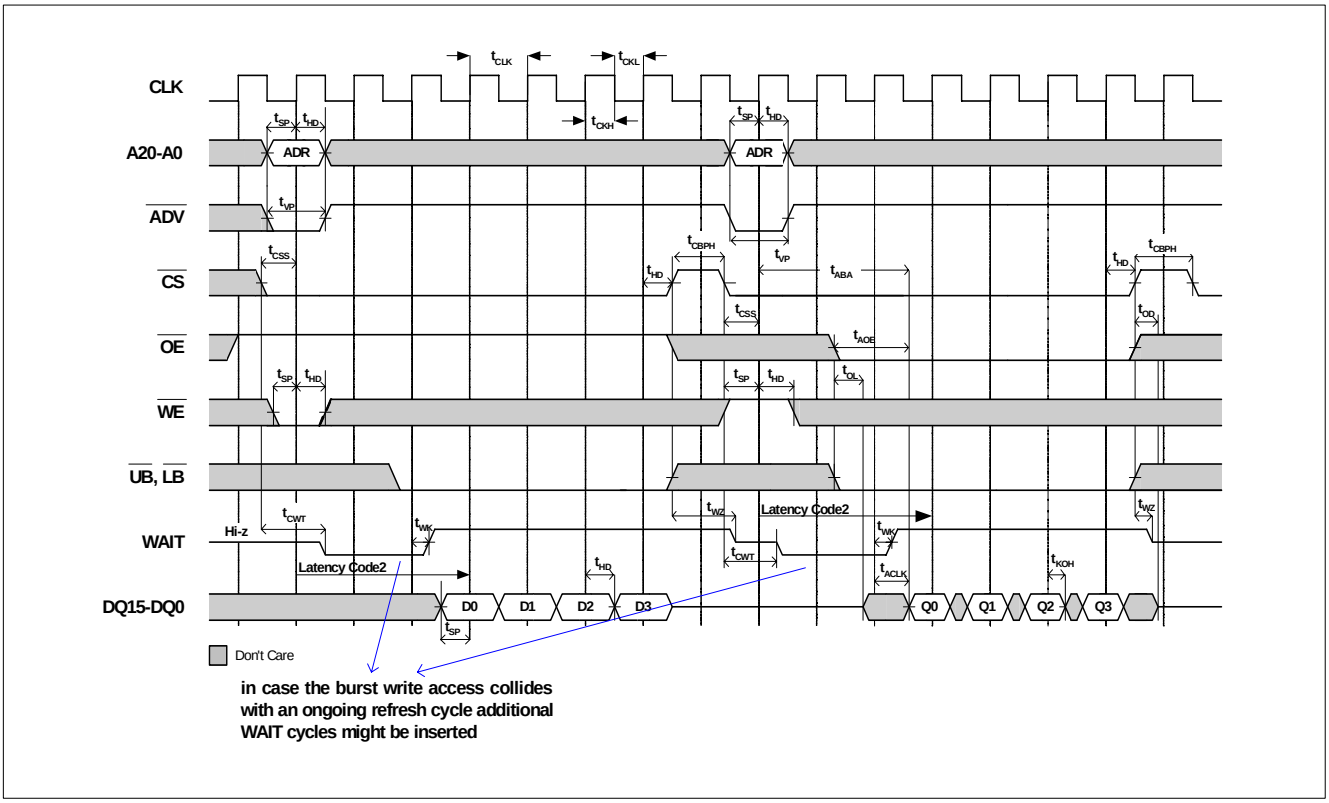


Figure 27 Synchronous Write Burst Followed by Synchronous Read Burst

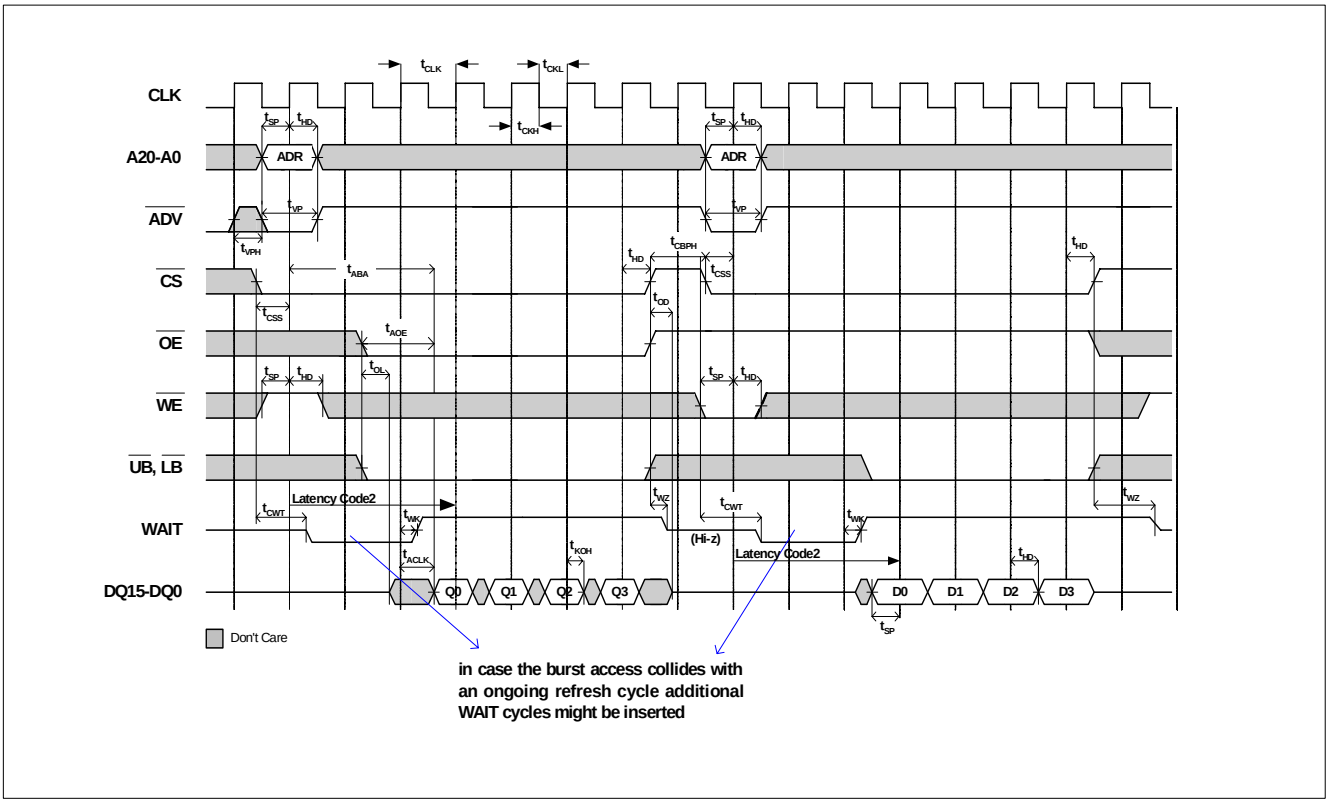


Figure 28 Synchronous Read Burst Followed by Synchronous Write Burst

Table 17 Timing Parameters - Synchronous Read/Write Burst

Parameter		Symbol	9.6		12.5		15		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
Clock period frequency	Lat = 3	f_{CLK3}	–	104	–	80	–	66	MHz	–
	Lat = 2	f_{CLK2}	–	66	–	50	–	40	MHz	–
Clock period	Lat = 3	t_{CLK3}	9.6	–	12.5	–	15	–	ns	–
	Lat = 2	t_{CLK2}	15	–	20	–	25	–	ns	–
Clock high time		t_{CKH}	3	–	3.5	–	4	–	ns	–
Clock low time		t_{CKL}	3	–	3.5	–	4	–	ns	–
Clock rise/fall time		t_T	–	1.8	–	2	–	2	ns	–
Input setup time to CLK (except $\overline{CS}$)		t_{SP}	3	–	3.5	–	4	–	ns	–
Input hold time from CLK		t_{HD}	1.5	–	2	–	2	–	ns	–
$\overline{ADV}$ pulse width high		t_{VPH}	5	–	5	–	7	–	ns	1)
$\overline{ADV}$ pulse width low		t_{VP}	4	–	4	–	6	–	ns	–
Burst read 1st access delay from CLK		t_{ABA}	–	35	–	46.5	–	54	ns	2)
$\overline{CS}$ low setup to CLK		t_{CSS}	3.5	20	4	20	4	20	ns	3)
Chip select pulse width low time		t_{CSL}	–	10	–	10	–	10	µs	–
$\overline{CS}$ pulse width high		t_{CBPH}	5	–	6	–	8	–	ns	–
$\overline{OE}$ or $\overline{LB}$/$\overline{UB}$ low to output low-Z		t_{OL}	3	–	3	–	3	–	ns	–
$\overline{CS}$, $\overline{OE}$, or $\overline{LB}$/$\overline{UB}$ high to output high-Z		t_{OD}	0	6	0	8	0	8	ns	–
$\overline{OE}$ low to output delay		t_{AOE}	–	20	–	20	–	25	ns	–
$\overline{CS}$ low to WAIT valid		t_{CWT}	–	7	–	9	–	11	ns	–
$\overline{CS}$ high to WAIT high-Z		t_{WZ}	0	7	0	8	0	8	ns	–
CLK to WAIT valid		t_{WK}	–	7	–	9	–	11	ns	–
CLK to output delay		t_{ACLK}	–	7	–	9	–	11	ns	–
Output hold from CLK		t_{KOH}	2	–	2	–	3	–	ns	–

1) $\overline{ADV}$ low for new burst command can not be issued while the previous burst is in burst_init cycle (within latency).

2) In case of refresh collision to the first access, more WAIT cycles will be added.

3) For proper synchronous burst operation, t_{CSSmax} should be met. Otherwise, it is strongly recommended to use CellularRAM in asynchronous mode of operation, instead.

2.9 General AC Input/Output Reference Waveform

The input timings refer to a midlevel of $V_{DDQ}/2$ while as output timings refer to midlevel $V_{DDQ}/2$. The rising and falling edges are 10 - 90% and < 2 ns.

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 18 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Operating temperature range	T_C	-25	+85	°C	–
Storage temperature range	T_{STG}	-55	+150	°C	–
Soldering peak temperature (10 s)	T_{Sold}	–	260	°C	–
Voltage of V_{DD} supply relative to V_{SS}	V_{DD}	-0.3	+2.45	V	–
Voltage of V_{DDQ} supply relative to V_{SS}	V_{DDQ}	-0.3	+3.6	V	–
Voltage of any input relative to V_{SS}	V_{IN}	-0.3	+3.6	V	–
Power dissipation	P_D	–	180	mW	–
Short circuit output current	I_{OUT}	-50	+50	mA	–

Attention: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

3.2 Recommended Power & DC Operation Ratings

All values are recommended operating conditions unless otherwise noted.

Table 19 Recommended DC Operating Conditions

Parameter	Symbol	Limit Values			Unit	Notes
		Min.	Typ.	Max.		
Power supply voltage, core	V_{DD}	1.7	1.8	1.95	V	–
Power supply voltage, 1.8 V I/Os	V_{DDQ}	1.7	1.8	2.25	V	–
Input high voltage	V_{IH}	V_{DDQ} – 0.4	–	V_{DDQ} + 0.2	V	–
Input low voltage	V_{IL}	-0.2	–	0.4	V	–

Table 20 DC Characteristics

Parameter	Symbol	Limit Values			Unit	Notes
		Min.	Typ.	Max.		
Output high voltage (I_{OH} = -0.2 mA)	V_{OH}	$V_{DDQ} \times 0.8$	–	–	V	–
Output low voltage (I_{OL} = 0.2 mA)	V_{OL}	–	–	$V_{DDQ} \times 0.2$	V	–
Input leakage current	I_{LI}	–	–	1	µA	–
Output leakage current	I_{LO}	–	–	1	µA	–

Table 21 Operating Characteristics

Parameter	Symbol	9.6		12.5		15		Unit	Test Condition	Notes
		Min.	Max.	Min.	Max.	Min.	Max.			
Operating Current								mA	$V_{in} = V_{DD}$ or V_{SS}, Chip enabled, $I_{out} = 0$	1)
• Async read/write random @t_{RCmin}	I_{DD1}	–	20	–	20	–	17			
• Async read/write random @t_{RC}=1µs	I_{DD1L}	–	5	–	5	–	5			
• Async Page read	I_{DD1P}	–	15	–	15	–	12			
• Sync burst (continuous)	I_{DD4}	–	20	–	18	–	15			
• Burst Initial access	I_{DD5}	–	35	–	35	–	30			
Stand-By Current : L-part	I_{DD2}	–	90	–	90	–	90	µA	$V_{in} = V_{DD}$ or V_{SS},Chip deselected, (Full array)	–
Stand-By Current : Standard		–	120	–	120	–	120	µA		–
Deep Power Down Current	I_{DD3}	–	25	–	25	–	25	µA	$V_{in} = V_{DD}$ or V_{SS}	–

1) The specification assumes the output disabled.

3.3 Output Test Conditions

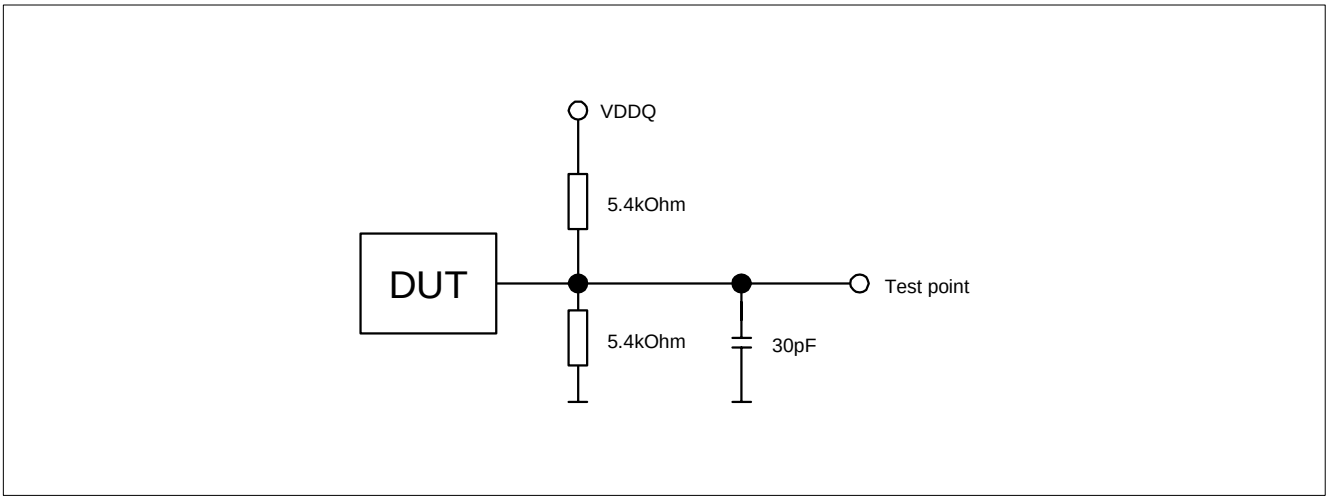


Figure 29 Output Test Circuit

Please refer to section **Section 2.9**.

3.4 Pin Capacitances

Table 22 Pin Capacitances

Pin	Limit Values		Unit	Condition
	Min.	Max.		
A20 - A0, $\overline{CS}$, $\overline{OE}$, $\overline{WE}$, $\overline{UB}$, $\overline{LB}$, CRE, $\overline{ADV}$	–	5.0	pF	T_A = +25 °C, freq. = 1 MHz, V_{pin} = 0 V, (sampled, not 100% tested)
CLK	–	5.0	pF	
DQ15 - DQ0	–	6.0	pF	
WAIT	–	6.0	pF	

4 Package Outlines

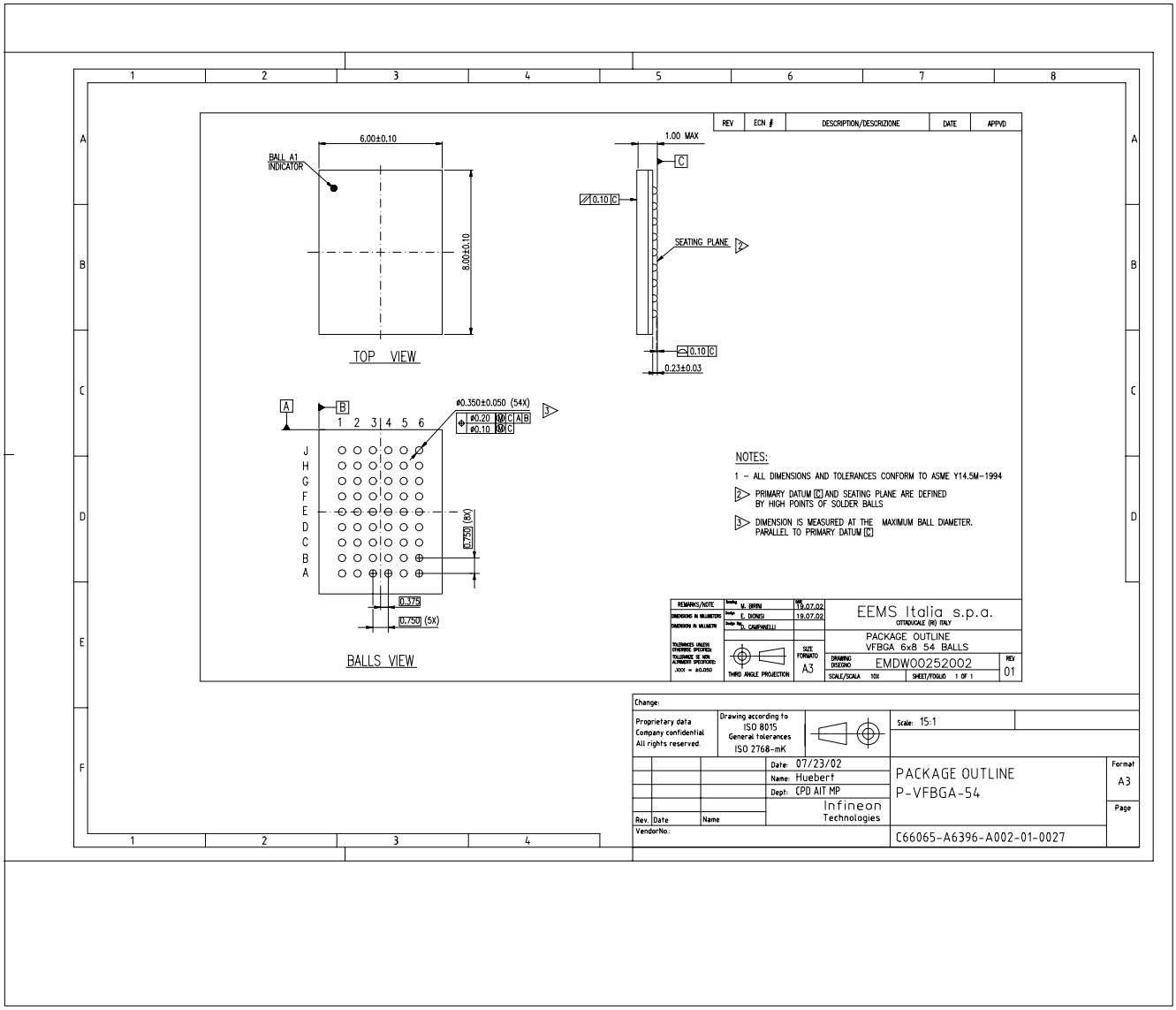


Figure 30 P-VFBGA-54 (Plastic Very Thin Fine Pitch Ball Grid Array Package)

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.

SMD = Surface Mounted Device

Dimensions in mm

5 Appendix A: Low-Frequency Mode

5.1 Asynchronous Access

Depending on the random access frequency two cases are distinguished:

High Frequency Mode (≥ 100 kHz):

There are no t_{RC} max. time nor $\overline{CS}$/$\overline{OE}$ max. low time restrictions during subsequent random read or write accesses.

Low Frequency Mode (< 100 kHz):

There are no t_{RC} max. time nor $\overline{CS}$/$\overline{OE}$ max. low time restrictions if all control signals ($\overline{CS}$, $\overline{OE}$, $\overline{WE}$, $\overline{UB}$/$\overline{LB}$) follow the modified timing as shown below, see attached timing diagram and timing table. There is no extra mode register setting necessary.

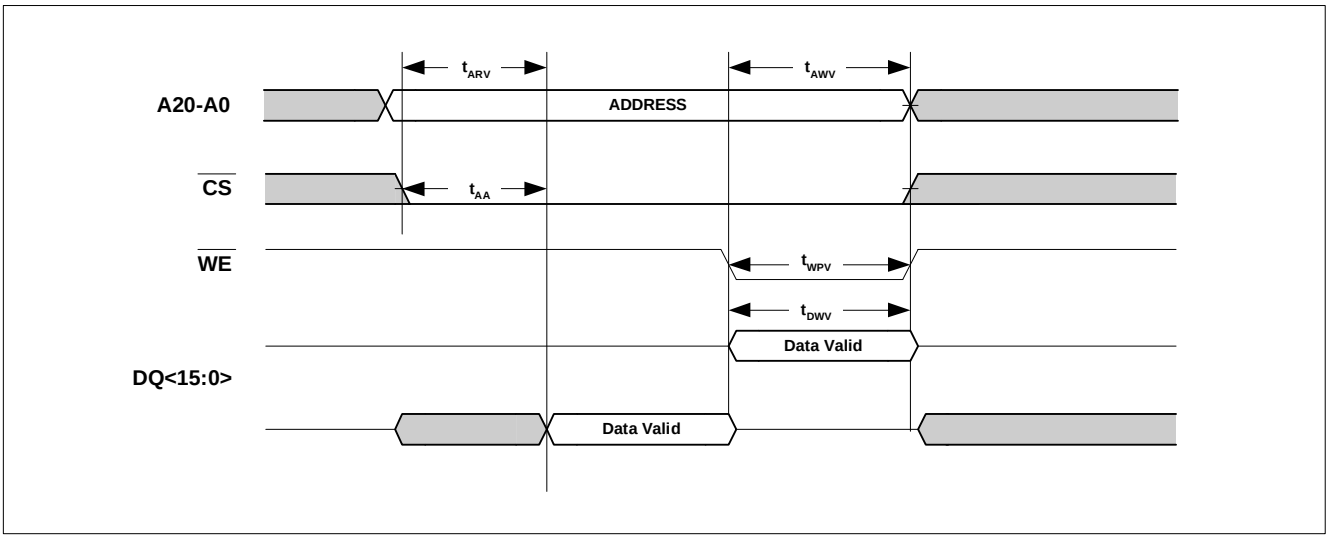


Figure 31 Low-Frequency Mode

Parameter	Symbol	9.6, 12.5		15		Unit	Notes
		Min.	Max.	Min.	Max.		
Address stable time for read access	t_{ARV}	70	–	85	–	ns	–
Address stable overlap with write pulse	t_{AWV}	70	–	85	–	ns	–
Write pulse width	t_{WPV}	70	–	85	–	ns	–
Data to write time overlap	t_{DWV}	70	–	85	–	ns	–

6 Appendix B: S/W Register Entry Mode (“4-cycle method”)

Other than CRE-controlled SCR operation, CellularRAM supports software (S/W) method as an alternative to access the control registers. Since S/W register entry mode consists of 4 consecutive access cycles to top memory location (all addresses are “1”), it is often referred as “4-cycle method”. 4-cycles starts from 2 back-to-back read cycles (initializing command identification) followed by one write cycle (command identification completed and which control register is accessed is known), then final write cycle for configuring the selected control register by the given input or read cycle to check the content of the register through DQ pins. It does function the configuration of control register bits like the way with dedicated pin, CRE method, but there are a few differences from CRE-controlled method as follow;

- Register read mode (checking content) is supported with S/W register entry as well as register write (program).
- The mode bits for control register are supplied through DQ <15:0> instead of address pins in CRE-controlled. Though each register has 21-bits (A<20:0>) for 32M CellularRAM, only low 16-bit registers becomes valid during S/W method.
- Only asynchronous read and write is allowed for consecutive 4 access cycles to top address. No synchronous timing is supported. If this entry mode is used in synchronous mode, then clock should stop running and stay at low level.
- Instead of A19 bit state, the selection of which control register, BCR or RCR, is done with the state of DQ<15:0> given at 3rd cycle. (“00h” for RCR, “01h” for BCR)
- Since S/W register entry asks for 4 complete access cycles in a row and the device is designed operating with internally regulated supply which is going to be discharged in deep power-down (DPD) mode, **DPD function is not supported** with this programming method.
- The method is realized by the device exactly when 2 consecutive read cycles to top memory location is followed by write cycle to the same location, so that any exceptional cycle combination - not only access mode, but also the number of cycles - will fail in invoking the register entry mode properly.

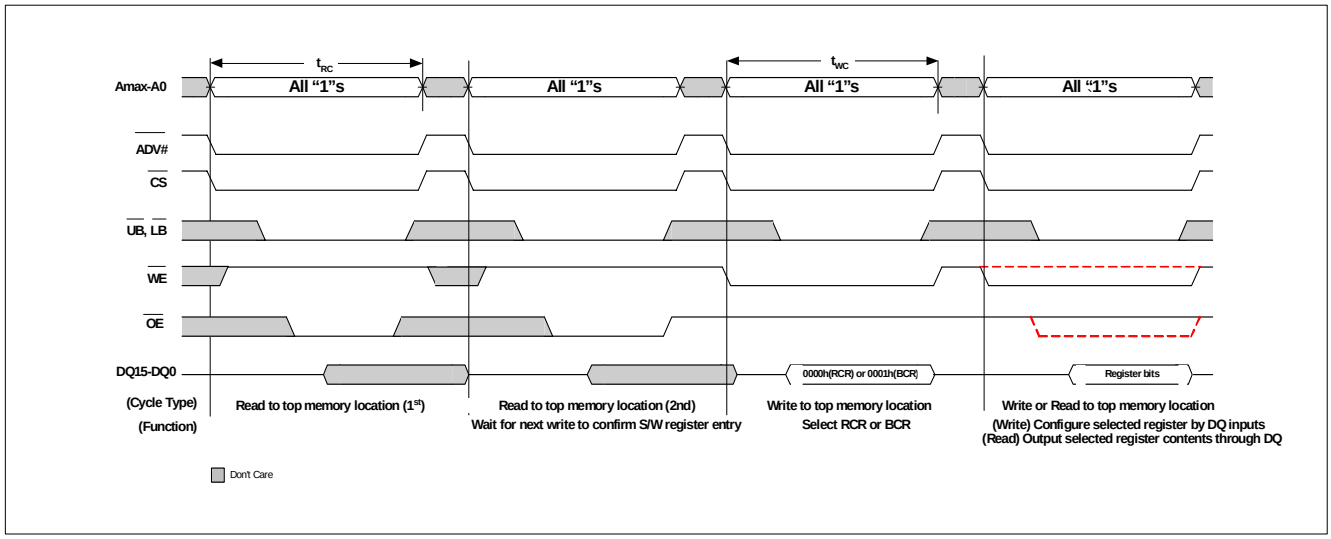


Figure 32 S/W Register Entry timing (Address input = 1FFFFFh)

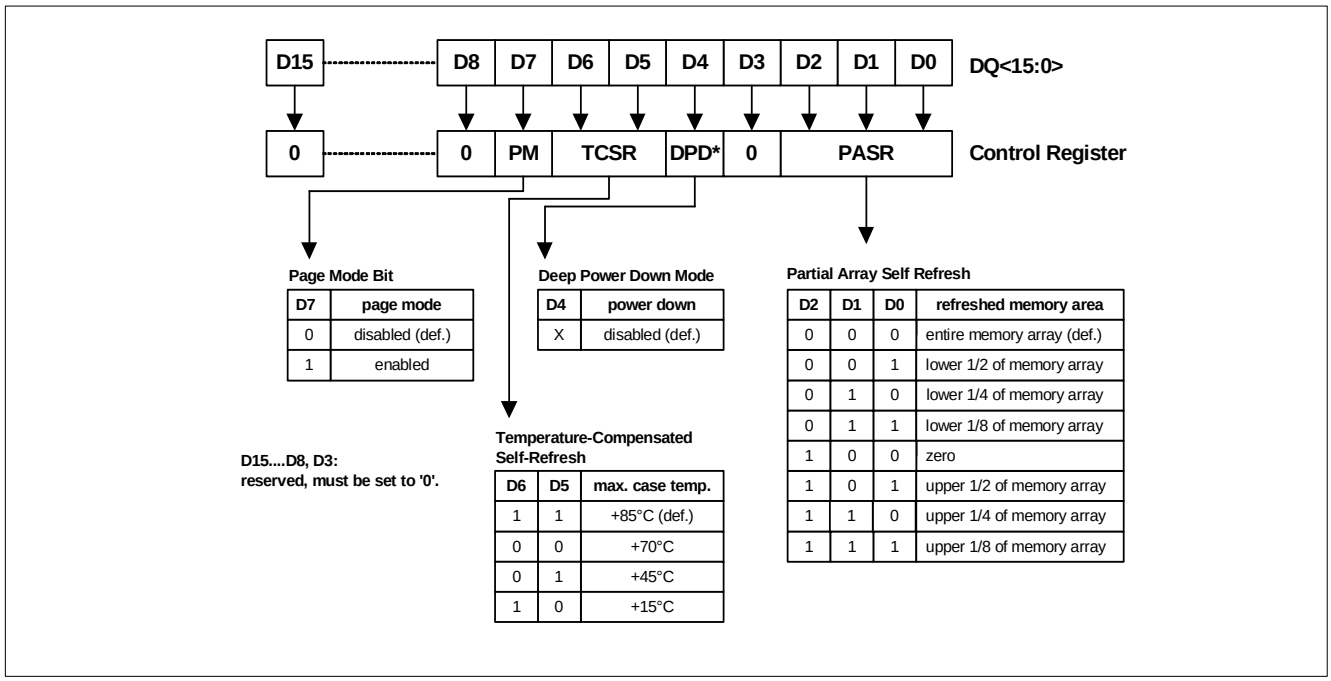


Figure 33 RCR Mapping in S/W Register Entry

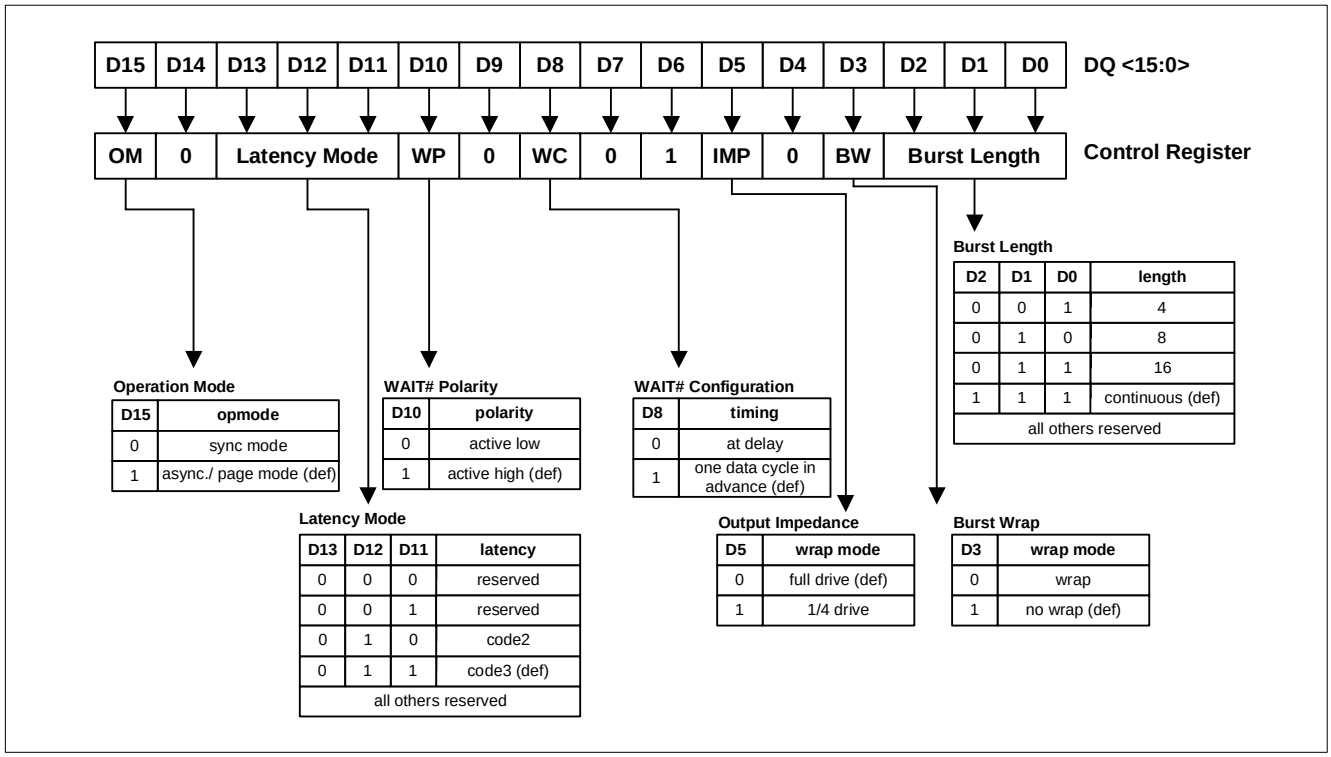


Figure 34 BCR Mapping in S/W Register Entry

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