

CYPRESS
SEMICONDUCTOR

T-46-23-10

CY7C161A
CY7C162A16,384 x 4 Static R/W RAM
Separate I/O**Features**

- Automatic power-down when deselected
- Transparent write (7C161A)
- CMOS for optimum speed/power
- High speed
— 12 ns t_{AA}
- Low active power
— 935 mW
- Low standby power
— 220 mW
- TTL-compatible inputs and outputs

- Capable of withstanding greater than 2001V electrostatic discharge.

Functional Description

The CY7C161A and CY7C162A are high-performance CMOS static RAMs organized as 16,384 by 4 bits with separate I/O. Easy memory expansion is provided by active LOW chip enables ($\overline{CE}_1$, $\overline{CE}_2$) and three-state drivers. They have an automatic-power-down feature, reducing the power consumption by 60% when deselected.

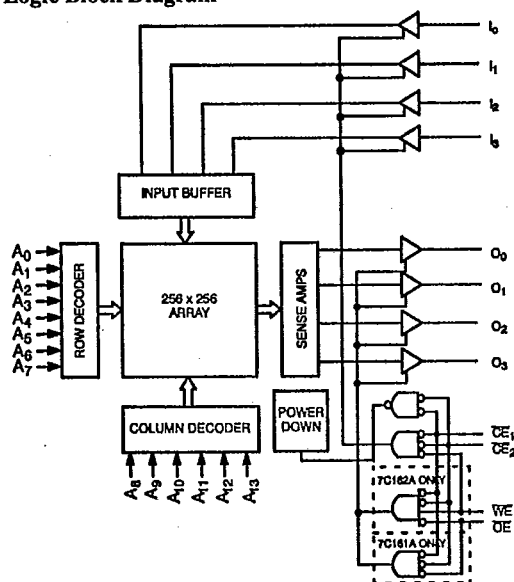
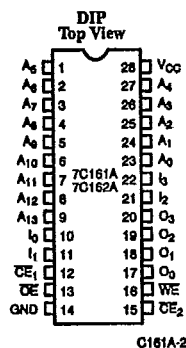
Writing to the device is accomplished when the chip enable ($\overline{CE}_1$, $\overline{CE}_2$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four input pins (I_0 through I_3)

is written into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking the chip enables ($\overline{CE}_1$, $\overline{CE}_2$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data output pins.

The output pins stay in high-impedance state when write enable ($\overline{WE}$) is LOW (7C162A only), or one of the chip enables ($\overline{CE}_1$, $\overline{CE}_2$) are HIGH.

A die coat is used to insure alpha immunity.

Logic Block Diagram**Pin Configurations**



T-46-23-10

CY7C161A

CY7C162A

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	– 65°C to +150°C
Ambient Temperature with Power Applied	– 55°C to +125°C
Supply Voltage to Ground Potential (Pin 24 to Pin 12)	– 0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	– 0.5V to +7.0V
DC Input Voltage	– 3.0V to +7.0V

Output Current into Outputs (Low)	20 mA
Static Discharge Voltage (per MIL-STD-883, Method 3015)	>2001V
Latch-Up Current	>200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Military ^[2]	– 55°C to +125°C	5V ± 10%



SRAMS

Electrical Characteristics Over the Operating Range^[3]

Parameters	Description	Test Conditions	7C161A–12 7C162A–12		7C161A–15 7C162A–15		7C161A–20 7C162A–20		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = – 4.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage ^[4]		– 0.5	0.8	– 0.5	0.8	– 3.0	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	– 10	+10	– 10	+10	– 10	+10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	– 10	+10	– 10	+10	– 10	+10	μA
I _{OS}	Output Short Circuit Current ^[5]	V _{CC} = Max., V _{OUT} = GND		– 350		– 350		– 350	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA		170		160		100	mA
I _{SB1}	Automatic $\overline{CE}$ Power-Down Current	Max. V _{CC} , $\overline{CE} \geq V_{IH}$, Min. Duty Cycle = 100%		40		40		40	mA
I _{SB2}	Automatic $\overline{CE}$ Power-Down Current	Max. V _{CC} , $\overline{CE}_1 \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} – 0.3V or V _{IN} ≤ 0.3V		20		20		20	mA

Shaded area contains advanced information.

Notes:

- T_A is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- V_{IL} min. = – 3.0V for pulse durations less than 30 ns.
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

CYPRESS
SEMICONDUCTOR

T-46-23-10

CY7C161A

CY7C162A

Electrical Characteristics Over the Operating Range^[3] (continued)

Parameters	Description	Test Conditions	7C161A-25 7C162A-25		7C161A-35, 45 7C162A-35, 45		Units
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage ^[4]		-3.0	0.8	-3.0	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-10	+10	-10	+10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	-10	+10	-10	+10	μA
I _{OS}	Output Short Circuit Current ^[5]	V _{CC} = Max, V _{OUT} = GND		-350		-350	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA		100		100	mA
I _{SB1}	Automatic $\overline{CE}$ Power-Down Current	Max. V _{CC} , $\overline{CE} \geq V_{IH}$, Min. Duty Cycle = 100%		40		30	mA
I _{SB2}	Automatic $\overline{CE}$ Power-Down Current	Max. V _{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V		20		20	mA

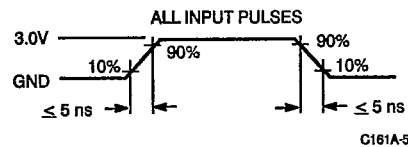
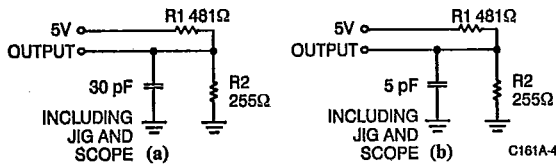
Capacitance^[6]

Parameters	Description	Test Conditions	Max.	Units
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	10	pF
C _{OUT}	Output Capacitance		10	pF

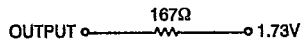
Note:

6. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT





CY7C161A

CY7C162A

T-46-23-10

Switching Characteristics Over the Operating Range^{2, 7, 8]}

Parameters	Description	7C161A-12 7C162A-12		7C161A-15 7C162A-15		7C161A-20 7C162A-20		7C161A-25 7C162A-25		7C161A-35 7C162A-35		7C161A-45 7C162A-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE														
t _{RC}	Read Cycle Time	12		15		20		25		35		45		ns
t _{AA}	Address to Data Valid		12		15		20		25		35		45	ns
t _{OHA}	Output Hold from Address Change	3		3		5		5		5		5		ns
t _{ACE}	CE LOW to Data Valid		12		15		20		25		35		45	ns
t _{DOE}	OE LOW to Data Valid		6		7		10		12		15		20	ns
t _{LZOE}	OE LOW to LOW Z	0		0		3		3		3		3		ns
t _{HZOE}	OE HIGH to HIGH Z		7		8		8		10		12		15	ns
t _{LZCE}	CE LOW to Low Z ^[9]	3		3		5		5		5		5		ns
t _{HZCE}	CE HIGH to High Z ^[9, 10]		7		8		8		10		15		15	ns
t _{PU}	CE LOW to Power-Up	0		0		0		0		0		0		ns
t _{PD}	CE HIGH to Power-Down		12		15		20		20		20		25	ns
WRITE CYCLE ^[11]														
t _{WC}	Write Cycle Time	12		15		20		20		25		40		ns
t _{SCE}	CE LOW to Write End	8		10		15		20		25		30		ns
t _{AW}	Address Set-Up to Write End	9		10		15		20		25		30		ns
t _{HA}	Address Hold from Write End	0		0		0		0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		0		0		0		ns
t _{PWE}	WE Pulse Width	8		10		15		15		20		20		ns
t _{SD}	Data Set-Up to Write End	6		7		10		10		15		15		ns
t _{HD}	Data Hold from Write End	0		0		0		0		0		0		ns
t _{LZWE}	WE HIGH to Low Z ^[9] (7C162A)	3		3		5		5		5		5		ns
t _{HZWE}	WE LOW to High Z ^[9, 10] (7C162A)		6		7		7		7		10		15	ns
t _{AWE}	WE LOW to Data Valid (7C161A)		12		15		20		25		30		35	ns
t _{ADV}	Data Valid to Output Valid (7C161A)		12		15		20		20		30		35	ns
t _{DCE}	CE LOW to Data Valid (7C161A)		12		15		20		25		30		35	ns

Shaded area contains advanced information.

Notes:

- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- Both $\overline{CE}_1$ and $\overline{CE}_2$ are represented by $\overline{CE}$ in the Switching Characteristics and Waveforms sections.
- At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for any given device.

- t_{HZCE} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ± 500 mV from steady state voltage.
- The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, $\overline{CE}_2$ LOW, and WE LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.



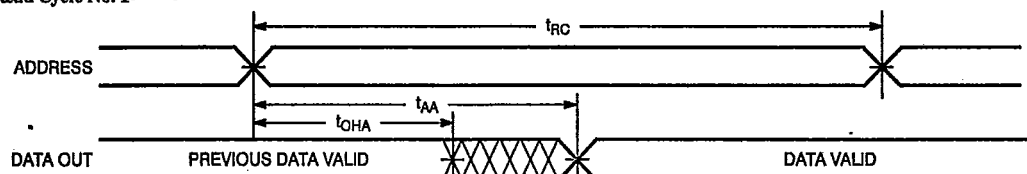
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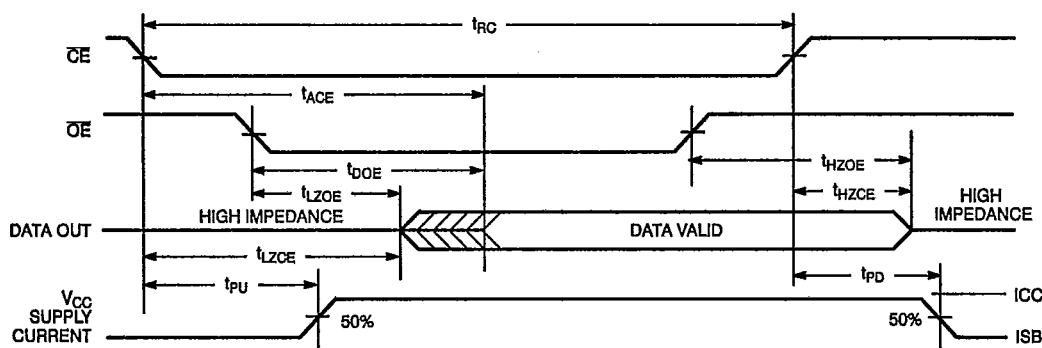
CY7C161A

CY7C162A

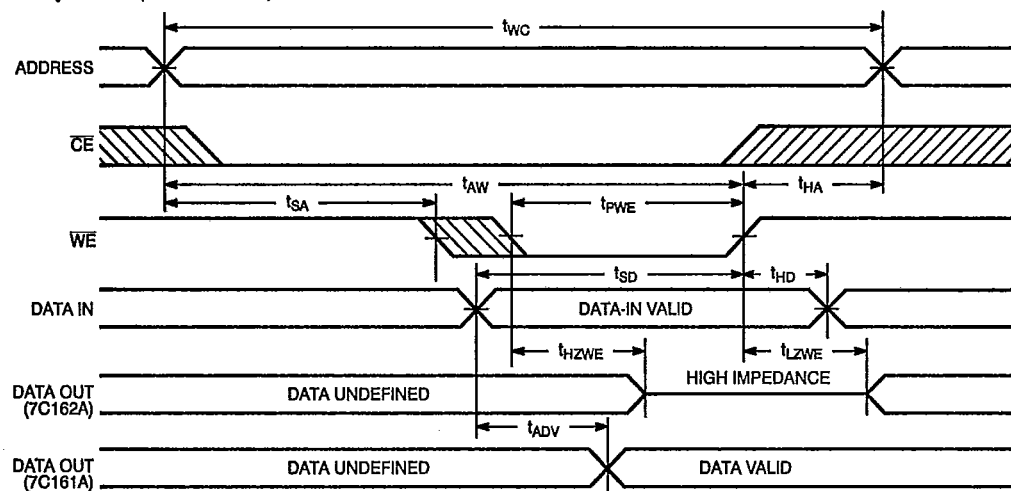
T-46-23-10

Switching Waveforms^[8]Read Cycle No. 1^[12, 13]

C161A-6

Read Cycle No. 2^[12, 14]

C161A-7

Write Cycle No. 1 ($\overline{WE}$ Controlled)^[11]

C161A-8

Notes:

12. $\overline{WE}$ is HIGH for read cycle.13. Device is continuously selected, $\overline{CE}_1, \overline{CE}_2 = V_{IL}$.14. Address valid prior to or coincident with $\overline{CE}_1, \overline{CE}_2$ transition LOW.

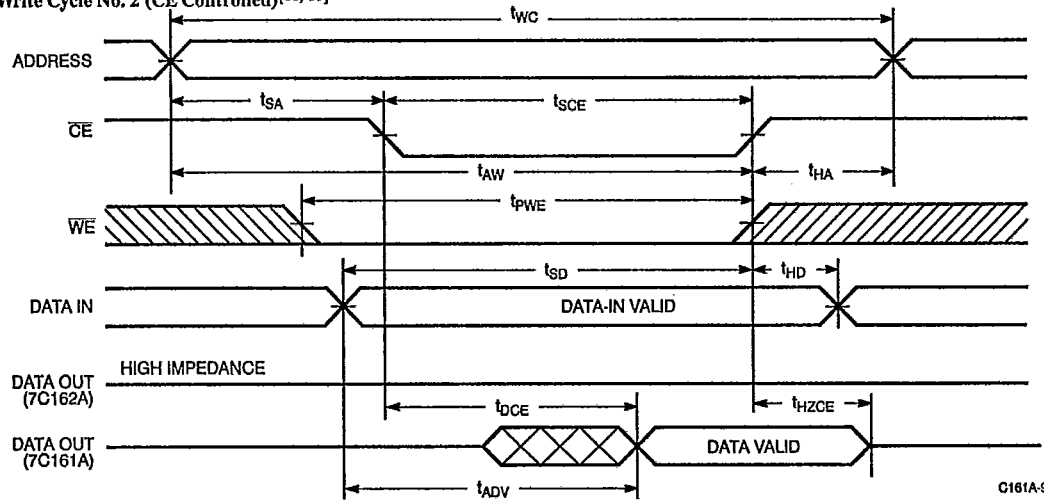


CY7C161A

CY7C162A

T-46-23-10

Switching Waveforms (continued)

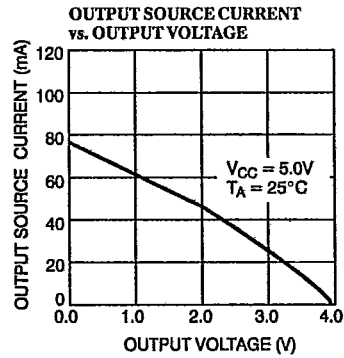
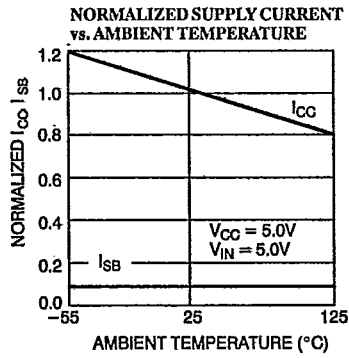
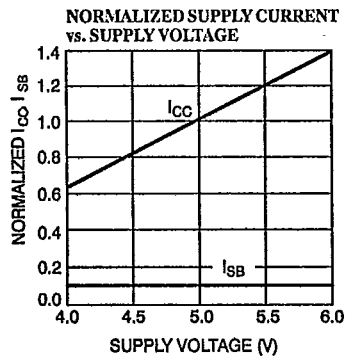
Write Cycle No. 2 ($\overline{\text{CE}}$ Controlled)[11, 15]

SRAMs

Notes:

15. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ HIGH, the output remains in a high-impedance state (7C162A only).

Typical DC and AC Characteristics



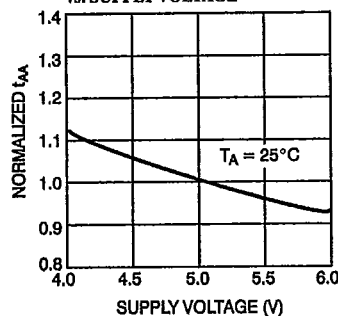
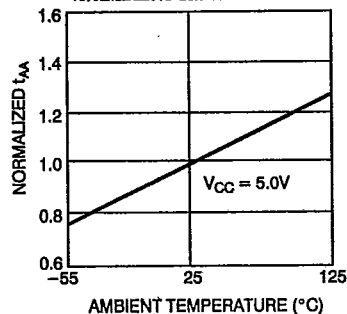
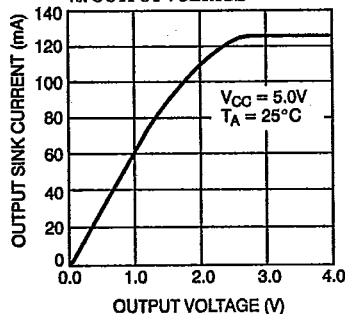
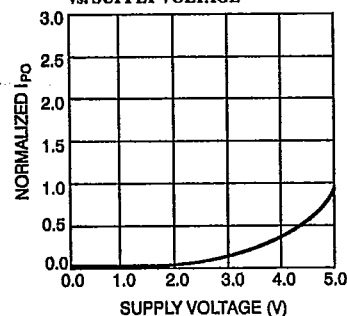
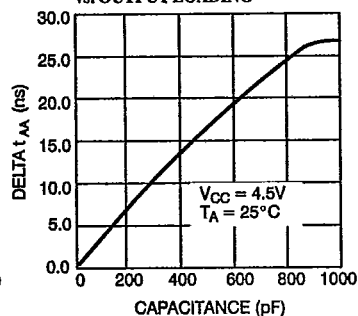
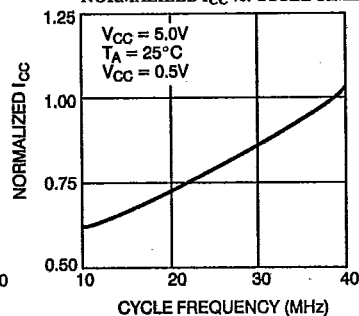


CY7C161A

CY7C162A

Typical DC and AC Characteristics (continued)

T-46-23-10

NORMALIZED ACCESS TIME
vs. SUPPLY VOLTAGENORMALIZED ACCESS TIME
vs. AMBIENT TEMPERATUREOUTPUT SINK CURRENT
vs. OUTPUT VOLTAGETYPICAL POWER-ON CURRENT
vs. SUPPLY VOLTAGETYPICAL ACCESS TIME CHANGE
vs. OUTPUT LOADINGNORMALIZED I_{CC} vs. CYCLE TIME

Address Designators

Address Name	Address Function	Pin Number
A5	X3	1
A6	X4	2
A7	X5	3
A8	X6	4
A9	X7	5
A10	Y0	6
A11	Y1	7
A12	Y5	8
A13	Y4	9
A0	Y3	23
A1	Y2	24
A2	X0	25
A3	X1	26
A4	X2	27



T-46-23-10

CY7C161A
CY7C162A

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
12	CY7C161A-12DMB	D22	Military
	CY7C161A-12LMB	L54	
15	CY7C161A-15DMB	D22	Military
	CY7C161A-15LMB	L54	
20	CY7C161A-20DMB	D22	Military
	CY7C161A-20LMB	L54	
25	CY7C161A-25DMB	D22	Military
	CY7C161A-25LMB	L54	
35	CY7C161A-35DMB	D22	Military
	CY7C161A-35LMB	L54	
45	CY7C161A-45DMB	D22	Military
	CY7C161A-45LMB	L54	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL} Max.	1, 2, 3
I _{IX}	1, 2, 3
I _{OZ}	1, 2, 3
I _{OS}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB1}	1, 2, 3
I _{SB2}	1, 2, 3



SRAMS

Speed (ns)	Ordering Code	Package Type	Operating Range
12	CY7C162A-12DMB	D22	Military
	CY7C162A-12KMB	K74	
	CY7C162A-12LMB	L54	
15	CY7C162A-15DMB	D22	Military
	CY7C162A-15KMB	K74	
	CY7C162A-15LMB	L54	
20	CY7C162A-20DMB	D22	Military
	CY7C162A-20KMB	K74	
	CY7C162A-20LMB	L54	
25	CY7C162A-25DMB	D22	Military
	CY7C162A-25KMB	K74	
	CY7C162A-25LMB	L54	
35	CY7C162A-35DMB	D22	Military
	CY7C162A-35KMB	K74	
	CY7C162A-35LMB	L54	
45	CY7C162A-45DMB	D22	Military
	CY7C162A-45KMB	K74	
	CY7C162A-45LMB	L54	

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t _{RC}	7, 8, 9, 10, 11
t _{AA}	7, 8, 9, 10, 11
t _{OHA}	7, 8, 9, 10, 11
t _{ACE}	7, 8, 9, 10, 11
t _{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t _{WC}	7, 8, 9, 10, 11
t _{SCE}	7, 8, 9, 10, 11
t _{AW}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{SA}	7, 8, 9, 10, 11
t _{PWE}	7, 8, 9, 10, 11
t _{SD}	7, 8, 9, 10, 11
t _{HD}	7, 8, 9, 10, 11
t _{AWE} ^[16]	7, 8, 9, 10, 11
t _{ADV} ^[15]	7, 8, 9, 10, 11

Notes:
16. 7C161A only.

Shaded area contains advanced information.

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