PRELIMINARY **CY7C109A**

128K x 8 Static RAM

Features

- **High speed**
  - **— t_{AA} = 12 ns**
- **CMOS for optimum speed/power**
- **Low active power**
  - **— 1020 mW**
- **Low standby power**
  - **— 250 mW**
- **2.0V data retention (optional)**
  - **— 100 µW**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ options**

Functional Description

The CY7C109A is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}_1$), an active HIGH chip enable (CE_2), an active LOW output enable ($\overline{OE}$), and three-state drivers. This device has an automatic power-down feature that reduces power consumption by more than 75% when deselected.

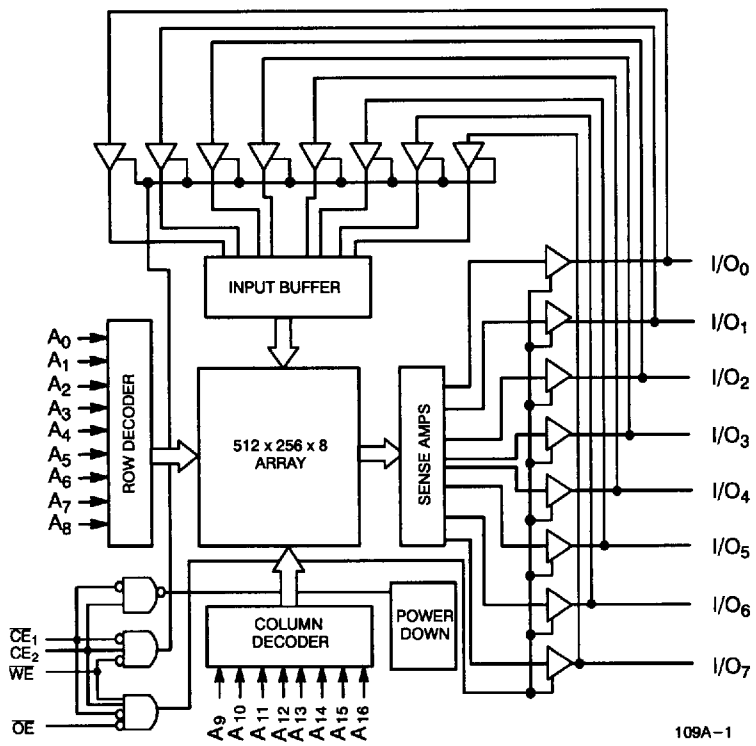
Writing to the device is accomplished by taking chip enable one ($\overline{CE}_1$) and write enable ($\overline{WE}$) inputs LOW and chip enable two (CE_2) input HIGH. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking chip enable one ($\overline{CE}_1$) and output enable ($\overline{OE}$) LOW while forcing write enable ($\overline{WE}$) and chip enable two (CE_2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW).

The CY7C109 is available in standard 400-mil-wide DIPs and SOJs and a leadless chip carrier.

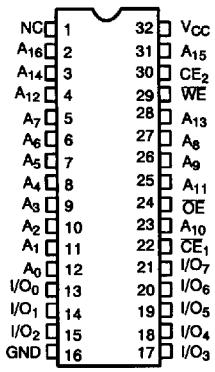
Logic Block Diagram



109A–1

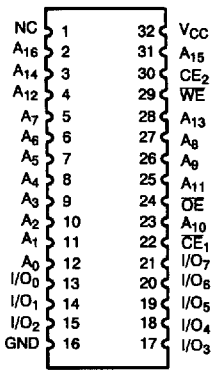
Pin Configurations

DIP/SOJ Top View



109A–2

LCC Top View



109A–3

Selection Guide

		7C109A–12	7C109A–15	7C109A–20	7C109A–25	7C109A–35
Maximum Access Time (ns)		12	15	20	25	35
Maximum Operating Current (mA)	Commercial	185	170	155	145	140
	Military		180	170	160	150
Maximum Standby Current (mA)	Commercial	45	40	30	30	25
	Military		40	30	30	25

Shaded area contains advanced information.

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December 1992 – Revised February 1996

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[1] .. −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... −0.5V to V_{CC} +0.5V

DC Input Voltage[1] ..... −0.5V to V_{CC} +0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	−55°C to +125°C	5V ± 10%

Notes:

1. V_{IL} (min.) = −2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7C109A−12 Min.	7C109A−12 Max.	7C109A−15 Min.	7C109A−15 Max.	7C109A−20 Min.	7C109A−20 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]			−0.3	0.8	−0.3	0.8	−0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−1	+1	−1	+1	−1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	−5	+5	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−300		−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		185		170		155	mA
			Mil				180		170	
I_{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{IH} or CE_2 ≤ V_{IL}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Com'l		45		40		30	mA
			Mil				40		30	
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{CC} − 0.3V, or CE_2 ≤ 0.3V, V_{IN} ≥ V_{CC} − 0.3V, or V_{IN} ≤ 0.3V, f=0	Com'l		10		10		10	mA
			L		2		2		2	
			Mil				10		10	
			L				2		2	

Shaded area contains advanced information.

Electrical Characteristics Over the Operating Range[3] (continued)

Parameter	Description	Test Conditions		7C109A–25 Min.	7C109A–25 Max.	7C109A–35 Min.	7C109A–35 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]			–0.3	0.8	–0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		–1	+1	–1	+1	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		–5	+5	–5	+5	μA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			–300		–300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		145		140	mA
			Mil		160		150	
I_{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{IH} or CE_2 ≤ V_{IL}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Com'l		30		25	mA
			Mil		30		25	
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{CC} – 0.3V, or CE_2 ≤ 0.3V, V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, f=0	Com'l		10		10	mA
			L		2		2	
			Mil		10		10	
			L		2		2	

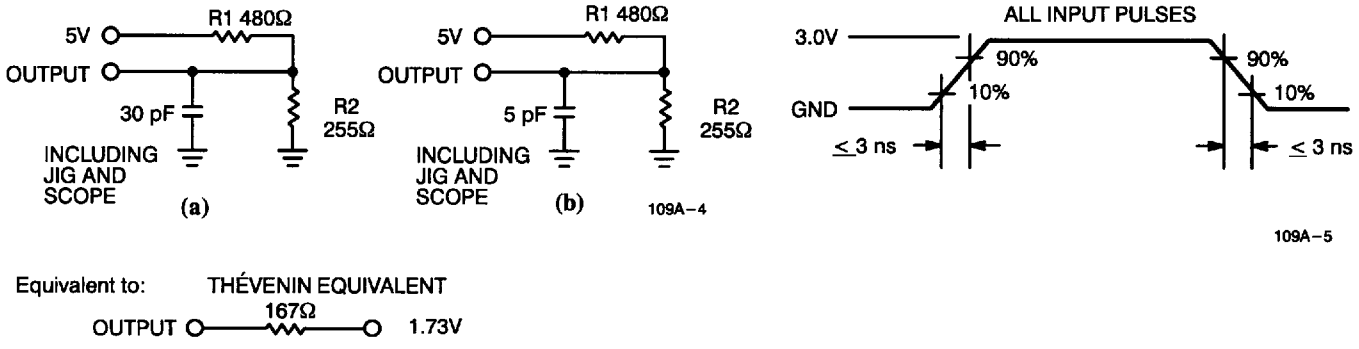
Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}: Addresses	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	7	pF
C_{IN}: Controls			10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

3. See the last page of this specification for Group A subgroup testing information.
4. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT

Switching Characteristics[3, 6] Over the Operating Range

Parameter	Description	7C109A–12		7C109A–15		7C109A–20		7C109A–25		7C109A–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Min.	
READ CYCLE												
t_{RC}	Read Cycle Time	12		15		20		25		35		ns
t_{AA}	Address to Data Valid		12		15		20		25		35	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		3		ns
t_{ACE}	$\overline{CE}_1$ LOW to Data Valid, CE_2 HIGH to Data Valid		12		15		20		25		35	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		6		7		8		10		10	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[7, 8]		6		7		8		10		10	ns
t_{LZCE}	$\overline{CE}_1$ LOW to Low Z, CE_2 HIGH to Low Z[8]	3		3		3		3		3		ns
t_{HZCE}	$\overline{CE}_1$ HIGH to High Z, CE_2 LOW to High Z[7, 8]		6		7		8		10		10	ns
t_{PU}	$\overline{CE}_1$ LOW to Power-Up, CE_2 HIGH to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}_1$ HIGH to Power-Down, CE_2 LOW to Power-Down		12		15		20		25		35	ns
WRITE CYCLE[9, 10]												
t_{WC}	Write Cycle Time	12		15		20		25		35		ns
t_{SCE}	$\overline{CE}_1$ LOW to Write End, CE_2 HIGH to Write End	10		12		15		20		25		ns
t_{AW}	Address Set-Up to Write End	10		12		15		20		25		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		12		15		20		25		ns
t_{SD}	Data Set-Up to Write End	7		8		10		15		20		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[8]	3		3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7, 8]		6		7		8		10		10	ns

Shaded area contains advanced information.

Notes:

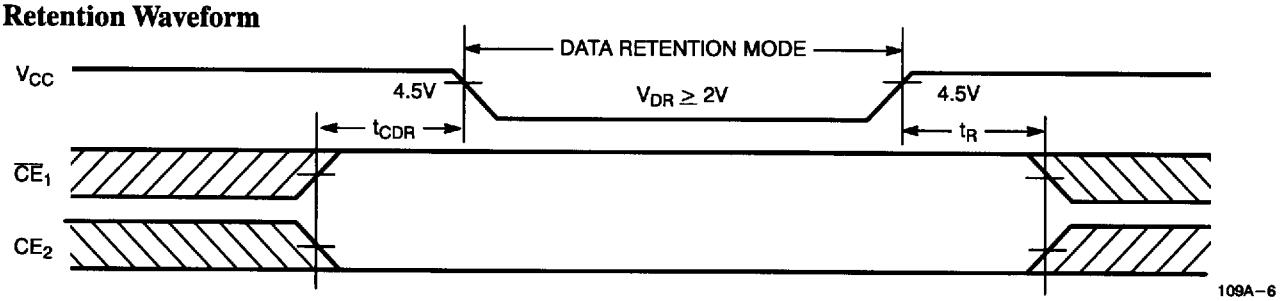
6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW. $\overline{CE}_1$ and $\overline{WE}$ must be LOW and CE_2 HIGH to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
10. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Data Retention Characteristics Over the Operating Range (L Version Only)

Parameter	Description	Conditions[11]	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
V_{DR}	V_{CC} for Retention Data		2.0		2.0		V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$, $\overline{CE_1} \geq V_{CC} - 0.3V$ or $CE_2 \leq 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		50		70	µA
t_{CDR}[5]	Chip Deselect to Data Retention Time		0		0		ns
t_R[5]	Operation Recovery Time		t_{RC}		t_{RC}		ns

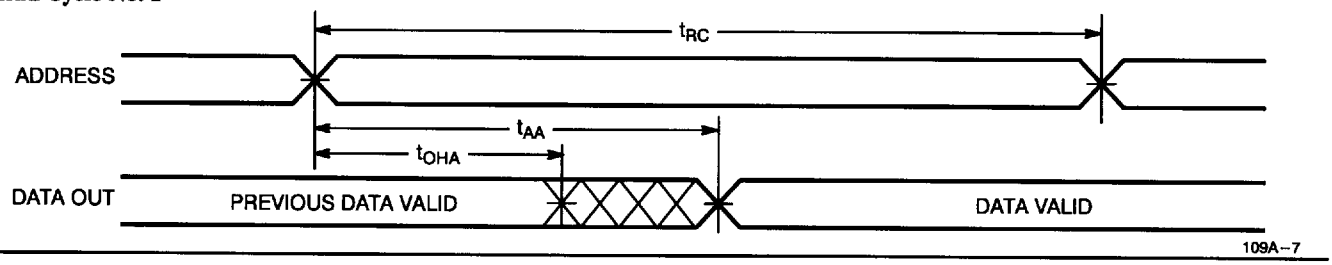
Note:
11. No input may exceed V_{CC} +0.5V.

Data Retention Waveform

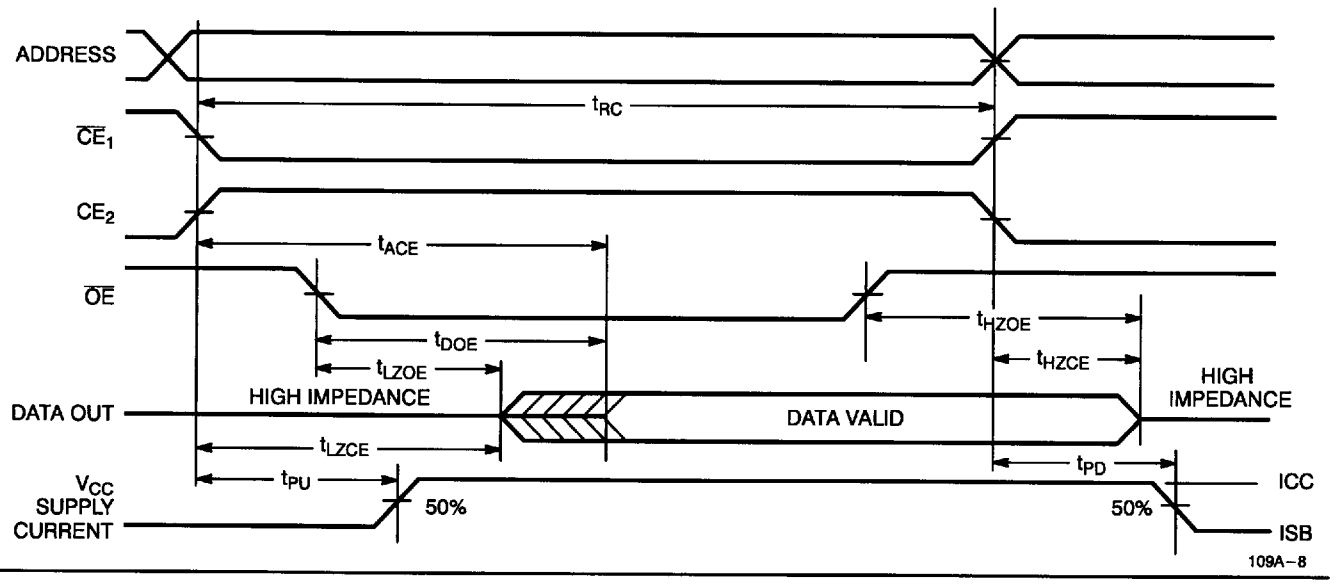


Switching Waveforms

Read Cycle No. 1[12, 13]



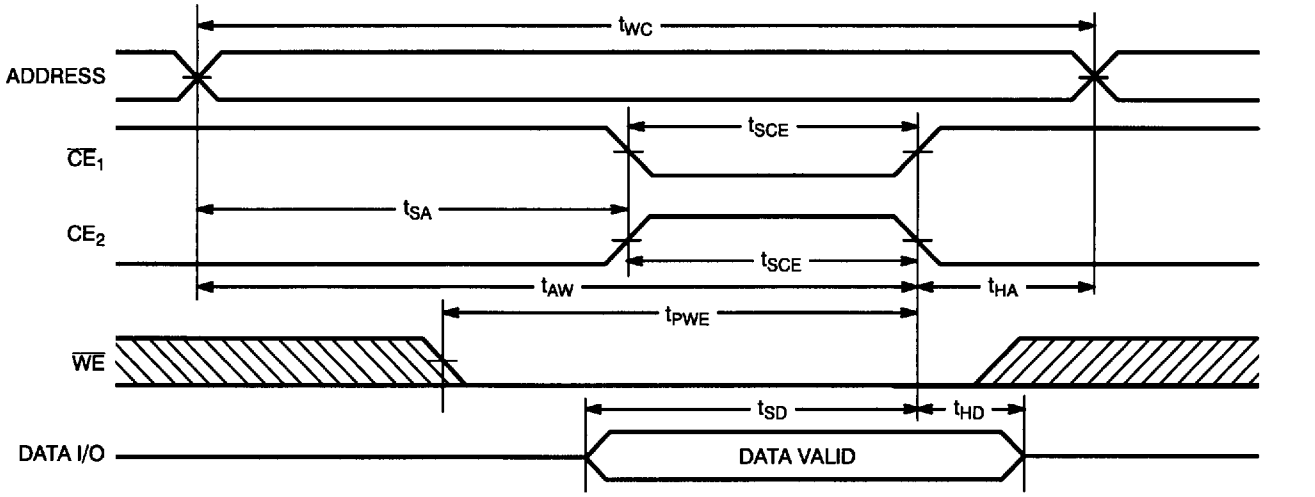
Read Cycle No. 2 ($\overline{OE}$ Controlled)[13, 14]



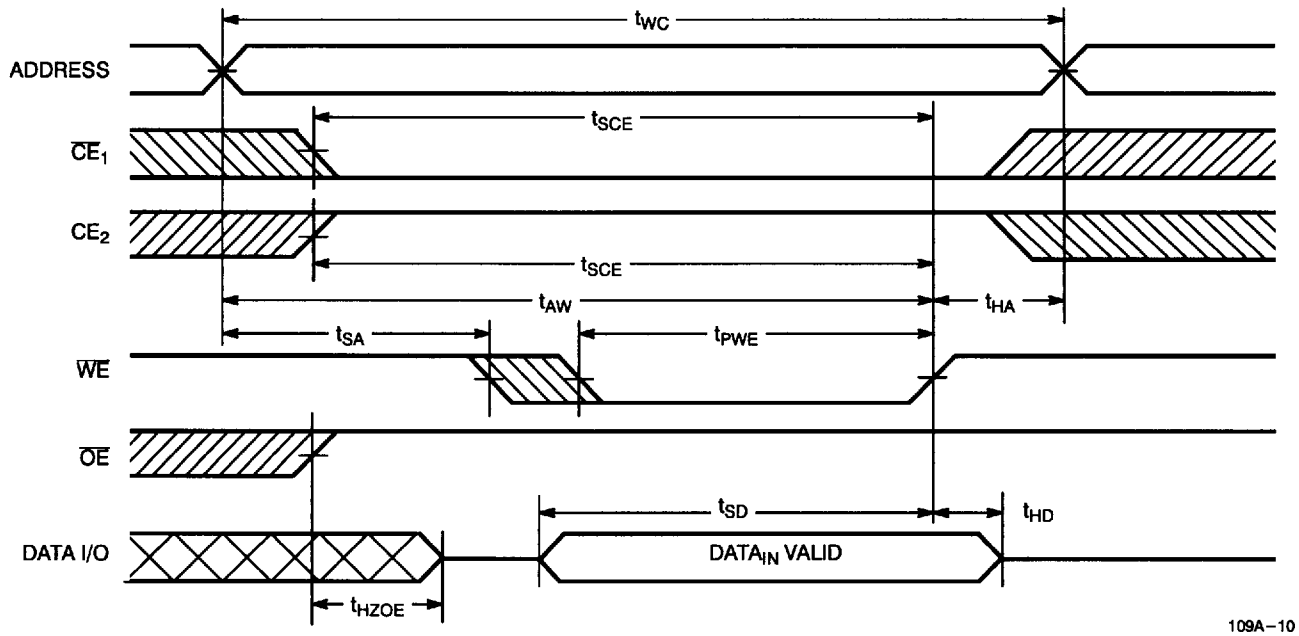
Notes:
12. Device is continuously selected. $\overline{OE}$, $\overline{CE_1}$ = V_{IL}, CE_2 = V_{IH}.
13. $\overline{WE}$ is HIGH for read cycle.
14. Address valid prior to or coincident with $\overline{CE_1}$ transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{CE_1}$ or CE_2 Controlled)[15, 16]



Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)[15, 16]

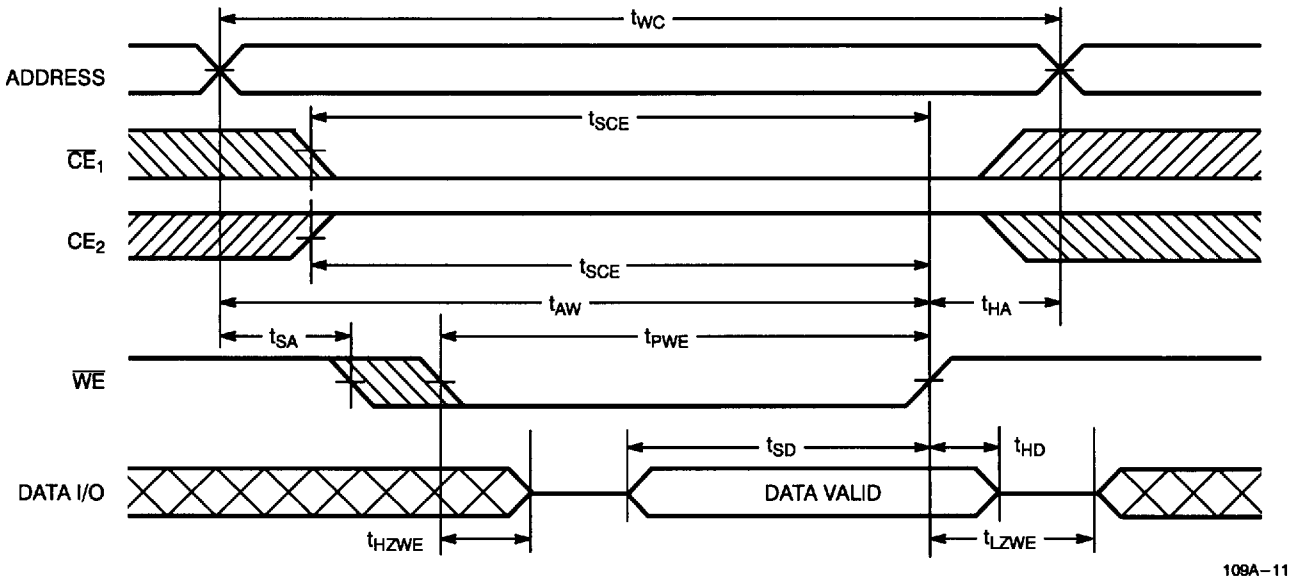


Notes:

15. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
16. If $\overline{CE_1}$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[10, 16]



Truth Table

$\overline{CE_1}$	CE_2	$\overline{OE}$	$\overline{WE}$	Input/Output	Mode	Power
H	X	X	X	High Z	Power-Down	Standby (I_{SB})
X	L	X	X	High Z	Power-Down	Standby (I_{SB})
L	H	L	H	Data Out	Read	Active (I_{CC})
L	H	X	L	Data In	Write	Active (I_{CC})
L	H	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C109A–12PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C109A–12VC	V33	32-Lead (400-Mil) Molded SOJ	
15	CY7C109A–15PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C109A–15VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C109A–15DMB	D44	32-Lead (400-Mil) CerDIP	Military
	CY7C109A–15LMB	L75	32-Pin Leadless Chip Carrier	
20	CY7C109A–20PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C109A–20VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C109A–20DMB	D44	32-Lead (400-Mil) CerDIP	Military
	CY7C109A–20LMB	L75	32-Pin Leadless Chip Carrier	

Shaded area contains advanced information.
Contact factory for "L" version availability.

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C109A–25PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C109A–25VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C109A–25DMB	D44	32-Lead (400-Mil) CerDIP	Military
	CY7C109A–25LMB	L75	32-Pin Leadless Chip Carrier	
35	CY7C109A–35PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C109A–35VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C109A–35DMB	D44	32-Lead (400-Mil) CerDIP	Military
	CY7C109A–35LMB	L75	32-Pin Leadless Chip Carrier	

Contact factory for "L" version availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

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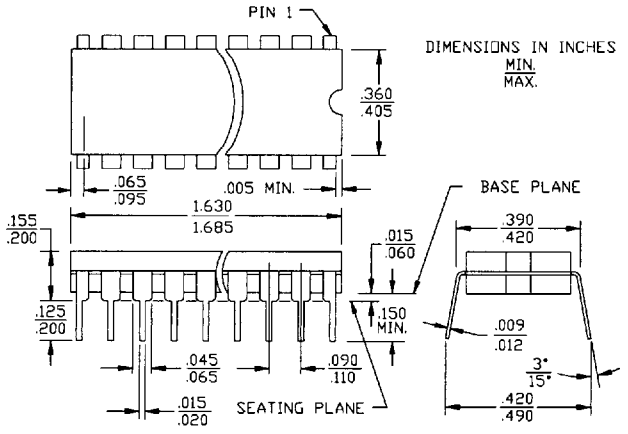
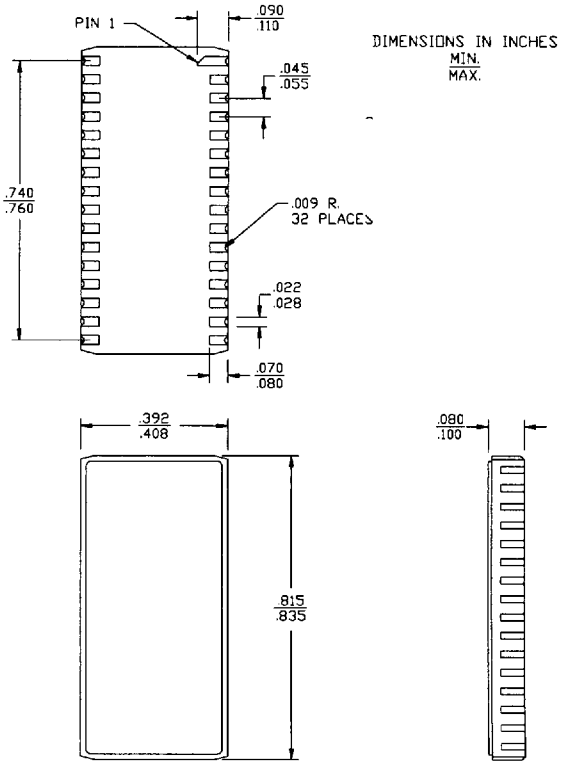
Package Diagrams

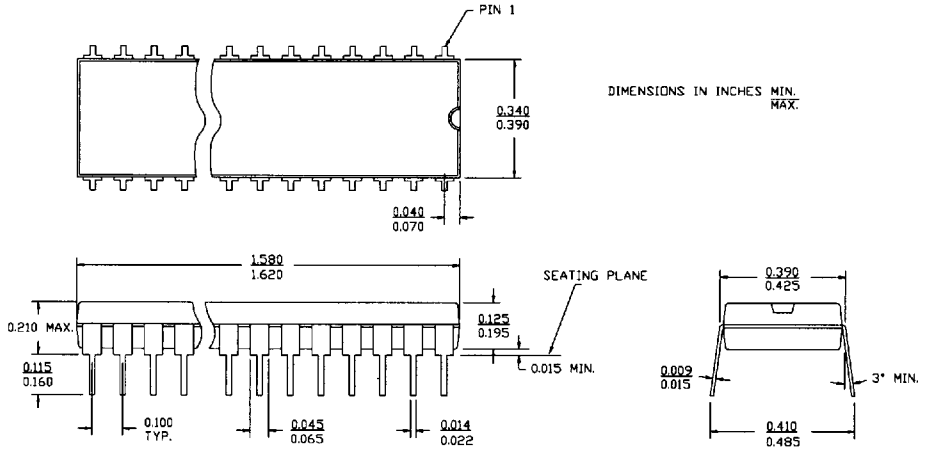
32-Lead (400-Mil) CerDIP D44



32-Pin Leadless Chip Carrier L75



32-Lead (400-Mil) Molded DIP P43



Package Diagrams (continued)

32-Lead (400-Mil) Molded SOJ V33