SONY

CXB1142Q/Q-Y

Quad 4 : 1 Multiplexer with Latch

T-68-11-51

Description

The CXB1142Q is an ultra high speed monolithic ECL IC, which contains four 4 : 1 multiplexers with transparent Latched outputs. The data select (S_0, S_1) inputs determine which data input is enabled. When Latch enable (LEN) input is LOW, the Latch is transparent. The selected data is Latched on the positive transition of the Latch enable input. The Master Reset (MR) overrides all other control inputs and turns Q outputs to LOW.

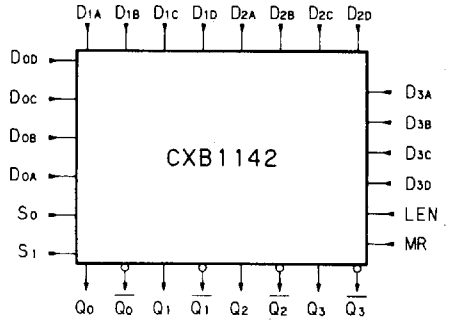
Features

- Typical propagation delay time: T_{pd}=830ps (D_{nA}-D_{nD} to Qn)
- Differential outputs
- Internal pull down resistors on input pins to maintain logic LOW level with the pins left open
- ECL 100K compatible I/O levels

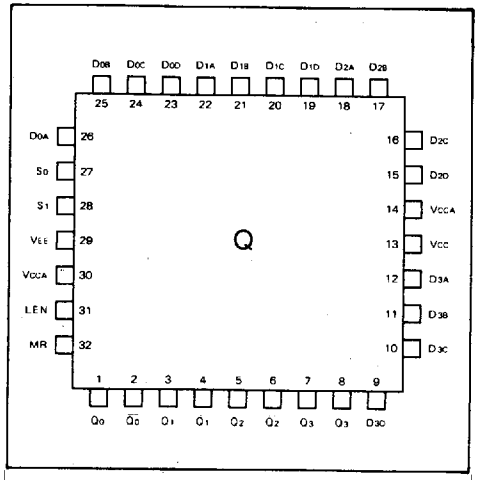
Pin Names

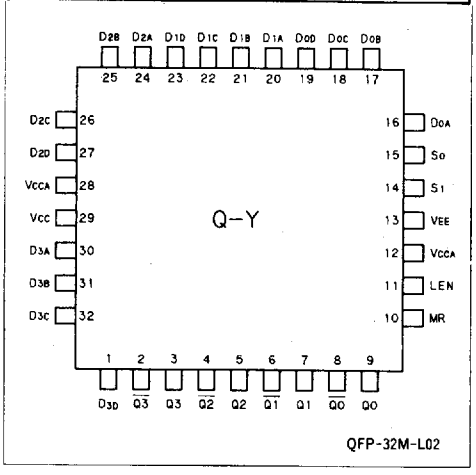
$D_{nA}-\overline{D_{nD}}$, Qn, $\overline{Qn}$	Data inputs / Data outputs
Sn	Data select inputs
LEN	Latch enable input
MR	Direct Master Reset input
V_{CC}	Circuit ground
V_{CCA}	Circuit ground for outputs
V_{EE}	Negative power supply

Logic Symbol



Pin Assignment





QFP-32M-L02

Truth Table

Select inputs		Outputs
S_0	S_1	Qn
L	L	D_{nA}
H	L	D_{nB}
L	H	D_{nC}
H	H	D_{nD}

Note : H ; HIGH voltage Level
L ; LOW voltage Level

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DC Characteristics

$V_{EE}=-4.5V\pm0.3V$, $V_{CC}=V_{CCA}=GND$, $V_{TT}=-2.0V$, $T_C=0°C$ to $+85°C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	I_{EE}		−125	−92	−64	mA

Note: Other DC characteristics; See pages 3-3 and 3-4.

AC Characteristics

$V_{EE}=-4.5V\pm0.3V$, $V_{CC}=V_{CCA}=GND$, $V_{TT}=-2.0V$, $T_C=0°C$ to $+85°C$, $R_T=50\Omega$ to V_{TT}

Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit
Propagation delay time	T_{PLH}	D_{NA} to D_{ND}	Qn	LEN=L	610	820	1070	ps
	T_{PHL}				620	830	1080	
	T_{PLH}	Sn			780	1050	1370	
	T_{PHL}				800	1070	1390	
	T_{PLH}	LEN			650	870	1130	
	T_{PHL}				660	880	1140	
	T_{PLH}	MR			770	1030	1340	
	T_{PHL}				790	1060	1380	
Gate-to-Gate skew	T_{SG-G}	D		LEN=L		60	100	
Set up time	T_S	D, LEN			150			
		Sn, LEN			390			
Hold time	T_H	LEN, D			100			
		LEN, Sn			140			
Release time	T_R	MR, LEN			340			
Min. Pulse width	T_{PW}	MR			520			
Rise time	T_{TLH}	D		20% to 80%		250	330	
Fall time	T_{THL}					240	320	

Note: AC test circuit; See pages 4-3, 4-4 and 4-5.

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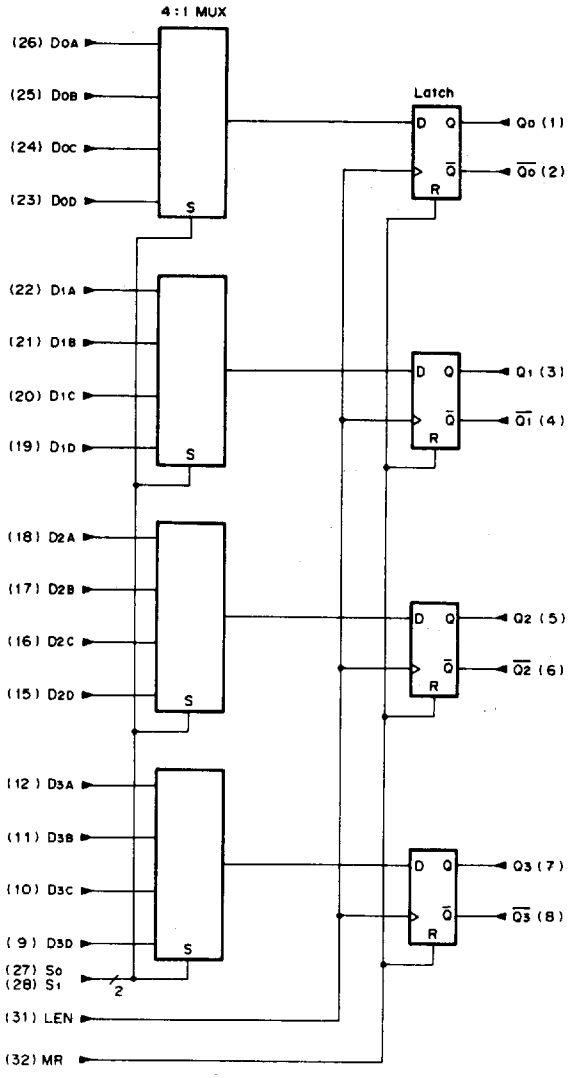
Block Diagram



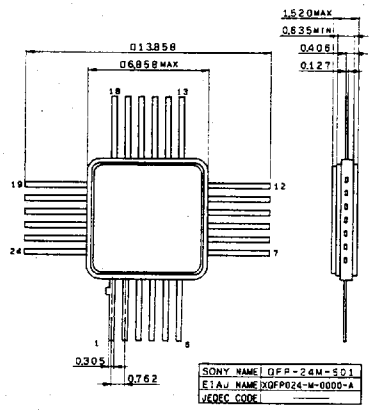
Package Data

T-90-20

Package Outline Uuit: mm

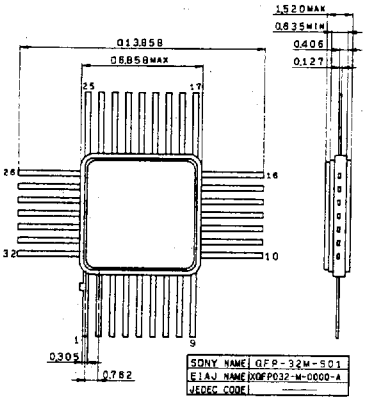
24pin QFP (QFP-24M-S01)

24pin QFP (Metal) 0.3g



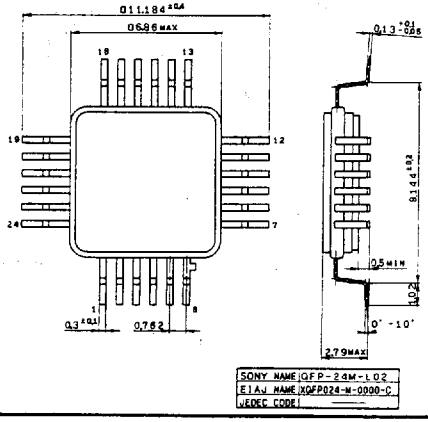
32pin QFP (QFP-32M-S01)

32pin QFP (Metal) 0.2g



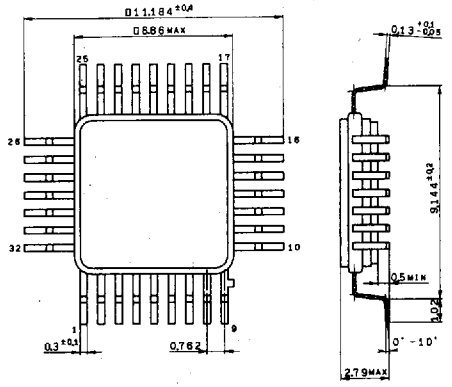
24pin QFP (QFP-24M-L02)

24pin QFP (Metal) 0.3g



32pin QFP (QFP-32M-L02)

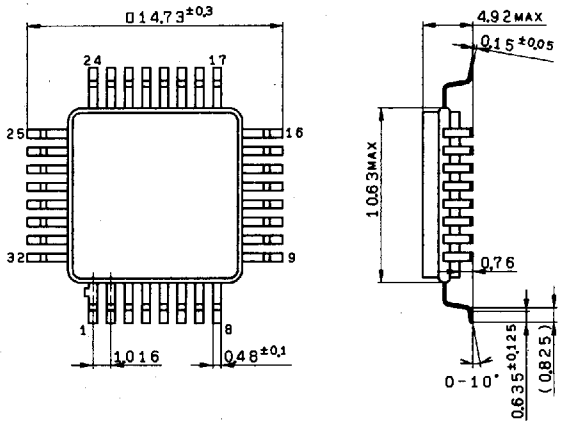
32pin QFP (Metal) 0.2g



SONY NAME	QFP-32M-L02
EIAJ NAME	XQFP032-M-0000-C
JEDEC CODE	———

32pin QFP (QFP-32C-L01)

32pin QFP (Ceramic)



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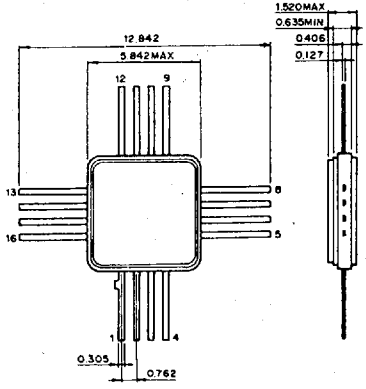
EIAJ NAME	XQFP032-G-0000-A
JEDEC CODE	———

16pin QFP



Package Data

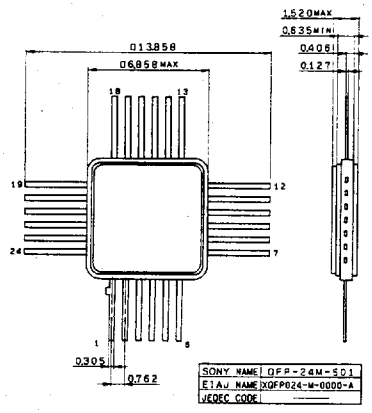
Package Data

T-90-20

Package Outline Uuit: mm

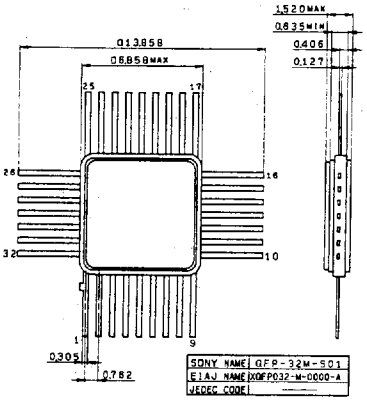
24pin QFP (QFP-24M-S01)

24pin QFP (Metal) 0.3g



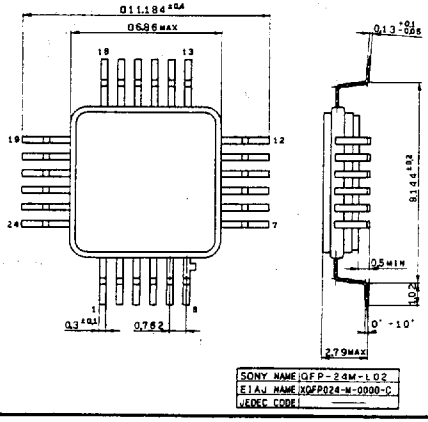
32pin QFP (QFP-32M-S01)

32pin QFP (Metal) 0.2g



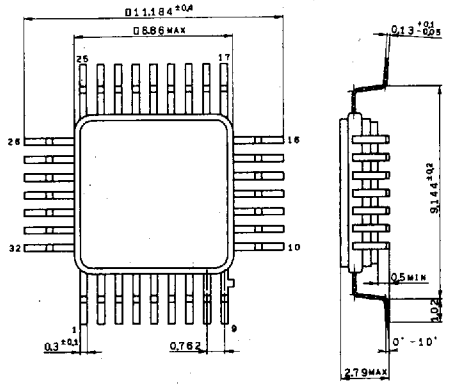
24pin QFP (QFP-24M-L02)

24pin QFP (Metal) 0.3g



32pin QFP (QFP-32M-L02)

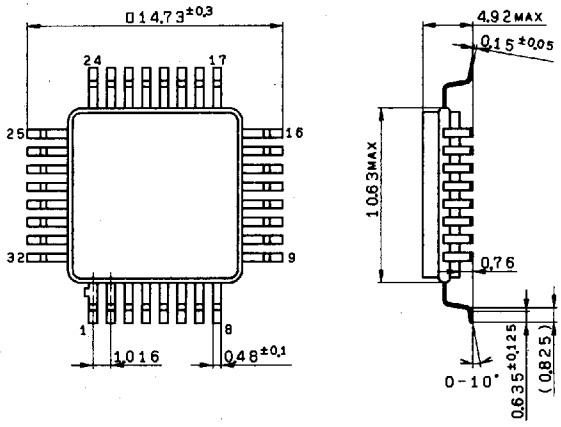
32pin QFP (Metal) 0.2g



SONY NAME	QFP-32M-L02
EIAJ NAME	XQFP032-M-0000-C
JEDEC CODE	———

32pin QFP (QFP-32C-L01)

32pin QFP (Ceramic)



SONY NAME	QFP-32C-L01
EIAJ NAME	XQFP032-G-0000-A
JEDEC CODE	———

16pin QFP