MOTOROLA

Advance Information

32K x 9-Bit Fast Static Random Access Memory

6205C

Commercial Plus and Mil/Aero Applications

AVAILABLE AS

1) JAN: N/A
2) SMD: Pending
3) 883: 6205C - XX/BXAJC

X = CASE OUTLINE AS FOLLOWS:

PACKAGE: DIL: X
FP: Y

XX = Speed in ns (15, 20, 25)

ELECTRICALLY TESTED PER:
MPG6205C

The 6205C is a 294,912 bit static random access memory organized as 32,768 words of 9 bits, fabricated using Motorola's third-generation high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The 6205C is packaged in a 600 mil, 32 pin ceramic side-braze package, and a 32 pin Flat-Pack package.

- Single 5.0 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- Fast Access Time — 15, 20, 25 ns Max.
- Equal Address and Chip Enable Access Times
- Output Enable ($\overline{G}$) feature for Increased System Flexibility and to Eliminate Bus Connection Problems
- Low Power Operation: 145 - 170 mA Maximum AC Current
- Fully TTL Compatible — Three State Outputs

BURN-IN CONDITIONS:
per MIL-STD-883, method: 1015/1005, condition D

V_{CC} = 5.0 V(min)/ 6.0 V(max), R_1 = 2.0 kΩ ± 5%, C_1 = 0.1 µF ± 20%,
V_H = 3.0 V(min)/5.0 V(max), V_L = – 0.5 V(min)/0.5 V(max),

CP1:	100 KHz	CP6:	3.125 KHz	CP11:	97.66 Hz	CP16:	3.052 Hz
CP2:	50 KHz	CP7:	1.563 KHz	CP12:	48.83 Hz	CP17:	1.526 Hz
CP3:	25 KHz	CP8:	0.781 KHz	CP13:	24.41 Hz	CP18:	0.763 Hz
CP4:	12.5 KHz	CP9:	0.391 KHz	CP14:	12.21 Hz		
CP5:	6.25 KHz	CP10:	0.195 KHz	CP15:	6.104 Hz		

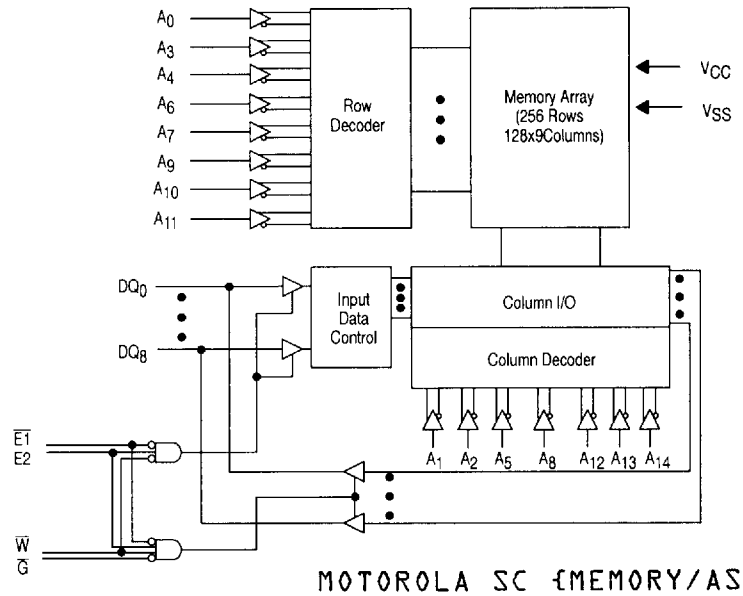
PIN NAME and FUNCTIONS

$A_0 - A_{14}$	Address Inputs
$\overline{W}$	Write Enable
$\overline{E1}$, E2	Chip Enable
$\overline{G}$	Output Enable
$DQ_0 - DQ_8$	Data Input/Output
V_{CC}	+ 5.0 V Power Supply
V_{SS}	Ground
NC	No Connection

This document contains information on a new product. Specifications and information herein are subject to change without notice.

PIN ASSIGNMENTS			
Function	**DIL Case-875-01**	**Flat Pack**	**Burn-In (Condition-D)**
NC	1	1	N.C.
NC	2	2	N.C.
A_8	3	3	CP9 to R_1
A_7	4	4	CP8 to R_1
A_6	5	5	CP7 to R_1
A_5	6	6	CP6 to R_1
A_4	7	7	CP5 to R_1
A_3	8	8	CP4 to R_1
A_2	9	9	CP3 to R_1
A_1	10	10	CP2 to R_1
A_0	11	11	CP1 to R_1
DQ_0	12	12	CP16 to R_1
DQ_1	13	13	CP16 to R_1
DQ_2	14	14	CP16 to R_1
DQ_3	15	15	CP17 to R_1
V_{SS}	16	16	GND
DQ_4	17	17	CP17 to R_1
DQ_5	18	18	CP17 to R_1
DQ_6	19	19	CP18 to R_1
DQ_7	20	20	CP18 to R_1
DQ_8	21	21	CP18 to R_1
$\overline{E1}$	22	22	GND
A_{12}	23	23	CP13 to R_1
$\overline{G}$	24	24	V_{CC}
A_{11}	25	25	CP12 to R_1
A_{10}	26	26	CP11 to R_1
A_9	27	27	CP10 to R_1
A_{13}	28	28	CP14 to R_1
$\overline{W}$	29	29	GND
E2	30	30	V_{CC}
A_{14}	31	31	CP15 to R_1
V_{CC}	32	32	V_{CC}, C_1 to GND

BLOCK DIAGRAM



TRUTH TABLE							
$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	X	Not Selected	I_{SB1}, I_{SB2}	High Z	—
X	L	X	X	Not Selected	I_{SB1}, I_{SB2}	High Z	—
L	H	H	H	Output Disabled	I_{CCA}	High Z	—
L	H	L	H	Read	I_{CCA}	D_{OUT}	Read Cycle
L	H	X	L	Write	I_{CCA}	High Z	Write Cycle

X = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS: (See Note)			
Rating	**Symbol**	**Value**	**Unit**
Power Supply Voltage	V_{CC}	– 0.5 to +7.0	V
Voltage Relative to V_S for Any Pin Except V_{CC}	V_{IN}, V_{OUT}	– 0.5 to V_{CC} +0.5	V
Output Current (per I/O)	I_{OUT}	±30	mA
Power Dissipation (T_A = 85°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	–55 to +125	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Temperature Range	T_A	–55 to +125	°C
Maximum Junction Temperature	T_J	+150	°C
Thermal Resistance, Junction to Case	θ_{JD}	per MIL-M-38510 appendix C	°C/W

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could effect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = –55°C to +125°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS					
Parameters	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}**	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}*	–0.5	—	0.8	V

* V_{IL} (max) = 0.5 Vdc for Output Enable ($\overline{G}$); and Chip Enable ($\overline{E}$)

** V_{IH} (max) = V_{CC} + 0.3 Vdc; V_{IH} (max) = V_{CC} + 2 Vac (pulse width ≤ 20 ns)

DC CHARACTERISTICS					
Parameters		**Symbol**	**Min**	**Max**	**Unit**
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	—	±1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, or $\overline{G}$ = V_{IH}, V_{OUT} = 0 to 5.5 V)		$I_{lkg(O)}$	—	±1.0	µA
Power Supply Current ($\overline{E}$ = V_{IL}, V_{IN} = V_{IH}, or V_{IL}, I_{OUT} = 0, V_{CC} = max, F = 1/t_{AVAV})	15 ns 20 ns 25 ns	I_{CCA} I_{CCA} I_{CCA}	— — —	170 155 145	mA mA mA
Standby Current ($\overline{E1}$ = V_{IH}), or E2 = V_{IL}, V_{CC} = max, f = fmax,	15 ns 20 ns 25 ns	I_{SB1} I_{SB1} I_{SB1}	— — —	50 45 40	mA mA mA
Standby Current ($\overline{E1}$ ≥ V_{CC} – 2.0 V, V_{CC} = max, f = 0 MHz, or E2 ≤ V_{SS} + 0.2 V, V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{CC} – 0.2 V)		I_{SB2}	—	20	mA
Output Low Voltage (I_{OL} = 8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)		V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)			
Characteristics	**Symbol**	**Max**	**Unit**
Input Capacitance (Control Pins) $\overline{E1}$, E2, $\overline{G}$, $\overline{W}$	C_{in}	8	pF
Output Capacitance	C_{out}	8	pF

AC TEST LOADS OR EQUIVALENT

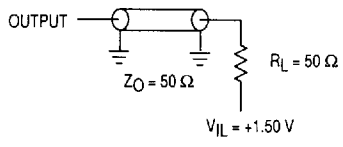


Figure 1A.

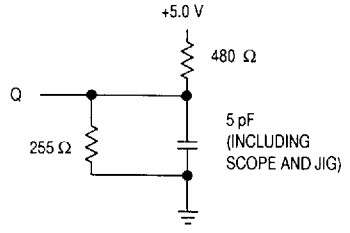


Figure 1B.

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = − 55°C to + 125°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level	1.5 V
Input Pulse levels	0 to 3.0 V
Input Rise/Falls Time	≥ 5.0 ns
Output Timing Measurement Reference Level	1.5 V
Output Load	See Figure 1A

READ CYCLE (See Notes 1, and 2)

Parameters	Symbol	Alternate Symbol	6205C-15		6205C-20		6205C-25		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	15	—	20	—	25	—	ns	3
Address Access Time	t_{AVQV}	t_{AA}	—	15	—	20	—	25	ns	—
Enable Access Time	t_{ELQV}	t_{ACS}	—	15	—	20	—	25	ns	4
Output Enable Access Time	t_{GLQV}	t_{OE}	—	8	—	10	—	12	ns	—
Output Hold from Address Change	t_{AXQX}	t_{OH}	4	—	4	—	4	—	ns	—
Enable Low to Output Active	t_{ELQX}	t_{CLZ}	4	—	4	—	4	—	ns	5, 6, 7
Enable High to Output High-Z	t_{EHQZ}	t_{CHZ}	0	8	0	9	0	10	ns	5, 6, 7
Output Enable Low to Output Active	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	ns	5, 6, 7
Output Enable High to Output High-Z	t_{GHQZ}	t_{OHZ}	0	7	0	8	0	10	ns	5, 6, 7

NOTES:
1. $\overline{W}$ is high at all times for read cycle.
2. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is the opposite polarity to $\overline{E}$.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. At any given voltage and temperature, t_{EHQZ}(max) is less than t_{ELQX}(min), and t_{GHQZ}(max) is less than t_{GLQX}(min), both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E1}$ = V_{IL}, E2 = V_{IH}, $\overline{G}$ = V_{IL}).

WRITE CYCLE 1 (See Notes 1, 2 and 3)

Parameters	Symbol	Alternate Symbol	6205C-15		6205C-20		6205C-25		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	15	—	20	—	25	—	ns	4
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	ns	—
Address Valid to End of Write	t_{AVWH}	t_{AW}	12	—	15	—	20	—	ns	—
Write Pulse Width	t_{WLWH}, t_{WLEH}	t_{WP}	12	—	15	—	20	—	ns	—
Write Pulse Width, $\overline{G}$ High	t_{WLWH}, t_{WLEH}	t_{WP}	10	—	12	—	15	—	ns	5
Data Valid to End of Write	t_{DVWH}	t_{DW}	7	—	8	—	10	—	ns	—
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	ns	—
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	7	0	8	0	10	ns	6, 7, 8
Write High to Output Active	t_{WHQX}	t_{OW}	4	—	4	—	4	—	ns	6, 7, 8
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	ns	—

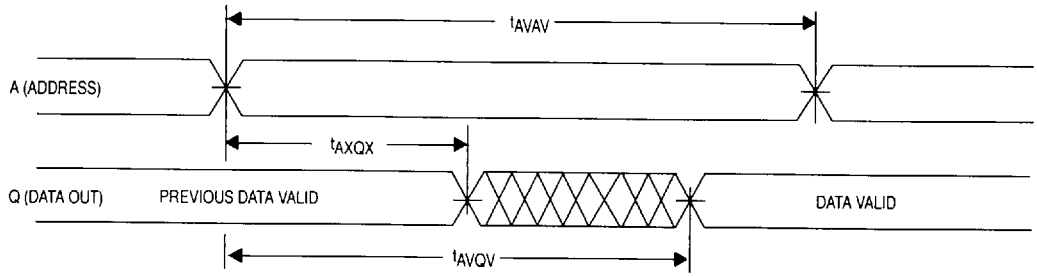
NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is opposite polarity to $\overline{E1}$.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. If $\overline{G}$ ≥ V_{IH}, the output will remain in a high impedance state.
6. At any given voltage and temperature, t_{WQLZ}(max) is less than t_{WHQX}(min), both for a given device and from device to device.
7. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
8. This parameter is sampled and not 100% tested.

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1, and 2)

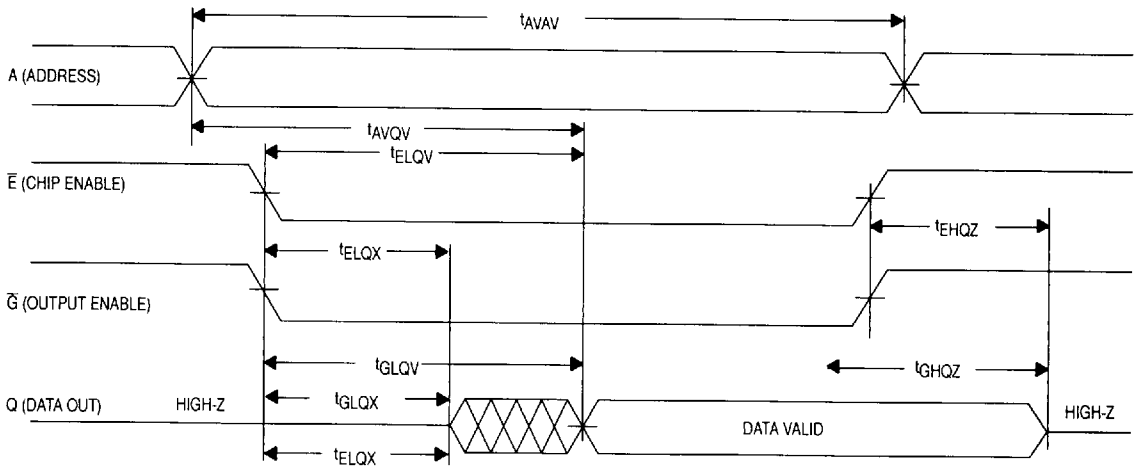
Parameters	Symbol	Alternate Symbol	6205C-15		6205C-20		6205C-25		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	15	—	20	—	25	—	ns	3
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	ns	—
Address Valid to End of Write	t_{AVEH}	t_{AW}	12	—	15	—	20	—	ns	—
Enable to End of Write	t_{ELEH}, t_{ELWH}	t_{WC}	10	—	12	—	15	—	ns	4, 5
Data Valid to End of Write	t_{DVEH}	t_{DW}	7	—	8	—	10	—	ns	—
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	ns	—
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	ns	—

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is opposite polarity to $\overline{E}$.
3. All timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance state.

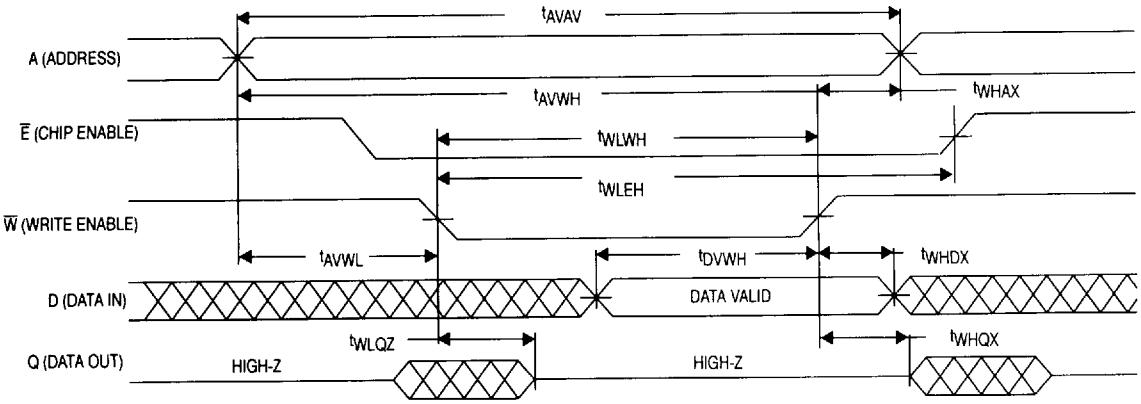
READ CYCLE 1 (See Note 8)



READ CYCLE 2 (See Note 4)



WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)



WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)