| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
| | | | |

| | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| REV | | | | | | | | | | | | | | | | | | | | | | | | |
| SHEET | | | | | | | | | | | | | | | | | | | | | | | | |
| REV | | | | | | | | | | | | | | | | | | | | | | | | |
| SHEET | | | | | | | | | | | | | | | | | | | | | | | | |
| REV STATUS OF SHEETS | REV | | | | | | | | | | | | | | | | | | | | | | | |
| | SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | | | | | | | |

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY Joseph A. Kerby

CHECKED BY Charles E. Besore

APPROVED BY

DRAWING APPROVAL DATE 91-08-30

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, LINEAR, MICROPROCESSOR COMPATIBLE, 12-BIT ANALOG-TO-DIGITAL CONVERTERS, MULTICHIP

| SIZE | CAGE CODE | |
|---|---|---|
| A | 67268 | 5962-88615 |

SHEET 1

DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E068

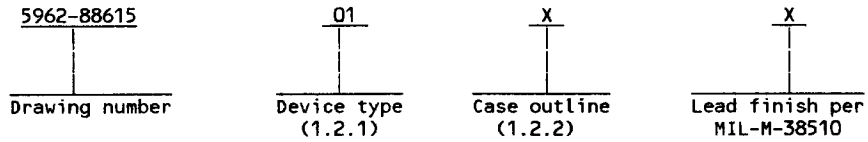
DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:




1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

| Device type | Generic number | Circuit function |
|---|---|---|
| 01 | 674AU | Multi-chip, high performance, 12-bit A/D converter with microprocessor interface |
| 02 | 674AT | Multi-chip, medium performance, 12-bit A/D converter with microprocessor interface |

1.2.2 Case outline(s). The case outline(s) shall be as designated in appendix C of MIL-M-38510, and as follows:

| Outline letter | Case outline |
|---|---|
| X | D-10 (28-lead, 1.490" x .610" x .232"), dual-in-line package |
| 3 | C-4 (28-terminal, 460" x .460" x .100"), square chip carrier package |

1.3 Absolute maximum ratings.

| | |
|---|---|
| $V_{CC}$ to digital common | 0 V dc to +16.5 V dc |
| $V_{EE}$ to digital common | 0 V dc to -16.5 V dc |
| $V_{LOGIC}$ to digital common | 0 V dc to +7 V dc |
| Analog common to digital common | ±1 V dc |
| Control inputs (CE, $\overline{CS}$, $A_0$, 12/$\overline{8}$, R/$\overline{C}$) to digital common | -0.5 V dc to $V_{LOGIC}$ +0.5 V dc |
| Analog inputs (REF IN, BIP OFF, 10 $V_{IN}$) to analog common | ±16.5 V dc |
| 20 $V_{IN}$ analog input voltage to analog common | ±24 V dc |
| $V_{REF\ OUT}$ | Indefinite short to common<br>10 ms short to $V_{CC}$ |
| Power dissipation ($T_A$ = +25°C): | 833 mW |
| Lead temperature (soldering, 10 seconds) | +300°C |
| Storage temperature range | -65°C to +150°C |
| Junction temperature ($T_J$) | +175°C |
| Thermal resistance, junction-to-case ($\Theta_{JC}$) | See MIL-M-38510, appendix C |
| Thermal resistance, junction-to-ambient($\Theta_{JA}$): | |
| Case X | +60°C/W |
| Case 3 | +70°C/W |

1.4 Recommended operating conditions.

| | |
|---|---|
| Logic supply ($V_{LOGIC}$) | +4.75 V dc to +5.25 V dc |
| Positive supply ($V_{CC}$) | +11.4 V dc to +16.5 V dc |
| Negative supply ($V_{EE}$) | -11.4 V dc to -16.5 V dc |
| Ambient operating temperature range ($T_A$) | -55°C to +125°C |



Powered by ICminer.com Electronic-Library Service CopyRight 2003

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD,s).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).



Powered by ICminer.com Electronic-Library Service CopyRight 2003

TABLE I. Electrical performance characteristics.

| Test | Symbol | Conditions 1/ $-55°C \le T_A \le +125°C$ $V_{CC}$ = +15 V, $V_{LOGIC}$ = +5 V $V_{EE}$ = -15 V unless otherwise specified | Device types | Group A subgroups | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Power supply current from $V_{LOGIC}$ 2/ | $I_{LOGIC}$ | Three-state outputs | All | 1, 2, 3 | | +45 | mA |
| Power supply current from $V_{CC}$ 2/ | $I_{CC}$ | | All | 1, 2, 3 | | +5 | |
| Power supply current from $V_{EE}$ 2/ | $I_{EE}$ | | All | 1, 2, 3 | -29 | | |
| Integral linearity error | LE | Unipolar 10 V span<br>Bipolar 20 V span | All | 1 | -0.5 | +0.5 | LSB |
| | | | | 2, 3 | -1.0 | +1.0 | |
| Differential linearity error (minimum resolution for which no missing codes are guaranteed) | DLE | Unipolar 10 V span<br>Bipolar 20 V span | All | 1, 2, 3 | 12 | | Bits |
| Unipolar offset voltage error | $V_{IO}$ | 10 V span | All | 1 | -2 | +2 | LSB |
| Unipolar offset voltage drift | $\frac{\Delta V_{IO}}{\Delta T}$ | | | 2, 3 | -1 | +1 | |
| Bipolar offset error | $B_Z$ | 20 V span | All | 1 | -4 | +4 | |
| Bipolar offset drift | $\frac{\Delta B_Z}{\Delta T}$ | | 01 | 2, 3 | -1 | +1 | |
| | | | 02 | 2, 3 | -2 | +2 | |
| Gain error | $A_E$ | With 50Ω resistor from REF OUT to REF IN<br>Bipolar 20 V span<br>$T_A$ = +25°C | All | 1 | -0.25 | +0.25 | % of FS |
| Gain error drift | $\frac{\Delta A_E}{\Delta T}$ | Bipolar 20 V span | 01 | 2, 3 | | 12.5 | ppm/°C |
| | | | 02 | | | 25 | |

See footnotes at end of table.



Powered by ICminer.com Electronic-Library Service CopyRight 2003

TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions 1/ $-55°C \le T_A \le +125°C$ $V_{CC}$ = +15 V, $V_{LOGIC}$ = +5 V $V_{EE}$ = -15 V unless otherwise specified | Device types | Group A subgroups | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Power supply sensitivity to $V_{CC}$ 3/ 4/ | +PSS1 | Unipolar 10 V span | All | 1, 2, 3 | -1 | +1 | LSB |
| Power supply sensitivity to $V_{LOGIC}$ 3/ 5/ | +PSS2 | Unipolar 10 V span | All | 1, 2, 3 | -0.5 | +0.5 | LSB |
| Power supply sensitivity to $V_{EE}$ 3/ 6/ | -PSS3 | Unipolar 10 V span | All | 1, 2, 3 | -1 | +1 | LSB |
| Input impedance 2/ | $Z_{IN}$ | 10 V span | All | 1, 2, 3 | 3 | 7 | kΩ |
| | | 20 V span | All | 1, 2, 3 | 6 | 14 | |
| Internal reference voltage 7/ | $V_{REF}$ | Bipolar 20 V span $I_{REFOUT}$ = 2 mA | All | 1, 2, 3 | +9.9 | +10.1 | V |
| Logic input high voltage (CE, CS, 12/8, R/C, $A_0$) 2/ 8/ | $V_{IH}$ | Logic "1" | All | 1, 2, 3 | +2.0 | | V |
| Logic input low voltage (CE, CS, 12/8, R/C, $A_0$) 2/ 8/ | $V_{IL}$ | Logic "0" | All | 1, 2, 3 | | +0.8 | V |
| Logic input current 2/ | $I_{IN(LOG)}$ | $V_{IH}$ = 5.0 V $V_{IL}$ = 0.0 V | All | 1, 2, 3 | -100 | +100 | μA |

See footnotes at end of table.



Powered by ICminer.com Electronic-Library Service CopyRight 2003

TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions 1/ $-55°C \le T_A \le +125°C$, $V_{CC}$ = +15 V, $V_{LOGIC}$ = +5 V, $V_{EE}$ = -15 V unless otherwise specified | Device types | Group A subgroups | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Logic low output voltage 2/ (DB11-DB0, STS) | $V_{OL}$ | Logic "0", $I_{sink}$ = +1.6 mA | All | 1, 2, 3 | | +0.4 | V |
| Logic high output voltage 2/ (DB11-DB0) | $V_{OH}$ | Logic "1", $I_{source}$ = 500 µA | All | 1, 2, 3 | +2.4 | | V |
| Three-state output leakage current (DB11-DB0) | $I_{OLT}$ | High-Z state, $V_{applied}$ = 5.0 V | All | 1, 2, 3 | -20 | +20 | µA |
| Functional tests 2/ | | (See 4.3.1c) | All | 7, 8 | | | |
| Low R/C pulse width 9/ | $t_{HRL}$ | See figure 3 | All | 9, 10, 11 | 50 | | ns |
| STS delay from R/C 10/ | $t_{DS}$ | | | | | 200 | |
| Data valid after R/$\overline{C}$ low 11/ | $t_{HDR}$ | | | | 25 | | |
| STS delay after valid data | $t_{HS}$ | | | | 30 | 600 | |
| High R/$\overline{C}$ pulse width 9/ | $t_{HRH}$ | | | | 150 | | |
| Data access time 12/ | $t_{DDR}$ | | | | | 150 | |
| STS delay from CE 10/ | $t_{DSC}$ | See figure 4 | | | | 200 | |
| CE pulse width 9/ | $t_{HEC}$ | | | | 50 | | |
| $\overline{CS}$ to CE setup | $t_{SSC}$ | | | | 50 | | |
| $\overline{CS}$ low during CE high | $t_{HSC}$ | | | | 50 | | |
| R/$\overline{C}$ to CE setup | $t_{SRC}$ | | | | 50 | | |

See footnotes at end of table.



Powered by ICminer.com Electronic-Library Service CopyRight 2003

TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions 1/ $-55°C \le T_A \le +125°C$, $V_{CC}$ = +15 V, $V_{LOGIC}$ = +5 V, $V_{EE}$ = -15 V unless otherwise specified | Device types | Group A subgroups | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| R/$\overline{C}$ low during CE high | $t_{HRC}$ | See figure 4 | All | 9, 10, 11 | 50 | | ns |
| $A_0$ to CE setup | $t_{SAC}$ | | | | 0 | | |
| $A_0$ valid during CE high | $t_{HAC}$ | | | | 50 | | |
| Conversion time 13/ | $t_C$ | 8-bit cycle, see figure 4 | All | 9, 10, 11 | 6 | 10 | µs |
| | | 12-bit cycle, see figure 4 | | | 9 | 15 | |
| Access time (from CE) 12/ | $t_{DD}$ | See figure 5 | All | 9, 10, 11 | | 150 | ns |
| Data valid after $\overline{CE}$ low 11/ | $t_{HD}$ | | | | 25 | | |
| Output float delay 11/ | $t_{HL}$ | | | | | 150 | |
| $\overline{CS}$ to CE setup | $t_{SSR}$ | | | | 50 | | |
| R/$\overline{C}$ to CE setup | $t_{SRR}$ | | | | 0 | | |
| $A_0$ to CE setup | $t_{SAR}$ | | | | 50 | | |
| $\overline{CS}$ valid after CE low | $t_{HSR}$ | | | | 0 | | |
| R/$\overline{C}$ high after CE low | $t_{HRR}$ | | | | 0 | | |
| $A_0$ valid after CE low | $t_{HAR}$ | | | | 50 | | |

See footnotes at end of table.



Powered by ICminer.com Electronic-Library Service CopyRight 2003

TABLE I. Electrical performance characteristics - Continued.

1/ $12/\overline{8}$ connected to $V_{LOGIC}$, $A_0$ and $\overline{CS}$ at logic "0", CE at logic "1". 10 V unipolar: 50Ω resistor pin 8 to pin 10, 50Ω resistor pin 12 to ground. Analog input connected to pin 13. 20 V bipolar: 50Ω resistor pin 8 to pin 12, 50Ω resistor pin 8 to pin 10. Analog input connected to pin 14. These conditions apply unless otherwise noted.

2/ Device types are tested to the conditions stated in table I, but are guaranteed to the specified limits for the following variations in the supply voltage ranges. $V_{LOGIC}$ = 5 V to ±5%, $V_{CC}$ = +12 V ±5% and +15 V to ±10%, $V_{EE}$ = -12 V ±5% and -15 V ±10%.

3/ Maximum change in full scale calibration due to supply voltage shifts. Full scale calibration to be measured at minimum and maximum voltage settings for each individual supply.

4/ +13.5 V ≤ $V_{CC}$ ≤ +16.5 V, $V_{LOGIC}$ = 5 V, $V_{EE}$ = -15 V and +11.4 V ≤ $V_{CC}$ ≤ +12.6 V, $V_{LOGIC}$ = 5 V, $V_{EE}$ = -12 V.

5/ 4.75 V ≤ $V_{LOGIC}$ ≤ 5.25 V, $V_{CC}$ = 15 V, $V_{EE}$ = -15 V.

6/ -16.5 V ≤ $V_{EE}$ ≤ -13.5 V, $V_{LOGIC}$ = 5 V, $V_{CC}$ = +15 V and -12.6 V ≤ $V_{EE}$ ≤ -11.4 V, $V_{LOGIC}$ = 5 V, $V_{CC}$ = +12 V.

7/ Reference should be buffered for operation on ±12 V supplies. External load should not change during conversion.

8/ $12/\overline{8}$ is not TTL compatible and must be hard-wired to $V_{LOGIC}$ or digital common.

9/ Pulse width is measured at the Schottky TTL input logic threshold voltage (1.3 V).

10/ $t_{DS}$ and $t_{DSC}$ are measured from the point when the input signal crosses the Schottky TTL logic threshold voltage (1.3 V) to when the STS output reaches 2.4 V. No external loading is applied to STS.

11/ $t_{HDR}$, $t_{HD}$, and $t_{HL}$ are measured from the point when the input signal crosses the Schottky TTL logic threshold voltage (1.3 V), to when the output voltage has moved 0.5 V in the direction of its final high impedance output voltage. Each individual data bit (DB0 - DB11) is measured for both logic one to "high Z" and logic zero to "high Z" transitions. External loading is as shown on figure 6.

12/ $t_{DDR}$ and $t_{DD}$ are measured from the point when the input signal crosses the Schottky TTL logic threshold voltage (1.3 V), to when the output crosses either 2.4 V for a logic one, or 0.4 V for a logic zero. Each individual data bit (DB0 - DB11) is measured for both "high Z" to logic zero transitions. External loading is as shown on figure 7.

13/ $t_c$ is measured as the time from when the STS line crosses the 1.0 V level, going positive, to when it crosses the 1.0 V level going negative. No external loading is applied to STS.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.



Powered by ICminer.com Electronic-Library Service CopyRight 2003

| Device types | 01 and 02 |
|---|---|
| Case outlines | X and 3 |
| Terminal number | Terminal symbol |
| 1 | +5 V supply ($V_{LOGIC}$) |
| 2 | Data mode select ($12/\overline{8}$) |
| 3 | Chip select ($\overline{CS}$) |
| 4 | Byte address/short cycle ($A_0$) |
| 5 | Read/convert ($R/\overline{C}$) |
| 6 | Chip enable (CE) |
| 7 | +12 V/ +15 V supply ($V_{CC}$) |
| 8 | +10 V reference (REF OUT) |
| 9 | Analog common (AC) |
| 10 | Reference input (REF IN) |
| 11 | -12 V/ -15 supply ($V_{EE}$) |
| 12 | Bipolar offset (BIP OFF) |
| 13 | 10 V span input (10 $V_{IN}$) |
| 14 | 20 V span input (20 $V_{IN}$) |
| 15 | Digital common (DC) |
| 16 | DB0 |
| 17 | DB1 |
| 18 | DB2 |
| 19 | DB3 |
| 20 | DB4 |
| 21 | DB5 |
| 22 | DB6 |
| 23 | DB7 |
| 24 | DB8 |
| 25 | DB9 |
| 26 | DB10 |
| 27 | DB11 (MSB) |
| 28 | Status (STS) |

FIGURE 1. Terminal connections.



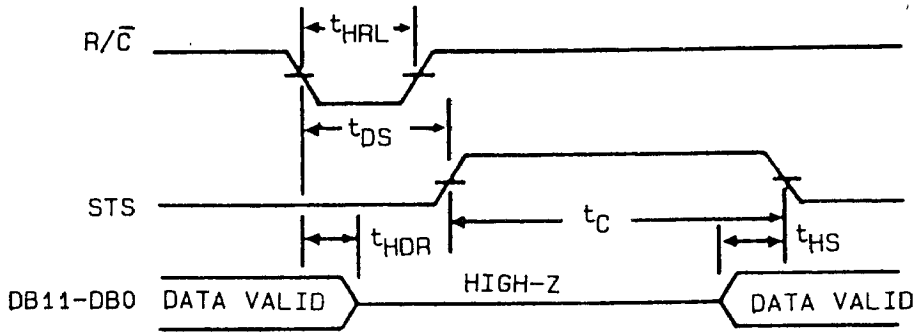
Powered by ICminer.com Electronic-Library Service CopyRight 2003

| CE | $\overline{CS}$ | R/$\overline{C}$ | 12/$\overline{8}$ | $A_0$ | Operation |
|---|---|---|---|---|---|
| 0 | X | X | X | X | None |
| X | 1 | X | X | X | None |
| 1 | 0 | 0 | X | 0 | Initiate 12-bit conversion |
| 1 | 0 | 0 | X | 1 | Initiate 8-bit conversion |
| 1 | 0 | 1 | 1 | X | Enable 12-bit parallel output |
| 1 | 0 | 1 | 0 | 0 | Enable 8 most significant bits |
| 1 | 0 | 1 | 0 | 1 | Enable 4LSBs + 4 trailing zeros |

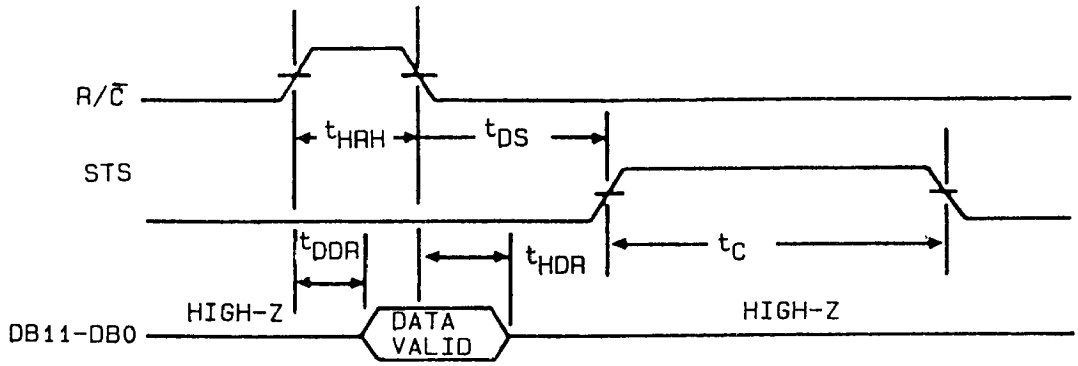
FIGURE 2. Truth table.



Powered by ICminer.com Electronic-Library Service CopyRight 2003




LOW PULSE FOR R/C - OUTPUTS ENABLED AFTER CONVERSION




HIGH PULSE FOR R/C - OUTPUTS ENABLED WHILE R/C HIGH, OTHERWISE HIGH-Z

FIGURE 3. High/low pulse for R/C.



Powered by ICminer.com Electronic-Library Service CopyRight 2003

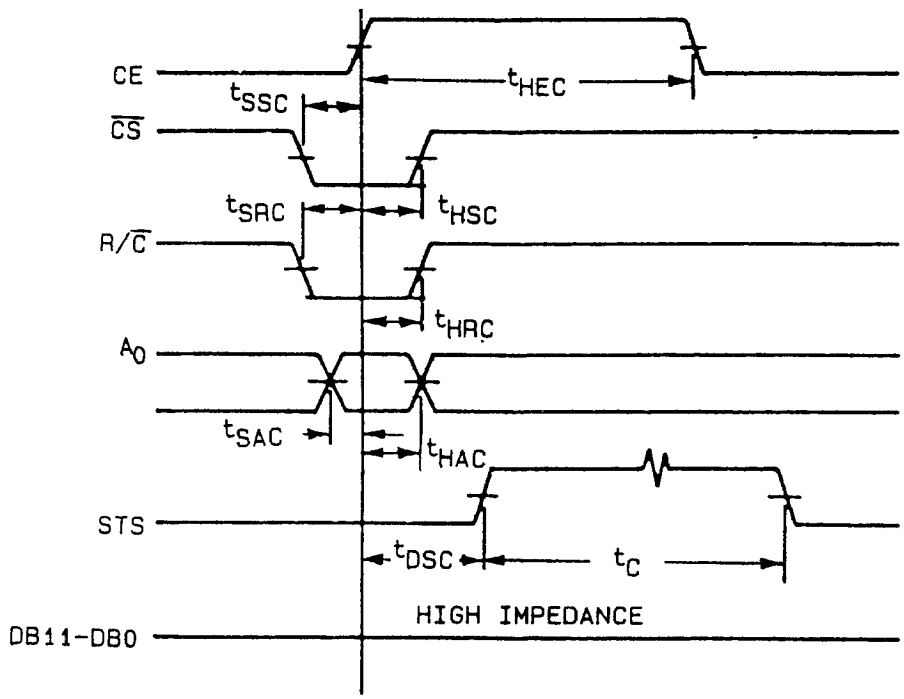



FIGURE 4. Convert start timing.



Powered by ICminer.com Electronic-Library Service CopyRight 2003

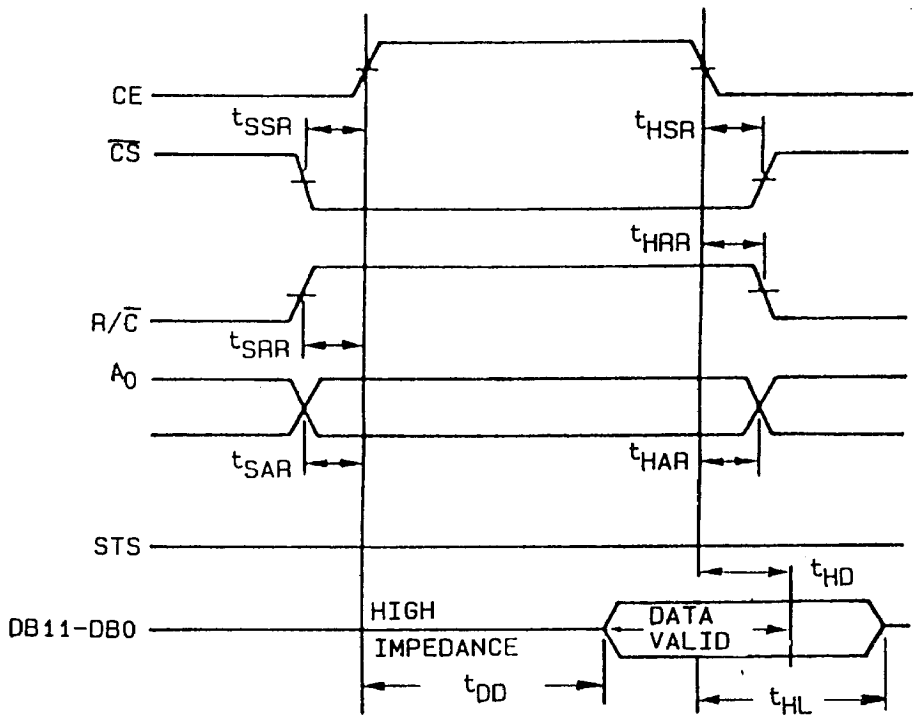



FIGURE 5. Read cycle timing.

| | | | |
|---|---|---|---|
| STANDARDIZED<br>MILITARY DRAWING<br>DEFENSE ELECTRONICS SUPPLY CENTER<br>DAYTON, OHIO 45444 | SIZE<br>A | | 5962-88615 |
| | | REVISION LEVEL | SHEET<br>13 |



Powered by ICminer.com Electronic-Library Service CopyRight 2003

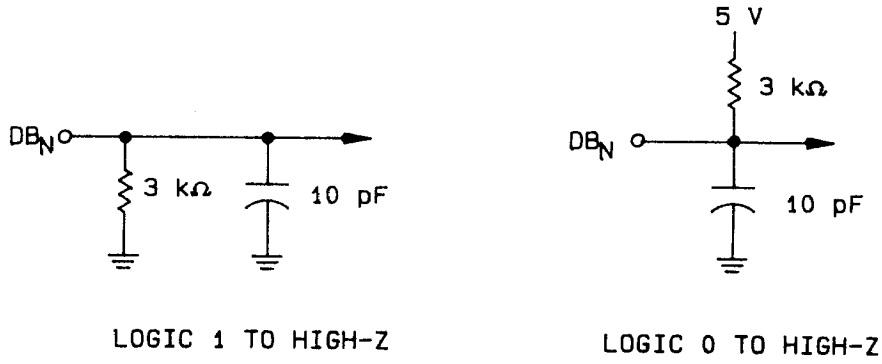



FIGURE 6. Load circuit for output float delay test.

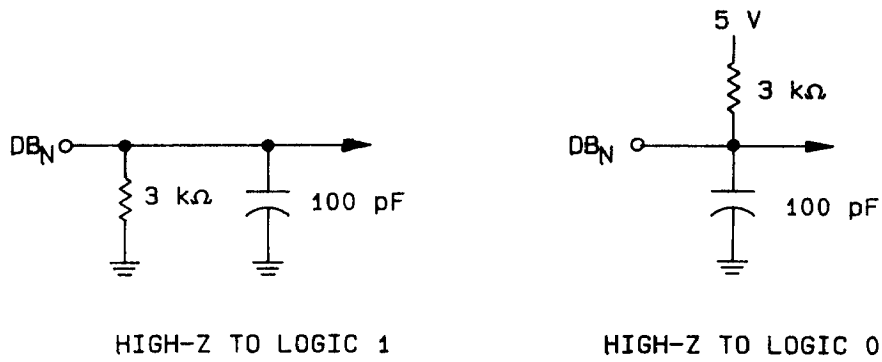



FIGURE 7. Load circuit for access time test.



Powered by ICminer.com Electronic-Library Service CopyRight 2003

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) $T_A$ = +125°C, minimum

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. Internal visual inspection shall be in accordance with method 2017 of MIL-STD-883.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 tests shall verify the truth table on figure 2.

4.3.2 Groups C and D inspection.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883:

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) $T_A$ = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.



Powered by ICminer.com Electronic-Library Service CopyRight 2003

TABLE II. Electrical test requirements.

| MIL-STD-883 test requirements | Subgroups (per method 5005, table I) |
|---|---|
| Interim electrical parameters (method 5004) | 1 |
| Final electrical test parameters (method 5004) | 1*, 2, 3 |
| Group A test requirements (method 5005) | 1, 2, 3, 7, 8, 9 10**, 11** |
| Group C and D end-point electrical parameters (method 5005) | 1 |

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the limits specified in table I.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Replaceability is determined as follows:

a. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

b. When a QPL source is established, the device specified in this drawing will be replaced by the microcircuit identified as PIN M38510/14005, 06BXX.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5375.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS.



Powered by ICminer.com Electronic-Library Service CopyRight 2003