PAL16R8-5/4 Series

5 ns TTL Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 5 ns and 4.5 ns maximum propagation delay
- f_{MAX} = 117 MHz
- 4 ns and 3.5 ns maximum from clock input to data output
- Popular 20-pin architectures: 16L8, 16R8, 16R6, 16R4
- Programmable replacement for high-speed TTL logic
- Register preload for testability
- Power-up reset for initialization
- Supported by popular industry standard design software
- Programmable on standard PAL® device programmers
- -5 version available in standard DIP and PLCC packages for compatibility with -7 version
- 28-pin PLCC -4 package provides ultra-clean high-speed signals

GENERAL DESCRIPTION

The PAL16R8-5/4 Series (PAL16L8-5/4, PAL16R8-5/4, PAL16R6-5/4, PAL16R4-5/4) are the fastest TTL PAL devices in the standard PAL16R8 Series. With 5 ns and 4.5 ns maximum propagation delay times, the PAL16R8-5/4 Series provides the highest speed in the 20-pin TTL PAL device family, making the series ideal for high-performance applications. The PAL16R8-5/4 Series is provided with standard 20-pin DIP and PLCC pinouts and a 28-pin PLCC pinout. The 28-pin PLCC pinout contains seven extra ground pins interleaved between the outputs to reduce noise and increase speed.

The family utilizes Advanced Micro Devices' advanced trench-isolated bipolar process and fuse-link technology. The devices provide user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at a reduced chip count.

The family allows the systems engineer to implement the design on-chip, by opening fuse links to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

The PAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs.

In addition, the PAL device provides the following options:

- Variable input/output pin ratio
- Programmable three-state outputs
- Registers with feedback

Product terms with all connections opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state. Registers consist of D-type flip-flops that are loaded on the LOW-to-HIGH transition of the clock. Unused input pins should be tied to Vcc or GND.

The entire PAL device family is supported by a variety of popular design software packages. The PAL family is programmed on conventional PAL device programmers with appropriate personality and socket adapter modules. See pages 20 and 21 for approved programmers and software. Once the PAL device is programmed and verified, an additional connection may be opened to prevent pattern readout. This feature secures proprietary circuits.

PRODUCT SELECTOR GUIDE

DEVICE	DEDICATED INPUTS	OUTPUTS	PRODUCT TERMS/ OUTPUT	FEEDBACK	ENABLE
PAL16L8	10	6 comb. 2 comb.	7 7	I/O –	prog. prog.
PAL16R8	8	8 reg.	8	reg.	pin
PAL16R6	8	6 reg. 2 comb.	8 7	reg. I/O	pin prog.
PAL16R4	8	4 reg. 4 comb.	8 7	reg. I/O	pin prog.

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PAL16L8

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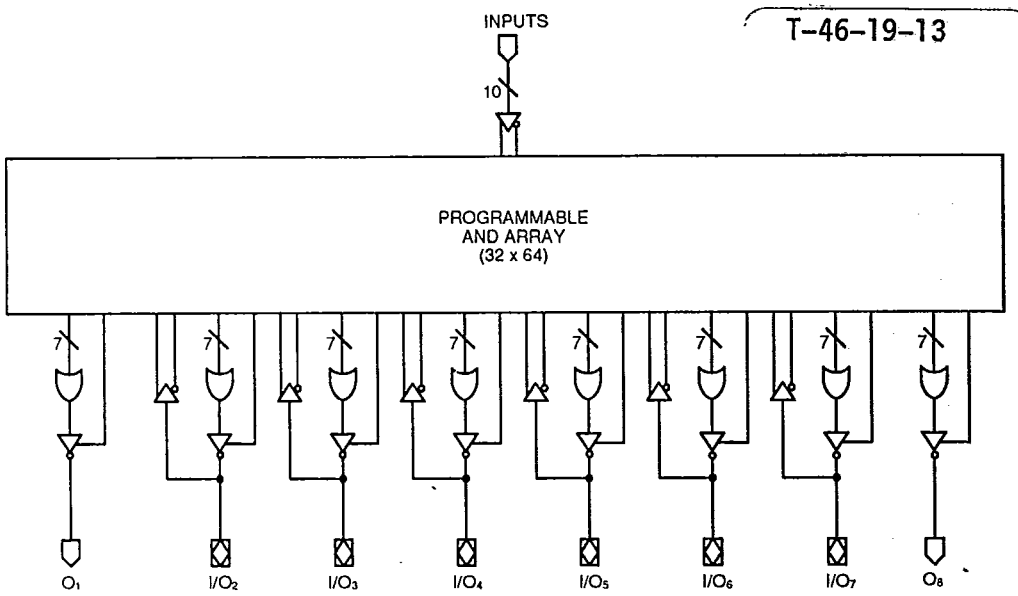

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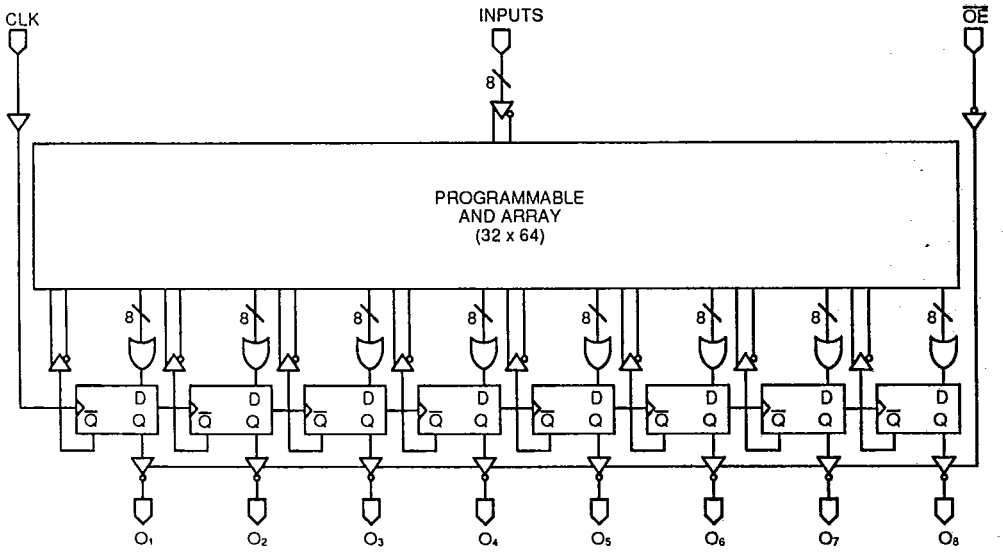
PAL16R8



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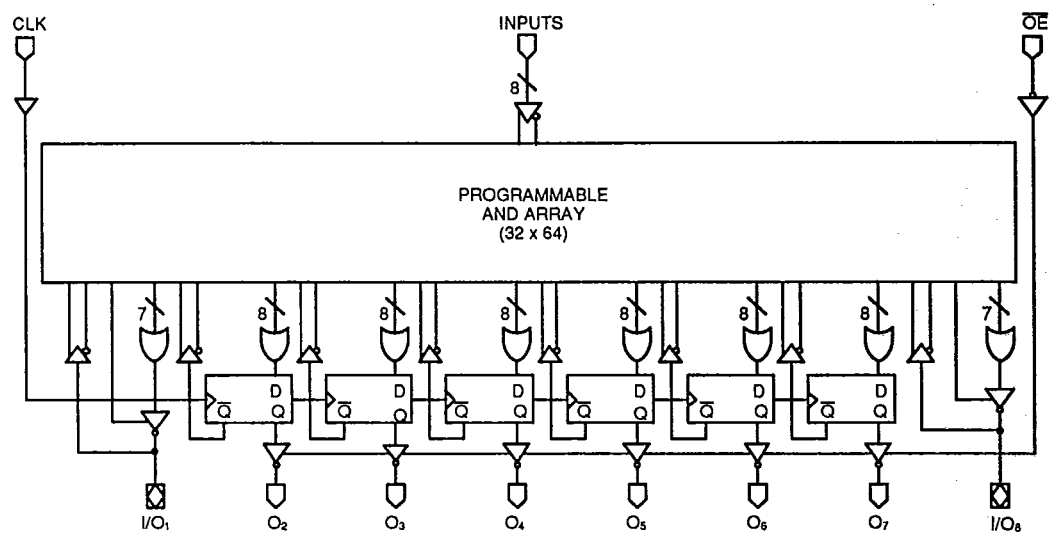
PAL16R6



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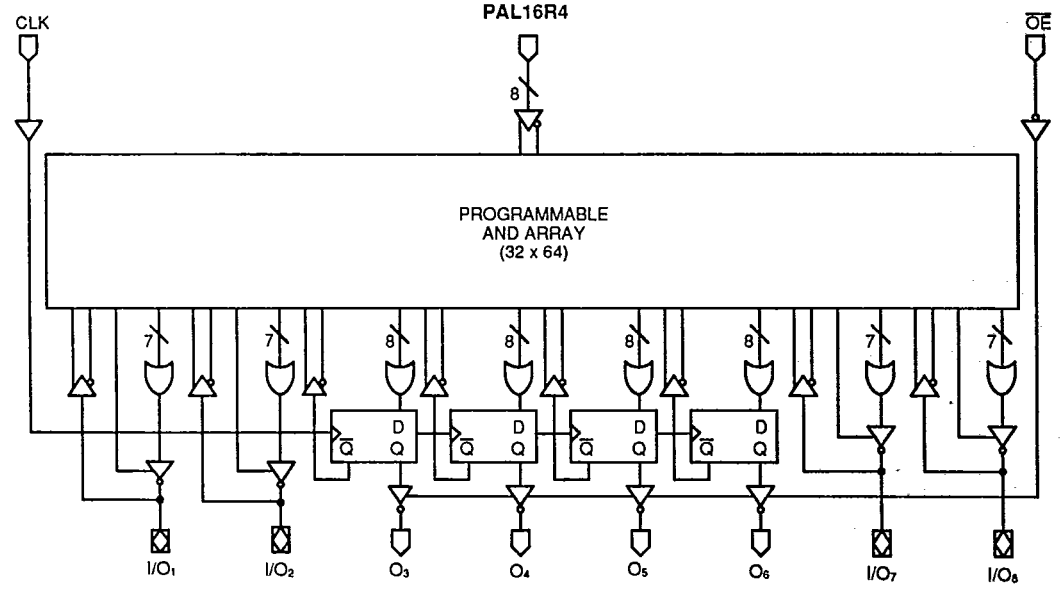
PAL16R4



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CONNECTION DIAGRAMS
Top View

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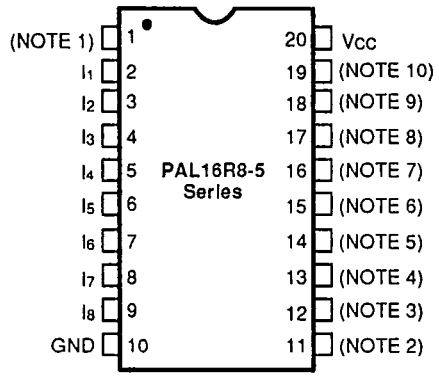
DIP



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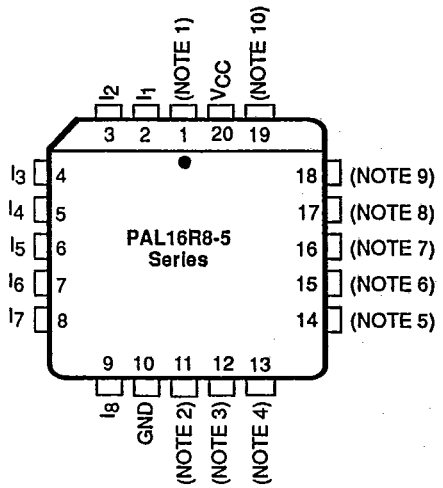
20-Pin PLCC



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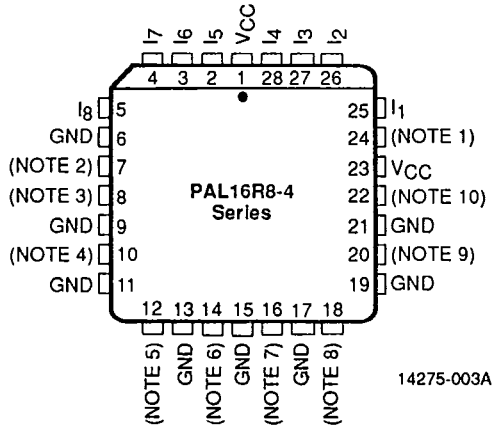
28-Pin PLCC



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PIN DESIGNATIONS

CLK	Clock
GND	Ground
I	Input
I/O	Input/Output
O	Output
$\overline{OE}$	Output Enable
Vcc	Supply Voltage

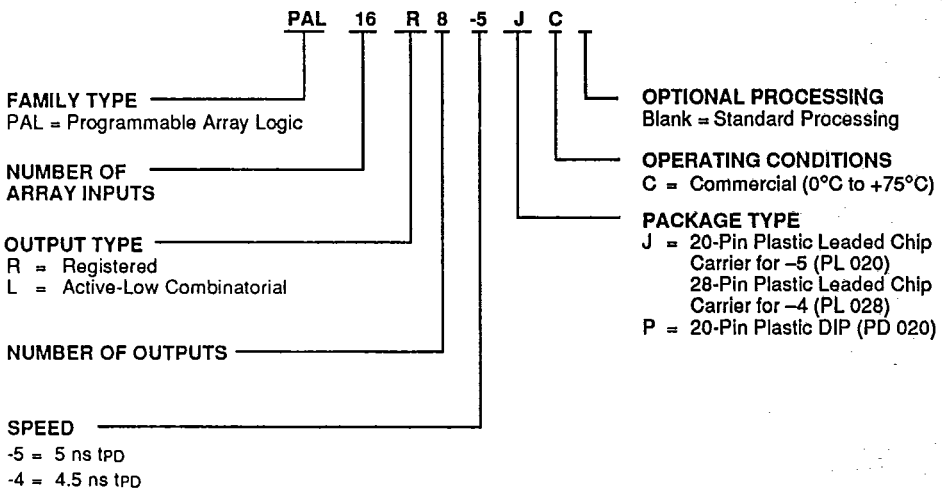
Note:
Pin 1 is marked for orientation.

Note	16L8	16R8	16R6	16R4
1	I_0	CLK	CLK	CLK
2	I_9	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
3	O_1	O_1	I/O_1	I/O_1
4	I/O_2	O_2	O_2	I/O_2
5	I/O_3	O_3	O_3	O_3
6	I/O_4	O_4	O_4	O_4
7	I/O_5	O_5	O_5	O_5
8	I/O_6	O_6	O_6	O_6
9	I/O_7	O_7	O_7	I/O_7
10	O_8	O_8	I/O_8	I/O_8

ORDERING INFORMATION (Preliminary)
Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of these elements:

Family Type
Number of Array Inputs
Output Type
Number of Outputs
Speed
Package Type
Operating Conditions
Optional Processing



Valid Combinations	
PAL16L8	-5PC, -5JC, -4JC
PAL16R8	
PAL16R6	
PAL16R4	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note:

Marked with AMD logo.

FUNCTIONAL DESCRIPTION

Standard 20-pin PAL Family

The standard bipolar 20-pin PAL family devices have common electrical characteristics and programming procedures. Four different devices are available, including both registered and combinatorial devices. All parts are produced with a fuse link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Utilizing an easily-implemented programming algorithm, these products can be rapidly programmed to any customized pattern. Information on approved programmers can be found on page 21. Extra test words are preprogrammed during manufacturing to ensure extremely high field programming yields, and provide extra test paths to achieve excellent parametric correlation.

Pinouts

The PAL16R8-5 Series is available in the standard 20-pin DIP and PLCC pinouts and the PAL16R8-4 Series is available in the new 28-pin PLCC pinout. The standard 20-pin pinouts allow the designer to utilize the PAL16R8-7 pinout while gaining the 5 ns delay. The 28-pin PLCC pinout gives the designer the cleanest possible signal with only 4.5 ns delay.

The PAL16R8-4 pinout has been designed to minimize the noise that can be generated by high-speed signals. Because of its inherently shorter leads, the PLCC package is the best package for use in high-speed designs. The short leads and multiple ground signals reduce the effective lead inductance, minimizing ground bounce. Placing the ground pins between the outputs optimizes the ground bounce protection, and also isolates the outputs from each other, eliminating cross-talk. This pinout can reduce the effective propagation delay by as much as 20% from a standard DIP pinout. Design files for PAL16R8-4 Series devices are written as if the device had a standard 20-pin DIP pinout for most design software packages.

Variable Input/Output Pin Ratio

The registered devices have eight dedicated input lines, and each combinatorial output is an I/O pin. The PAL16L8 has ten dedicated input lines and six of the eight combinatorial outputs are I/O pins. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to Vcc or GND.

Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. On combinatorial outputs, a product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin and may be configured as a dedicated input if the output buffer is always disabled. On registered outputs, an input pin controls the enabling of the three-state outputs.

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Registers with Feedback

Registered outputs are provided for data storage and synchronization. Registers are composed of D-type flip-flops that are loaded on the LOW-to-HIGH transition of the clock input.

Register Preload

The register on the PAL16R8-5/4 Series can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery. Details on register preload can be found on page 18.

Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the PAL16R8-5/4 Series will be HIGH due to the active-low outputs. The Vcc rise must be monotonic and the reset delay time is 1000 ns maximum. Details on power-up reset can be found on page 19.

Security Fuse

After programming and verification, a PAL16R8-5/4 Series design can be secured by programming the security fuse. Once programmed, this fuse defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security fuse is programmed, the array will read as if every fuse is programmed.

Quality and Testability

The PAL16R8-5/4 Series offers a very high level of built-in quality. Extra programmable fuses provide a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

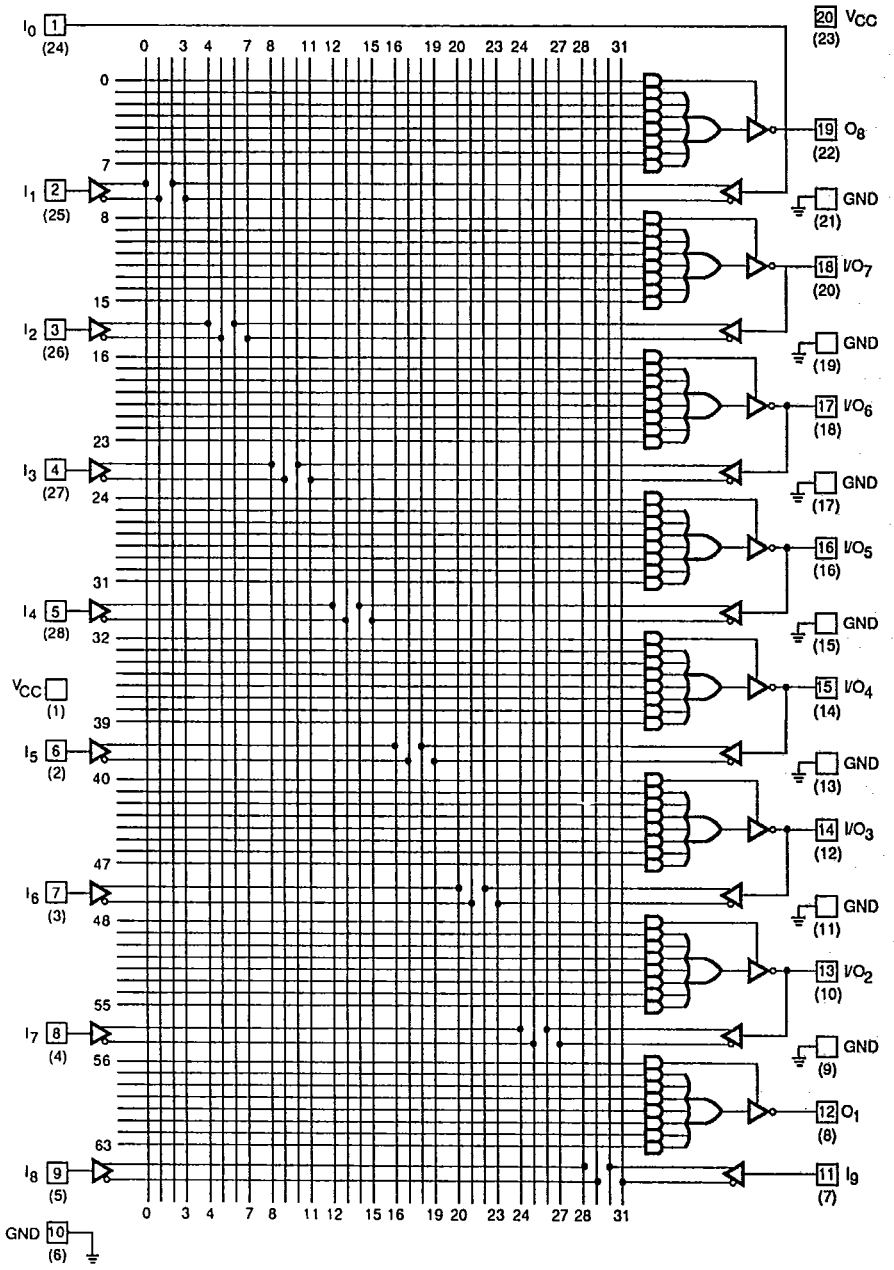
Technology

The PAL16R8-5/4 Series are fabricated with AMD's advanced trench-isolated bipolar process. This process reduces parasitic capacitances and minimum geometries to provide higher performance. The array connections are formed with proven TiW fuses for reliable operation.

LOGIC DIAGRAM

DIP and 20-Pin PLCC (28-Pin PLCC) Pinouts

16L8-5 (-4)



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LOGIC DIAGRAM

DIP and 20-Pin PLCC (28-Pin PLCC) Pinouts

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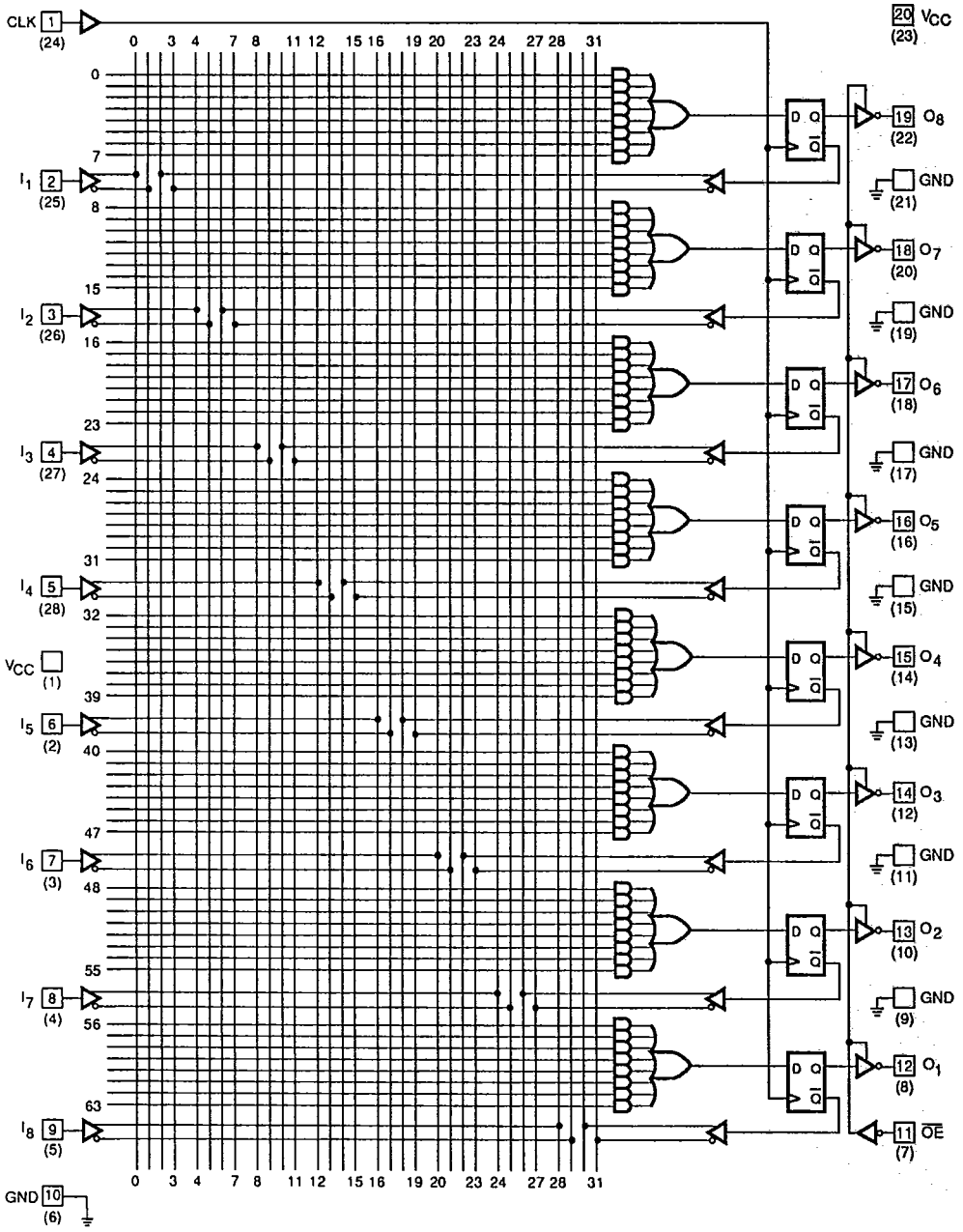
16R8-5 (-4)



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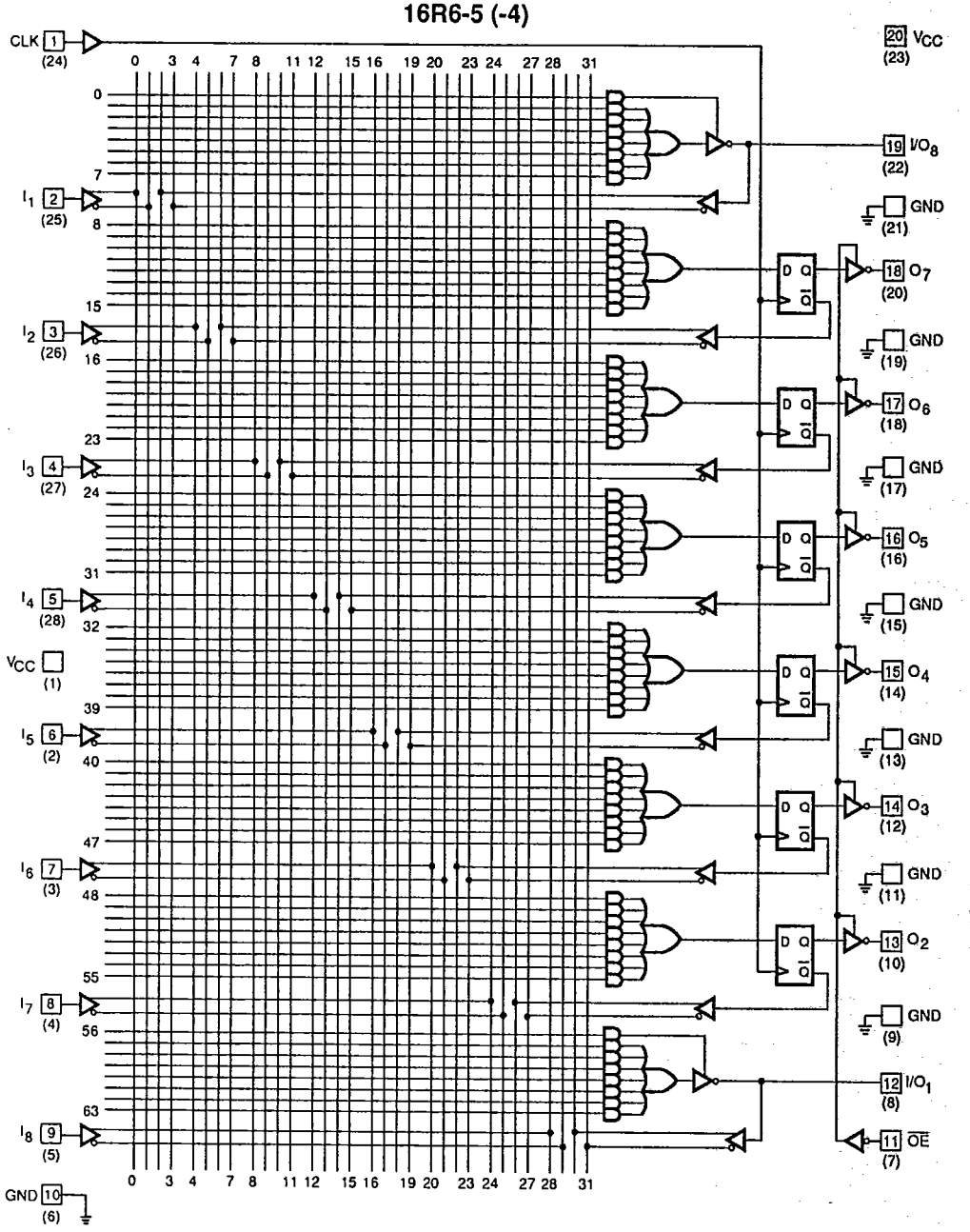
16R6-5 (-4)



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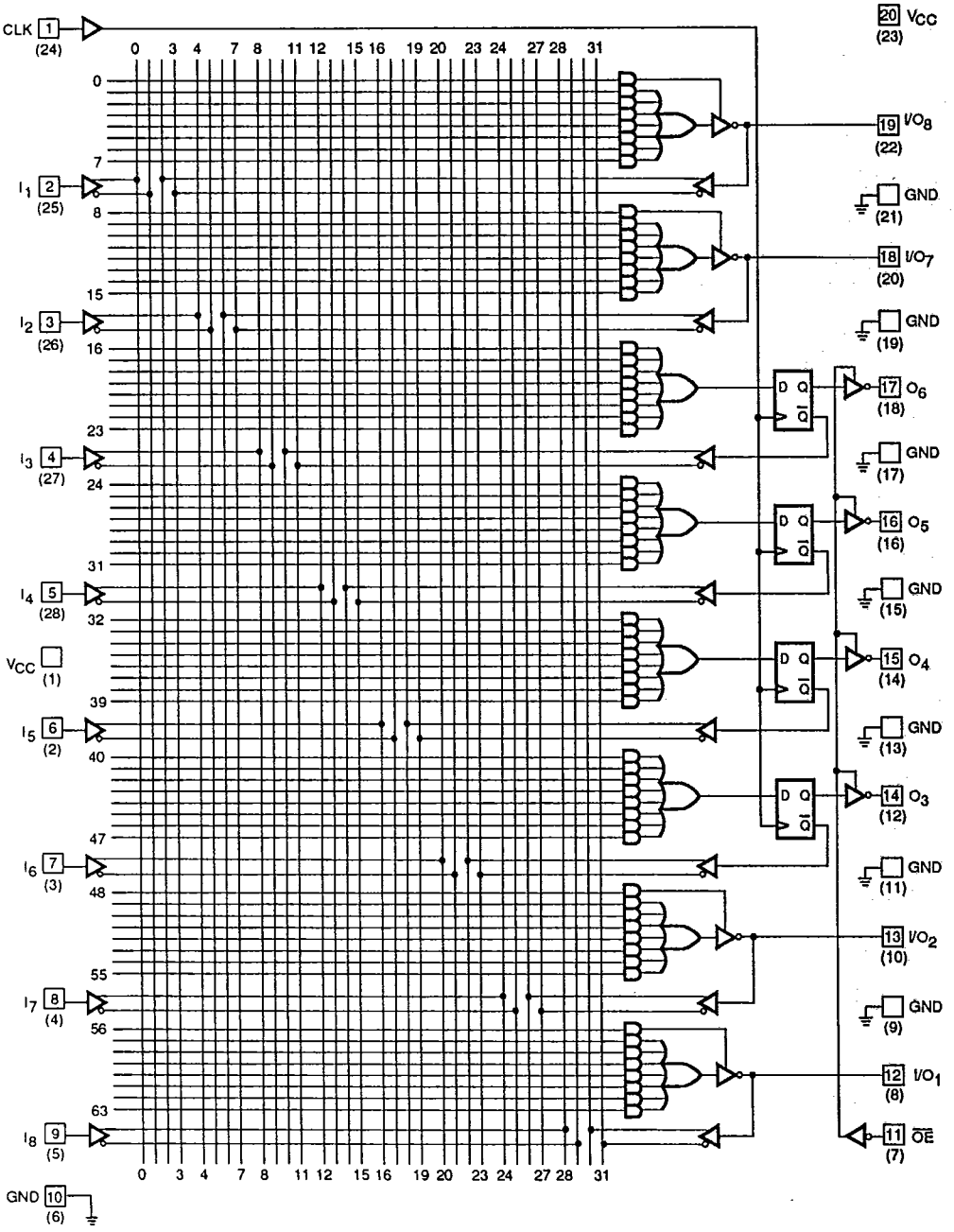
LOGIC DIAGRAM

T-46-19-13

DIP and 20-Pin PLCC (28-Pin PLCC) Pinouts

16R4-5 (-4)



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ABSOLUTE MAXIMUM RATINGS

Ambient Temperature with Power Applied	−65°C to +150°C
Storage Temperature	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−1.2 V to Vcc + 0.5 V
DC Input Current	−30 mA to +5 mA
DC Output or I/O Pin Voltage	−0.5 V to Vcc + 0.5 V
Static Discharge Voltage	2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (Vcc) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

PRELIMINARY

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −3.2 mA V_{IN} = V_{IH} or V_{IL} Vcc = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} Vcc = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = −18 mA, Vcc = Min.		−1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, Vcc = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, Vcc = Max. (Note 2)		−250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, Vcc = Max.		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, Vcc = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, Vcc = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		−100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, Vcc = Max. (Note 3)	−30	−130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) Vcc = Max.		210	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description		Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	CLK, $\overline{OE}$	V_{IN} = 2.0 V	V_{CC} = 5.0 V	8	pF
		I_1–I_8		T_A = 25°C	5	
C_{OUT}	Output Capacitance		V_{OUT} = 2.0 V	f = 1 MHz	8	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

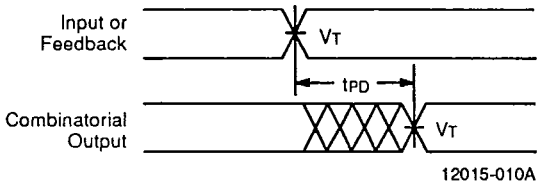
PRELIMINARY

Parameter Symbol	Parameter Description				-5 Min. (Note 3)	-5 Max.	-4 Min. (Note 3)	-4 Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			16L8, 16R8, 16R4	1	5	1	4.5	ns
t_S	Setup Time from Input or Feedback to Clock				4.5		4.5		ns
t_H	Hold Time				0		0		ns
t_{CO}	Clock to Output				1	4.0	1	3.5	ns
t_{SKEWR}	Skew Between Registered Outputs (Note 4)					1		0.5	ns
t_{WL}	Clock Width	LOW		16R8, 16R6, 16R4	4		4		ns
t_{WH}		HIGH			4		4		ns
f_{MAX}	Maximum Frequency (Note 5)	External Feedback	1/(ts + tco)		117		125		MHz
		Internal Feedback			125		125		MHz
		No Feedback	1/(t_{WH} + t_{WL})		125		125		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				1	6.5	1	6.5	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				1	5	1	5	ns
t_{EA}	Input to Output Enable Using Product Term Control			16L8, 16R6, 16R4	2	6.5	2	6.5	ns
t_{ER}	Input to Output Disable Using Product Term Control				2	5	2	5	ns

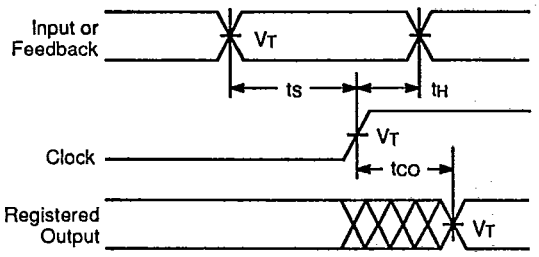
Notes:

2. See Switching Test Circuit for test conditions.
3. Delay minimums for t_{PD}, t_{CO}, t_{PZX}, t_{PXZ}, t_{EA}, and t_{ER} are chosen based on two considerations: they must allow for the large number of variables that define "best case" conditions, and they must attempt to anticipate possible future process enhancements that may increase performance. It is possible that such process improvements may someday push the minimum delays beyond what was originally anticipated; therefore minimums should be used with care, and are recommended primarily for simulation.
4. Skew testing takes into account pattern and switching direction differences between outputs.
5. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where the frequency may be affected.

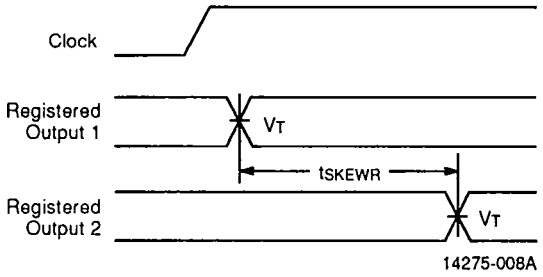
SWITCHING WAVEFORMS



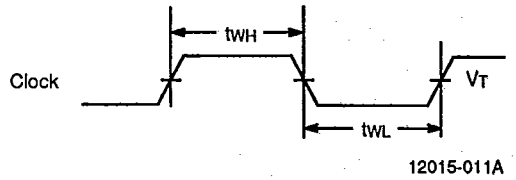
Combinatorial Output



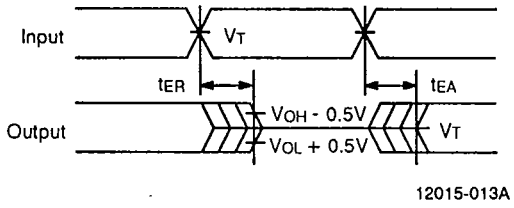
Registered Output



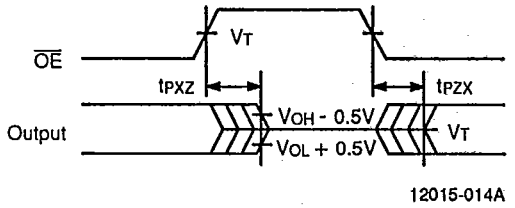
Registered Output Skew



Clock Width



Input to Output Disable/Enable



$\overline{OE}$ to Output Disable/Enable

Notes:

1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V
3. Input rise and fall times 2–3 ns typical.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

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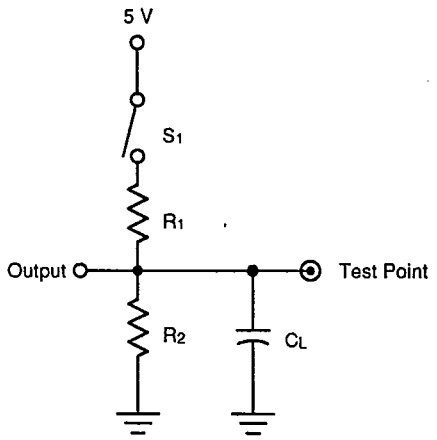
SWITCHING TEST CIRCUIT



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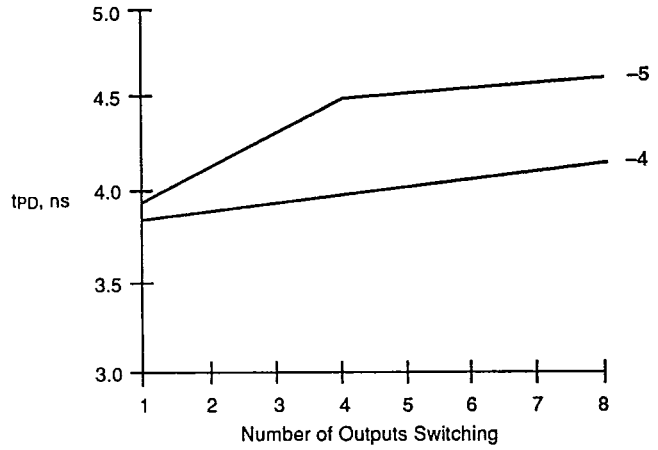
Specification	S_1	C_L	Commercial R_1	Commercial R_2	Measured Output Value
t_{PD}, t_{CO}	Closed	50 pF	200 Ω	200 Ω	1.5 V
t_{PZX}, t_{EA}	Z → H: Open Z → L: Closed				1.5 V
t_{PXZ}, t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} − 0.5 V L → Z: V_{OL} + 0.5 V

TYPICAL MEASURED SWITCHING CHARACTERISTICS (Note 1)



tPD vs. Number of Outputs Switching
VCC = 4.75 V, TA = 75°C

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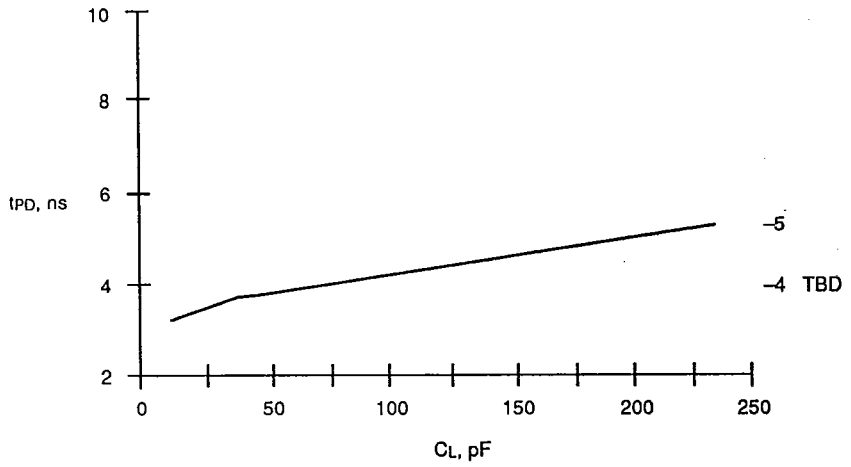

tPD vs. Load Capacitance
VCC = 5.25 V, TA = 25°C

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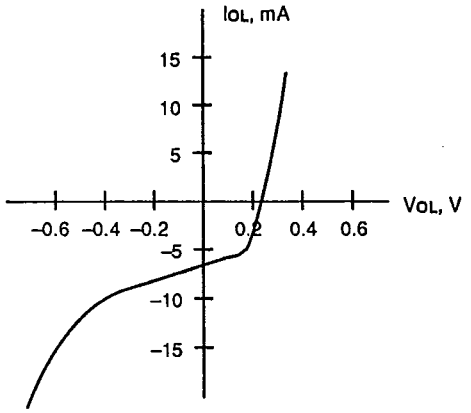
Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where tPD may be affected.

TYPICAL CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C



Output, LOW

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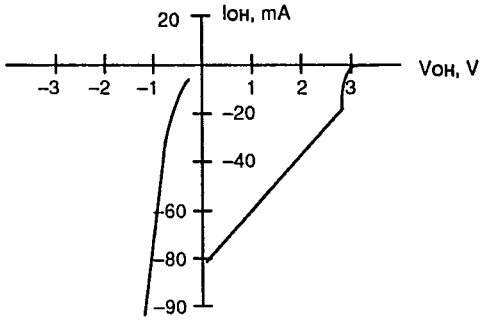
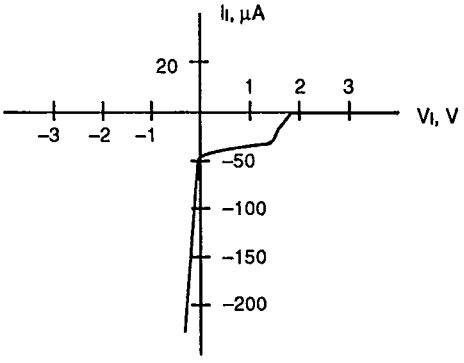


Output, HIGH

10240-004B



Input

10240-005A

f_{MAX} Parameters

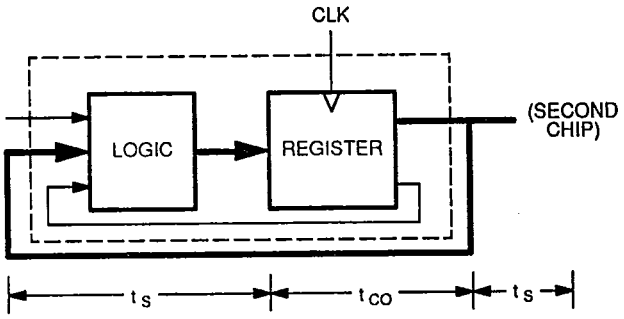
The parameter f_{MAX} is the maximum clock rate at which the device is guaranteed to operate. Because the flexibility inherent in programmable logic devices offers a choice of clocked flip-flop designs, f_{MAX} is specified for three types of synchronous designs.

The first type of design is a state machine with feedback signals sent off-chip. This external feedback could go back to the device inputs, or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the external signals ($t_S + t_{CO}$). The reciprocal, f_{MAX}, is the maximum frequency with external feedback or in conjunction with an equivalent speed device. This f_{MAX} is designated "f_{MAX} external".

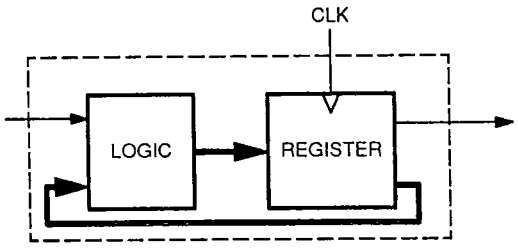
The second type of design is a single-chip state machine with internal feedback only. In this case, flip-flop inputs are defined by the device inputs and flip-flop outputs. Under these conditions, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic to the flip-flop inputs. This f_{MAX} is designated "f_{MAX} internal".

The third type of design is a simple data path application. In this case, input data is presented to the flip-flop and clocked through; no feedback is employed. Under these conditions, the period is limited by the sum of the data setup time and the data hold time ($t_S + t_H$). However, a lower limit for the period of each f_{MAX} type is the minimum clock period ($t_{WH} + t_{WL}$). Usually, this minimum clock period determines the period for the third f_{MAX}, designated "f_{MAX} no feedback".

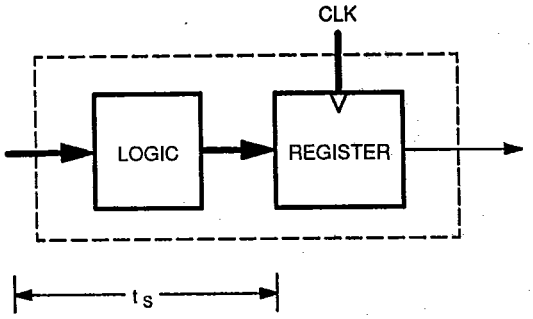
All frequencies except f_{MAX} internal are calculated from other measured AC parameters. f_{MAX} internal is measured directly.



f_{MAX} External; $1/(t_S + t_{CO})$



f_{MAX} Internal

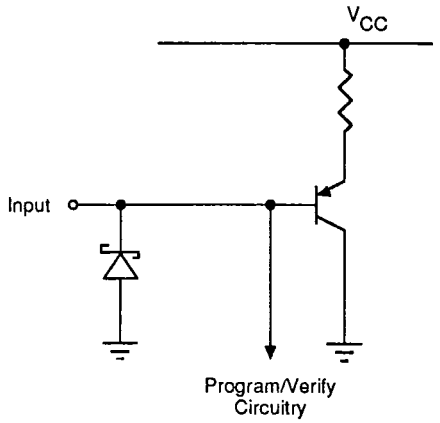


f_{MAX} No Feedback; $1/(t_S + t_H)$ or $1/(t_{WH} + t_{WL})$

12350-022A

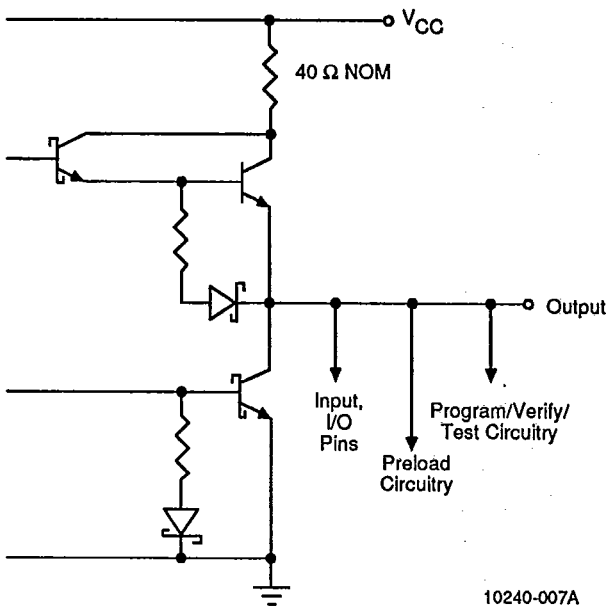
INPUT/OUTPUT EQUIVALENT SCHEMATICS

Typical Input



10240-006A

Typical Output



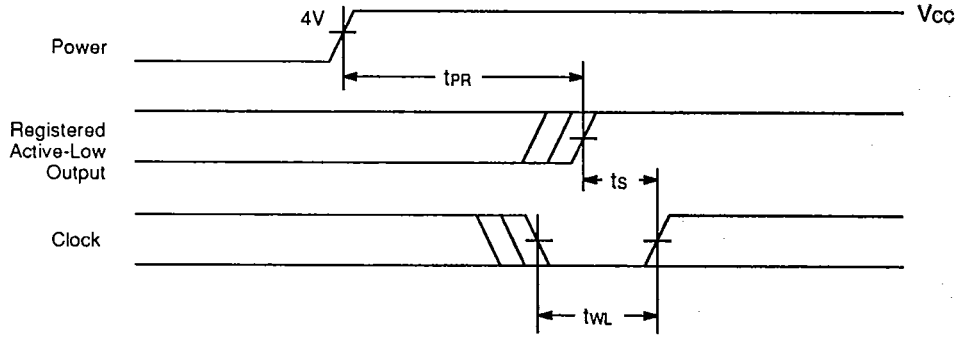
10240-007A

POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will be HIGH due to the inverting output buffer. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways Vcc can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The Vcc rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max.	Unit
t_{PR}	Power-up Reset Time	1000	ns
ts	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



12350-024A

Power-Up Reset Waveform

APPROVED PROGRAMMERS (subject to change)

Manufacturer	Programmer Configuration
Advanced Micro Devices, Inc. 901 Thompson Place MS 1028 Sunnyvale, CA 94088-3543 (800) 222-9323 or (408) 732-2400	LabPro Rev. 1.2 (Note 1)
BP Microsystems 10681 Haddington, Suite #190 Houston, TX 77043 (800) 225-2102 or (713) 461-9430	Model CP-1128 Rev. 1.55 (Note 1)
Data I/O Corporation 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 247-5700 or (206) 881-6444	UniSite™ Rev. 3.4 Family/Pinout Code: 16L8 20–17 16R4 20–81 16R6 20–80 16R8 20–82
Digelec Inc. 20144 Plummer St. Chatsworthy, CA 91311 (800) 367-8750 or (818) 701–9677 or 25 Galgaley Haplada St. Herzliya B46722, Israel 52-55-9615	Contact Manufacturer
Encore Technology, Inc. 13720 Midway Suite 105 Dallas, TX 75244 (800) 688-3122 or (214) 233-3122 or SMS Im Morgental 13 D-8994 Hergatz, Germany 07522-5018	Contact Manufacturer
JMC Hakusan High-Tech Park 807-1, Hakusan-Cho, Midori-Ku Yokohama-City 226, Japan 045/393-6150	Contact Manufacturer
Kontron Electronics Inc. Breslauer Str. 1 D-8057 Eching, Munich, Germany 8165-770	Contact Manufacturer
Logical Devices Inc. 1201 E. Northwest 65th Pl. Fort Lauderdale, FL 33309 (800) 331-7766 or (305) 491-7405	Contact Manufacturer
Micropross Parc d'Activite des Pres 5, rue Denis-Papin 59650 Villeneuve-d'Ascq, France (20) 47.90.40	Contact Manufacturer

Note:

1. –4 requires socket adapter.

APPROVED PROGRAMMERS (Continued)

Manufacturer	Programmer Configuration
Stag Microsystems, Inc. 1600 Wyatt Dr. Suite 3 Santa Clara, CA 95054 (408) 988-1118 or Stag House Martinfield, Welwyn Garden City Herfordshire UK AL7 1JT 707-332148	Contact Manufacturer
Systems General 244 S. Hillview Dr. Milpitas, CA 95035 (408) 236-6667 or 3F, No. 1, Alley 8, Lane 45 Bao Shing Rd., Shin Diau Taipei, Taiwan 2-917-3005	Contact Manufacturer

PROGRAMMER SOCKET ADAPTERS (subject to change)

Manufacturer	Programmer Configuration
Emulation Technology 2344 Walsh Ave. Bldg. F Santa Clara, CA 95051 (408) 982-0660	282003P300

DEVELOPMENT SYSTEMS (subject to change)

MANUFACTURER	SOFTWARE DEVELOPMENT SYSTEM
Advanced Micro Devices, Inc. P.O. Box 3453 901 Thompson Place MS 1028 Sunnyvale, CA 94088-3543 (800) 222-9323 or (408) 732-2400	PALASM® Software
Data I/O Corporation 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 247-5700 or (206) 881-6444	ABEL™ Software
ISDATA GmbH Haid-und-Neu-Str. 7 D-7500 Karlsruhe 1, West Germany 0721/69 30 92 or (408) 373-7359 in U.S.	LOG/iC™ Software
Logical Devices Inc. 1201 E. Northwest 65th Pl. Fort Lauderdale, FL 33309 (800) 331-7766 or (305) 491-7405	CUPL™ Software
MINC Inc. 6755 Earl Drive, Suite 200 Colorado Springs, CO 80918 (719) 590-1155	PLDesigner™ Software
OrCAD Systems Corporation 1049 S.W. Baseline St. Suite 500 Hillsboro, OR 97123 (503) 640-9488	OrCAD/PLD™ Software
MANUFACTURER	**TEST GENERATION SYSTEM**
Acugen Software, Inc. 427-3 Amherst St., Suite 391 Nashua, NH 03063 (603) 891-1995	Acugen (Anvil) ATG™ Software
Data I/O Corporation 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 247-5700 or (206) 881-6444	PLDtest™ Software

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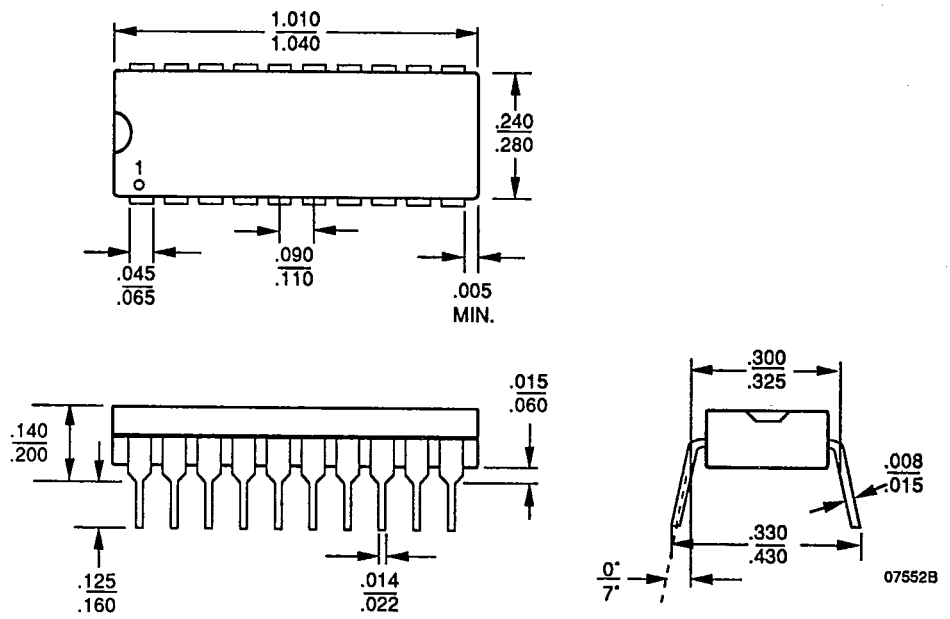
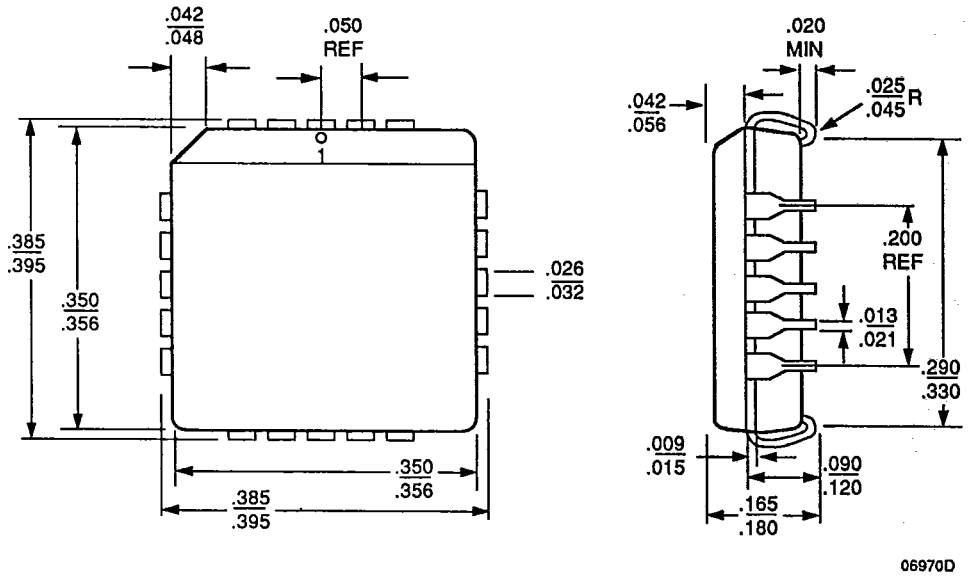
Test Generator is a trademark of ATG Associates.

PHYSICAL DIMENSIONS*
PD 020
20-Pin Plastic DIP



PL 020
20-Pin Plastic Leaded Chip Carrier



*For reference only. All dimensions measured in inches., unless otherwise noted. BSC is an ANSI standard for Basic Space Centering.

PHYSICAL DIMENSIONS*

PL 028

28-Pin Plastic Leaded Chip Carrier