T-52-13-90

GigaBit Logic **16G061A**

Dual High Speed Pin Driver
800 MHz Operating Frequency

FEATURES

- DC to 800 MHz minimum operating frequency range
- Variable output voltages for ECL, TTL, and CMOS
- 250 ps output rise and fall times (ECL/GaAs)
- 300 ps output rise and fall times for up to 5 Vp-p (10% to 90%)
- Adjustable output edge rate from 250 ps to 2000 ps
- Programmable output voltages up to 6.5 Vp-p over -2.5V to +6.5V range
- 100 mA output current drive capability
- High impedance, three state output control
- High speed ECL/GaAs compatible differential inputs
- On chip VBBS (-1.2V) reference voltage
- Available in 40-pin C-leaded or leadless chip carriers or in die form. Packages contain internal decoupling capacitors for optimum high frequency performance
- Packaged parts available in 50Ω series terminated or unterminated (Rs=8Ω) configurations

APPLICATIONS

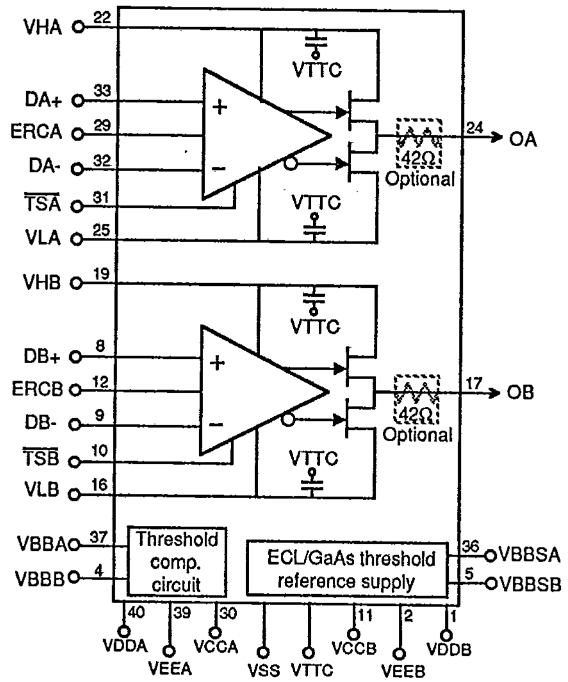
- ATE pin driver
- Differential line receiver
- Precision pulse generator
- Level comparator/translator
- Laser driver
- Switch driver
- General purpose driver
- CRT preamplifier

PRODUCT DESCRIPTION

The 16G061A is a dual pin driver designed for use in very high speed GaAs/ECL as well as TTL/CMOS logic test systems. The A and B drivers of the 16G061A are electrically independent and have separate power supplies. Under control of the differential inputs, the output is switched between the levels provided on the VH (V High) and VL (V Low) inputs. The differential inputs can be driven with ECL or GaAs levels. The 16G061A has an on-chip threshold voltage generator (VBBS). When VBBS is connected to the D- inputs, the D+ inputs of the 16G061A can be driven single-ended. The V High output level is adjustable from -1.1V to +6.5V and the V Low output level can be adjusted from -2.5V to +1.5V. The output amplitude extends to 6.5Vp-p. Controls are provided ($\overline{TSA}$, $\overline{TSB}$) to force the outputs into a high impedance, three-state condition.

The 16G061A features a continuously variable Edge Rate Control (ERCA and ERCB) to vary the output rise and fall times. Rise and fall times are typically 250 ps for a 1V peak to peak output (GaAs/ECL) and 300 ps for a 5V peak to peak output when Edge Rate Control (ERC) is biased at VSS. This translates to a slew rate of 4V/ns for a 1V output and 17V/ns for a 5V output. Rise and fall times can be increased to 2ns typically for a 5Vp-p output by connecting ERC to VEE. This translates to a slew rate of 2.5V/ns for a 5V output. Between -5.1V and -4.8V the Edge Rate Control varies the edge rate at approximately 2 ps/mV for an ECL output swing and 3.5 ps/mV for a TTL output swing. Propagation delays (typ.) are 700ps for fast edge rate levels and, for slow edge rate levels, 1.5 ns.

BLOCK DIAGRAM



16G061A ORDERING INFORMATION

Package	Speed (Min. 25°C to 85°C): 800 MHz Unterminated	50Ω Terminated*	
40-pin LDCC	16G061A-2UC	16G061A-2TC	*Option T: 42Ω series resistor in the package: Rs=42+8=50Ω
40-pin LCC	16G061A-2UL	16G061A-2TL	
Die	16G061A-2X		

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ABSOLUTE MAXIMUM RATINGS

(Beyond which useful life may be impaired) (Notes 1, 4)

SYMBOL	PARAMETER	ABSOLUTE MAXIMUM RATINGS	NOTES
TSTOR	Storage Temperature	-65 °C to +150 °C	
TJ	Junction Temperature	-55 °C to +150 °C	
TC	Case Temperature Under Bias	-55 °C to +125 °C	2
VDD	Output Driver Gnd Supply	VSS to +1.0 V	
VSS	Supply Voltage	-4.0 V to +0.5 V	
VEE	Supply Voltage	-7.0 V to VSS + 0.5 V	
VCC	Supply Voltage	+0.5 V to +10.0V	
VIN	Voltage Applied to Any Input; Continuous VSS = -3.4 V, VEE = -5.2 V	-4.0 V to +0.5 V	
I IN	Current Into Any Input; Continuous	-0.5 mA to 1.0 mA	
VOUT	Voltage Applied to Any Output	VL-0.5V to VH + 0.5	3,5
IOUT	Current From Any Output; Continuous	-150 mA	
PD	Power Dissipation Per Output POUT = (VDDO-VOUT) x IOUT	100 mW	
VBB	Threshold Reference Input Voltage	-4.0V to +0.5V	
IBB	Input current (from interfacing family)	-0.5 mA to +1.0 mA	
VTTC	VH/VL Internal Decoupling Cap. Return	-6.0 V to VL	
VTT	Load Termination Supply	-6.0 V to VDD + 6.0 V	
VH-VL	Output Voltage Amplitude	9V	

Notes:
1. All voltages specified with VDD defined as Gnd. Positive current is defined as current into the device.
2. TC is measured at case top.
3. Subject to IOUT and power dissipation limitations.
4. Power supply sequencing is not necessary, but since the VEE supply is used to bias off the normally-on depletion mode transistors, sustained (>5 secs.) application of VSS in the absence of VEE may result in excessive power dissipation and damage to the device.
5. Voltage applied through a 42Ω series resistor.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
TC	Case operating temperature	25		85	°C	1
VDD	Supply voltage		Gnd		V	
VCC	Supply voltage	+4.5	VH + 2	7.5	V	
VSS	Supply voltage	-3.5	-3.4	-3.3	V	
VEE	Supply voltage	-5.5	-5.2	-5.1	V	
VTT	Load termination supply voltage	VSS	-2.0	-2.0	V	2
VTTC	VH & VL internal decoupling return		DUT GND		V	TTL,CMOS
			DUT VTT		V	ECL,GaAs
VH	High level set voltage	-1.1	VCC-2.0	VCC-1.0	V	
VL	Low level set voltage	-2.5		1.5	V	
VH - VL	Output voltage amplitude	0		6.5	V	3
Rseries	Series termination output resistance	44	42	40	Ω	4
Rload	Output termination load resistance	25	50	100	Ω	2

Notes:
1. Tcase measured at case top. **User attention to device thermal management is recommended.** See GigaBit Application Note 3, "Thermal Management of PicoLogic and NanoRam GaAs Digital IC Families" for a complete discussion of all aspects of device thermal management. Heatsinks are available from GigaBit.
2. For shunt termination
3. For series terminations. For shunt termination: Voh = VH x [Rt/(Rt+Ron)] ; Vol = VL x [Rt/(Rt+Ron)] ; Rt: termination resistance.
4. For series termination.

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DC CHARACTERISTICS (Note 1)

Tc = 25°C to 85°C, VSS = -3.3V to -3.5V, VEE = -5.1V to -5.5V, VCC = 5.0V (ECL) or 7.0V (TTL), VDD = Gnd

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	NOTES
Vih	Input voltage high	- 1.0		Vdd	V		
Vil	Input voltage low	VSS		- 1.6	V		
Vcm	Common mode Vin	-1.9	VBB	- 0.5	V		
Iin	Input current	- 500		500	µA	Vin = -0.5V to -1.9V	3
Iin-3	Input current (TSx input)		500	1000	µA		
Iin-vbb	Input current (VBB input)		500	1000	µA		
Voffset	Input offset voltage		50		mV		
Ioh	Output drive current		±100		mA		2
Voh	Output voltage high	VH - .02	VH	VH	V	No DC load, VH-VL≤6.5V	
Vol	Output voltage low	VL	VL	VL + .02	V	No DC load, VH-VL≤6.5V	
Izl	Three state output leakage			±50	µA	VL = -0.4V, VH = 2.7V	
Ron	Driver FET on rest.	6.5	8	9.5	Ω	At Voh, Vol	
VBBS	Threshold Ref. voltage (ECL/GaAs)	-1.05	- 1.2	-1.4	V		
IL	VL supply current		65	80	mA	No output load	4
ICC	Supply current		120	140	mA		4
IEE	Supply current		180	220	mA		4
ISS	Supply current		65	80	mA		4
PdE	Power dissipation		1.8	2.2	W	VCC = 5.0V (ECL)	
PdT	Power dissipation		2.0	2.4	W	VCC = 7.0V (TTL)	

Notes:
1. Test conditions unless otherwise indicated: -D input = -1.20V.
2. Test Conditions: VH - Vout ≥ 1V; VL - Vout ≤ - 1.0V.
3. Source impedance = 40Ω nominally. ΔVBBS/ΔTemp. = +0.6mV/°C; ΔVBBS/ΔVSS = +0.2mV/mV.
4. Measured at nominal supply voltages, 50% output duty cycle and with both drivers powered.

AC CHARACTERISTICS (Note 1, 2)

Tc = 25°C to 85°C, VSS = -3.3V to -3.5V, VEE = -5.1V to -5.5V, VCC = 5.0V (ECL) or 7.0V (TTL), VDD = Gnd

		ECL/GaAs Output Levels			TTL Output Levels				
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	NOTES
Fmax	Maximum operating frequency	800	1000		300	500		MHz	
td	Propagation delay		700	1000		700	1000	ps	4
tds	Prop. delay, slow edge rates		1500	2000		1500	2000	ps	5
td3	3-state delay		750	1000		850	1000	ps	4
td3s	3-state delay, slow edge rates		1500	2000		1500	2000	ps	5
Δtdm	Prop. delay match; H-L, L-H		100	150		100	250	ps	4
Δtdms	Prop.delay match,slow mode		300	400		300	600	ps	5
Δtd/Δdc	Δ Prop. delay with duty cycle		200	300		200	500	ps	4 or 5
Δtd/ΔT	Prop. delay temp. coeff.		± 1.0	±2.0		± 1.0	±2.0	ps/°C	4 or 5
T	Output slew rate	2.9	4		10	17		V/ns	4
Tr,f	Output rise and fall times		250	350		300	500	ps	3,4
Ts	Slow Output slew rate	0.4	0.7		1.7	2.5		V/ns	5
Tsr,sf	Slow Output rise and fall times		1500	2500		2000	3000	ps	3,5
Tset	Settling time to 0.05 (Voh - Vol)		0.5	1.0		0.5	1.0	ns	
W	Output crosstalk			(0.05) x (Voh-Vol)			(0.05) x (Voh-Vol)	V	@ 100 MHz

Notes:
1. Test Conditions (unless otherwise indicated): VBB = -1.2V, Vih = -1.0V, Vil = -1.6V. Input signal rise and fall times ≤200 ps.
2. ECL Vp-p output = 1.0V; TTL Vp-p output = 5.0V.
3. Output rise and fall times are measured at 10% and 90% points. 20% to 80% rise and fall times for ECL/GaAs levels are 175 ps typ. and for TTL levels 200 ps typ.
4. ERC = VSS
5. ERC = VEE

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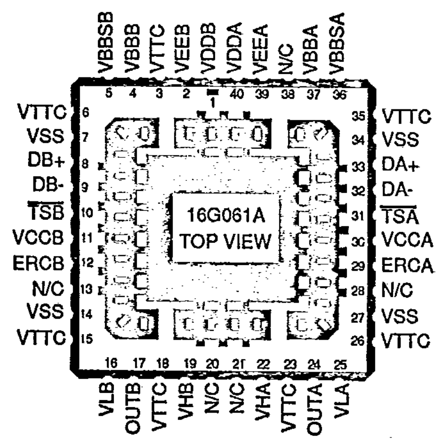
PIN DESCRIPTIONS

DA+, DA-	Differential data inputs A. (ECL/GaAs levels)
DB+, DB-	Differential data inputs B. (ECL/GaAs levels)
OA, OB	Output A, Output B.
VLA, VLB	Output Low level set voltages.
VHA, VHB	Output High level set voltages.
$\overline{TSA}$, $\overline{TSB}$	Three-State output controls. Output, OA or OB, is forced into a high impedance condition when $\overline{TSA}$ or $\overline{TSB}$ respectively is low. (ECL/GaAs levels).
ERCA, ERCB	Edge Rate Controls. Output Edge rates are continuously slowed when ERC is moved from VSS to VEE. Fast edge rates are obtained when ERC is tied to VSS. Slow edge rates are obtained when ERC is tied to VEE.
VDDA, VDDB	Ground Pins (0V).
VSS	- 3.4V power supplies.
VEEA, VEEB	-5.2V power supplies.
VCCA, VCCB	Positive power supplies. Nominally VH + 2V.
VTTC	AC return pin for the package internal decoupling capacitors tied to VH (VHigh) and VL (VLow) pins. VTTC may be either positive or negative with respect to VH and VL. When driving TTL/CMOS levels, VTTC = DUT ground is appropriate. When driving ECL/GaAs levels, VTTC should be connected to the DUT output termination voltage (DUT VTT). Connecting VTTC to the termination voltage associated with the 16G061A input signal may couple noise to the output.
VBBA, VBBB	Reference input to the 10G061A's input threshold compensation circuit. Connect to the VBB supplied from ECL when driving from ECL. Otherwise connect to corresponding VBBS pin.
VBBSA, VBBSB	PicoLogic Threshold reference output voltage. Connect to VBB when driving from PicoLogic™ Δ VBBS/Δ Temp = 0.6mV/°C, Δ VBBS/ΔVSS = 0.2 mV/mV.

40-PIN LEADLESS (TYPE L) OR C-LEADED (TYPE C) CHIP CARRIER



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FUNCTIONAL DESCRIPTION

The 16G061A pin driver contains two identical drivers which provide programmable output levels controlled by differential ECL inputs. Although this part was originally conceived for the purpose of driving integrated circuits in ATE systems, it has also found applications as analog switch driver, level comparator/translator, precision pulse generator and differential line receiver. Careful adherence to the following application information will maximize waveform fidelity.

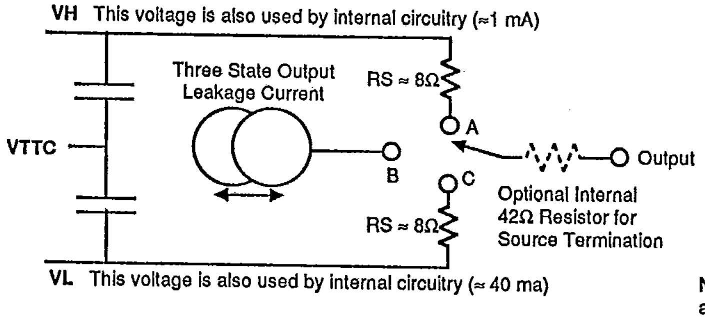
Input Circuit Description and Discussion

The 16G061A input structure is a differential input similar in nature to that found in several standard PicoLogic™ products such as the 10G010, 10G002 and 10G012B. Although the differential structure will operate over common mode range of approximately -0.5V to -1.9V, timing of the output waveform will more precisely adhere to that of the input if the inputs are maintained at ECL (or PicoLogic™) levels. The input may be driven from a single ended signal, but differential drive will effectively double the gain of the input stage, better establish the input threshold, and minimize output transient noise induced by input switching.

Any input circuit will have some input threshold uncertainty, even when differentially driven. This will translate from the voltage domain to the output time domain proportionally to the input signal rise and fall times around the threshold region. For this reason, it is important to have input signals as sharp as possible, thus favoring PicoLogic™ drive to ECL drive for critical applications. In all cases, the VBB should be externally supplied as the midpoint between VOH and VOL of the driving circuit (VBB = (VINH + VINL)/2. This same signal should also be applied to the unused input if the part is driven from a single ended source. The internal VBBS provided, should only be used with this device when precision of the output waveform is not critical.

Since the inputs are presumably derived from either ECL (emitter follower output) or GaAs (source follower output), a resistor pull down is required. Additionally, in order to meet electromagnetic requirements, **the input signals should be shunt terminated to the VTT supply used by the source logic not to the VTTC pin on the part, or be connected in the series** termination mode.

FIGURE 1.
SIMPLIFIED DIAGRAM OF OUTPUT
(Neglecting ERC)



Switch Position controlled by D+ and D- and TS

Inputs	$\overline{TS}$	Output
D+ > D-	High	A
Don't Care	Low	B
D+ < D-	High	C

Note: External unity gain amplifiers such as the LM324 or higher current operational amplifiers such as the LM759 can be used to buffer the VHigh (VH) and the VLow (VL) inputs when driven by DACs.

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FUNCTIONAL DESCRIPTION (CONTINUED)

Output Circuit Description

The output circuit is the key to the operation of this circuit. It may be represented by the simplified diagram on Figure 1 which ignores Edge Rate Control. The three position switch will be in the center (B) position independent of the state of IN+ or IN- if the three state input is low. If the three state input is high, the inputs IN+ and IN- control the state of the switch. When IN+ is more positive than IN-, the switch will be in the "A" position; when more negative, in the "C" position.

Since the output transistors appear as an 8Ω resistor, the addition of a 42 Ω chip resistor in series is required for driving a 50Ω unterminated transmission line. The output will be connected to the indicated rail and will supply whatever voltage appears at that rail. The circuitry driving the gates of the these output transistors consists of quite complex drivers. Clamping circuits are required to assure that breakdown voltages are not exceeded, that the edge rate control (ERC) can actually control the slew rate of the output, and to minimize any leakage currents on the outputs when they are in either the active or three state mode. Due to this complexity it is necessary that VH be maintained more positive than VL for proper functionality. The VH and VL supplies are also used to provide some biasing of the driver circuitry, hence VH and VL currents will be somewhat greater than the current supplied to the load.

Output Signal Accuracy

It should be noted that the output transistors are symmetrical, i.e. each transistor can both sink and source current. The 16G061A output circuit works much like the simplified block diagram of Figure 1. If the output of this circuit is required to sink or source additional current due either to the input impedance of the device being driven or a termination resistor to any potential, the output signal VOH and VOL levels will be altered due to this additional current being supplied through the 8Ω resistor. This may be best explained by an example terminating the output to -2V as in an ECL shunt terminated case (See Figure 2).

A correction factor must then be applied to correct VH and VL which can be readily calculated by the processor setting VH and VL via DACs. The following equations give VH' and VL', the corrected voltages which must be applied to the VH and VL pins in the case where the pin driver drives a DC load.

Let ρ (the resistor divide ratio) = RS/(RS + RL):
VH' = (VOH - ρVTT)/(1 - ρ)
VL' = (VOL - VTTρ)/(1 - ρ)

Note that if the termination resistor goes to ground (VTT = 0) then VH' = VOH/ (1 - ρ). The RS tolerance of typically ± 10% and variation over voltage and temperature will introduce an additional error. Self calibration techniques are therefore required to yield more accurate VOH and VOL levels.

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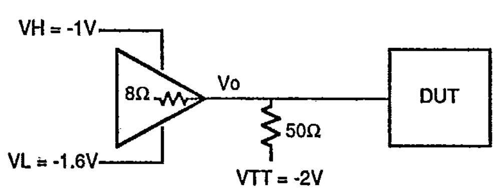
FIGURE 2

VOH = [VTT-VH][RS/(RS+RL)] + VH = -1.1379

Similarly VOL may be calculated as

VOL = [VTT-VL][RS/(RS+RL)] + VL = -1.6552



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GigaBit Logic **16G061A**

FUNCTIONAL DESCRIPTION (CONTINUED)

Dynamic Considerations

Since, typically, signals used with the 16G061A have edge rates exceeding in some cases 10,000 V/µs, special precautions must be observed as follows:

Terminations

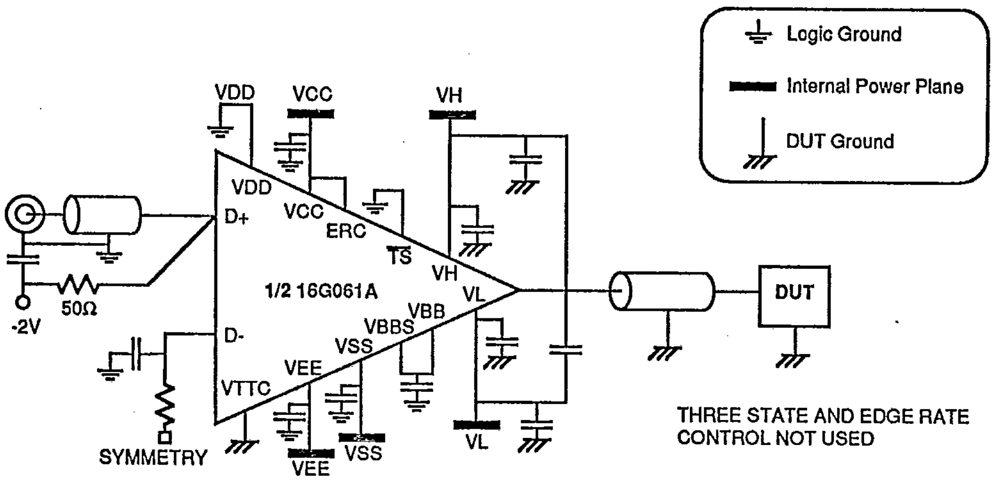
All outputs must be either source (back or series) terminated or shunt (load) terminated at the DUT unless the DUT is placed no more than 0.25" distant from the 16G061A. Shunt terminations affect the output levels and VH and VL must be compensated accordingly, as previously discussed. Source termination has the advantage of reducing power and not introducing any DC error. Application Note #2 discusses the theory behind source termination and should be reviewed by those unfamiliar with the concept. In the source terminated case, a resistor must be added in series with the output such that its value when summed with RS = 8Ω will match the characteristic impedance (Z0) of the transmission line being driven. For example, a 42Ω resistor added in series with RS (8Ω) would match a 50Ω environment. Incorporation of the resistor internal to the package minimizes the effects of package parasitics, and results in improved waveforms.

Decoupling

Decoupling is provided inside the package via the VTTC pin. Nevertheless, 1000 pF rf chip caps and 0.1 pF leaded caps should be used for decoupling both VH and VL to the DUT ground return. The ground return pin VTTC must be connected to the DUT ground and may be either positive or negative with respect to VL and VH. **Note that VTTC should not be connected to the same plane as the input termination resistors, as this will provide a path to couple the output into the input and could induce oscillation.**

When laying out the printed circuit board make allowances for providing a multiplicity of decoupling capacitors of various sizes and configurations with minimum lead lengths between the DUT return (VTTC) plane and both VH and VL.

FIGURE 3.
PIN DRIVER LAYOUT



FUNCTIONAL DESCRIPTION (CONTINUED)

Driving the 16G061A

In order to achieve optimum edge propagation delay match, it is necessary to drive the 16G061A with ≤200 ps rise and fall times signals. ΔPropagation delay with duty cycle depends on the input threshold variation. Therefore, it can be minimized by driving the 16G061A with fast input rise and fall times. See Figure 4.

Δ Propagation delay with duty cycle can also be minimized by reclocking the data with a reference clock running at approximately 50% duty cycle. The reclocking flip-flop should have very fast rise and fall times such as GigaBit's 10G021A. Most input data duty cycle variation effects are canceled by the reclocking at the input of the flip flop and minimized thereafter by the fast rise and fall times of the GaAs flip flop.

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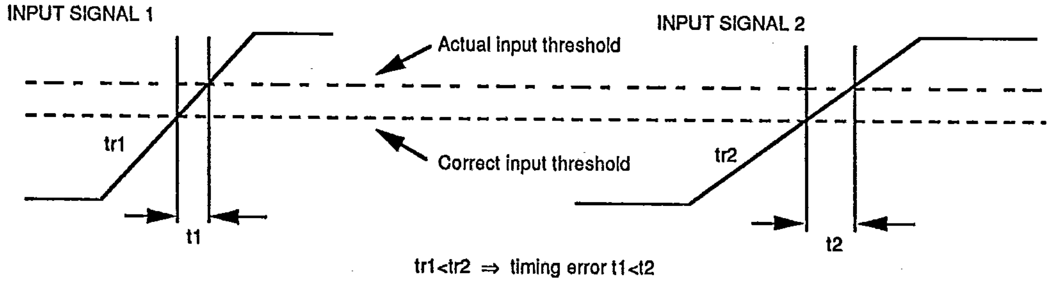
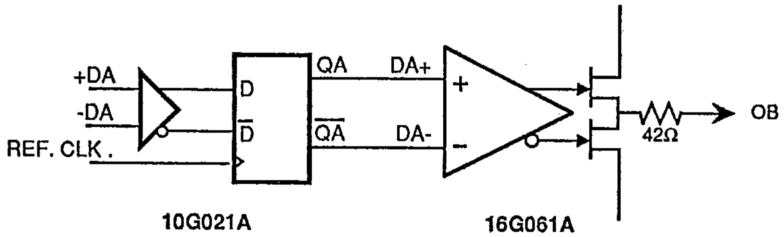
FIGURE 4



Δ propagation delay with duty cycle is dependent on the input rise and fall times.
Fast rise and fall times minimizes timing error and Δ propagation delay with duty cycle.

FIGURE 5



Elimination of the data duty cyle effect on propagation delay at the input of a 10G021A by reclocking the data with a 50% duty cycle reference clock

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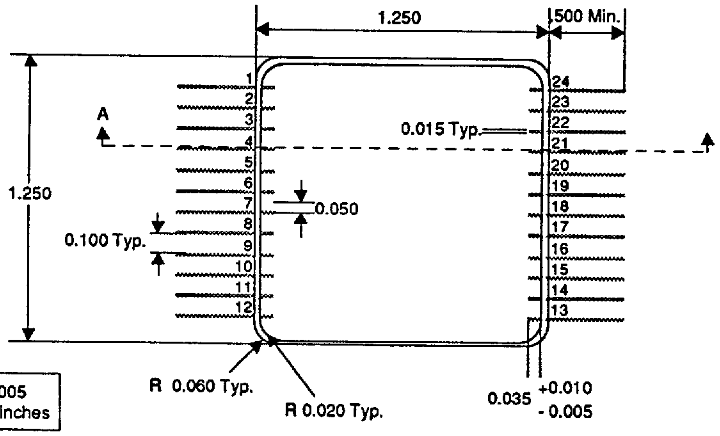
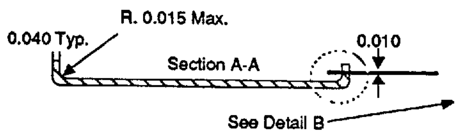
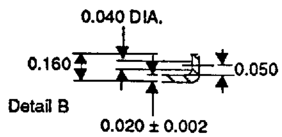
24 PIN METAL FLATPACK
18 PIN PACKAGE

24 PIN METAL FLATPACK
Type H

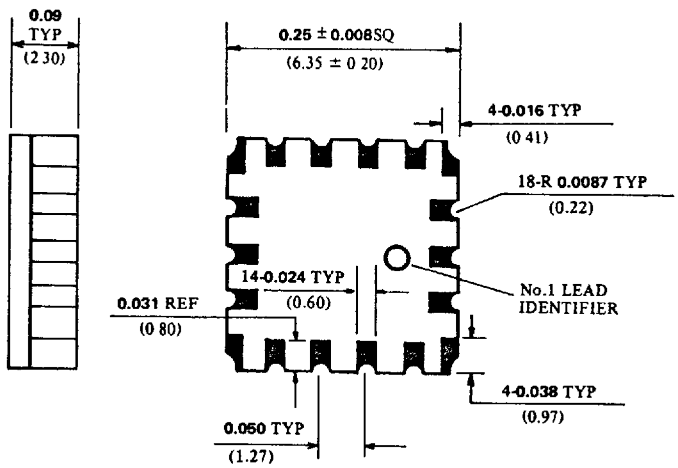


Tolerances: ±0.005
All dimension in inches





18 PIN LEADLESS CHIP CARRIER
TYPE L1



All dimensions shown in inches and (millimeters)

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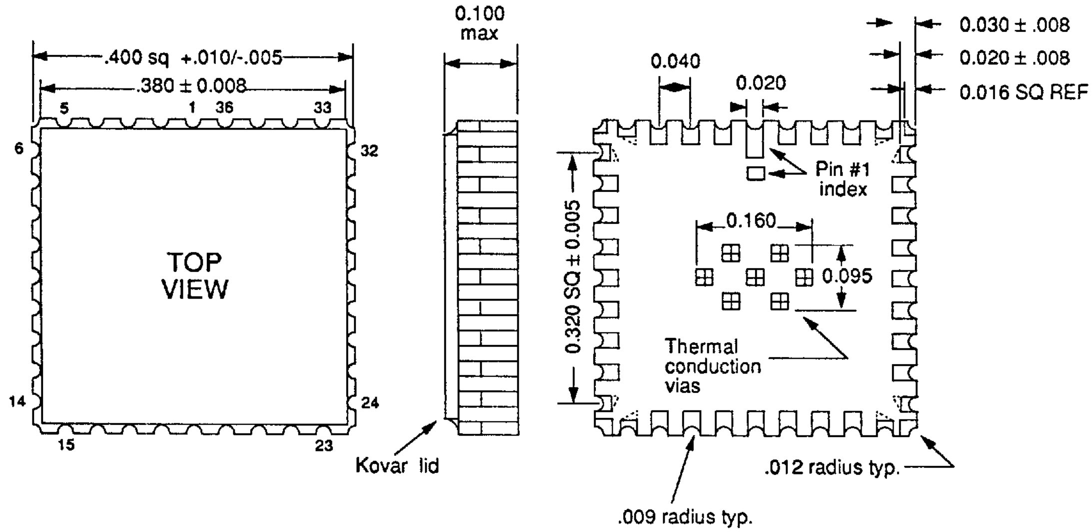
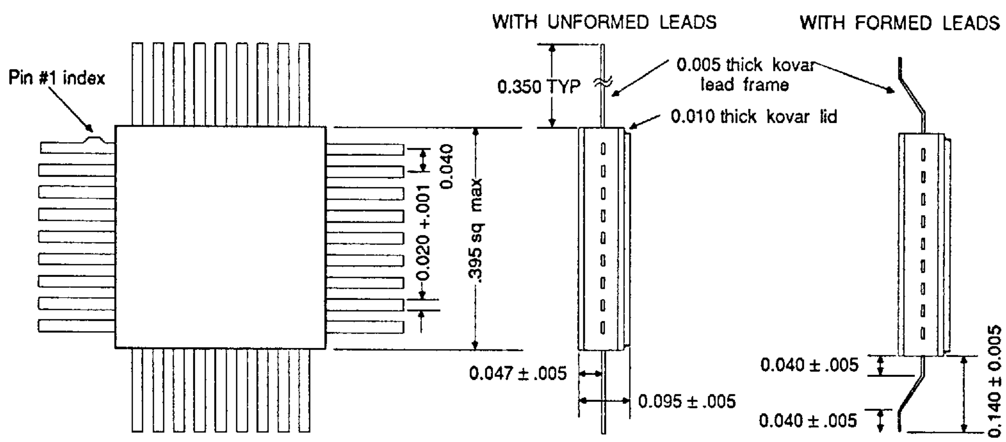
36 PIN PACKAGES

36 PIN LEADLESS CHIP CARRIER
TYPE L36



NOTES:
1) The package bottom thermal vias, top lid surface and 4 metallized corner castellations (when present) are all at Vss potential.
2) All dimensions in inches.
3) Plin #1 identifier may be an elongated pad or small, square gray marker.

36 I/O LEAD FLATPACK
TYPE F



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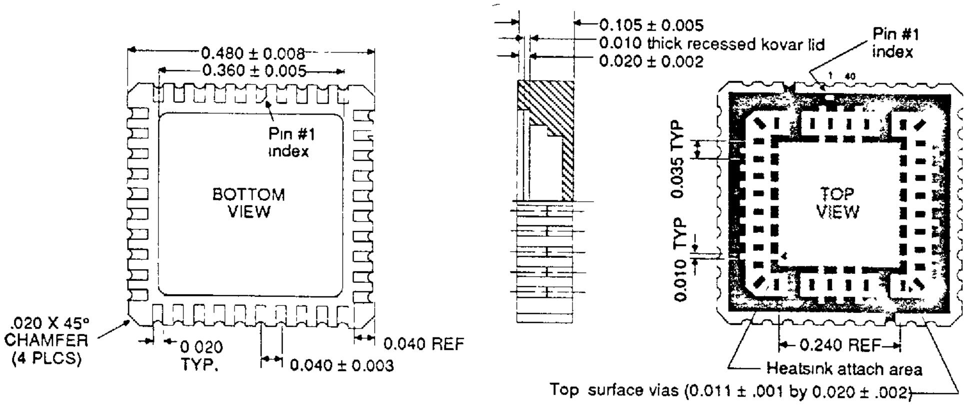
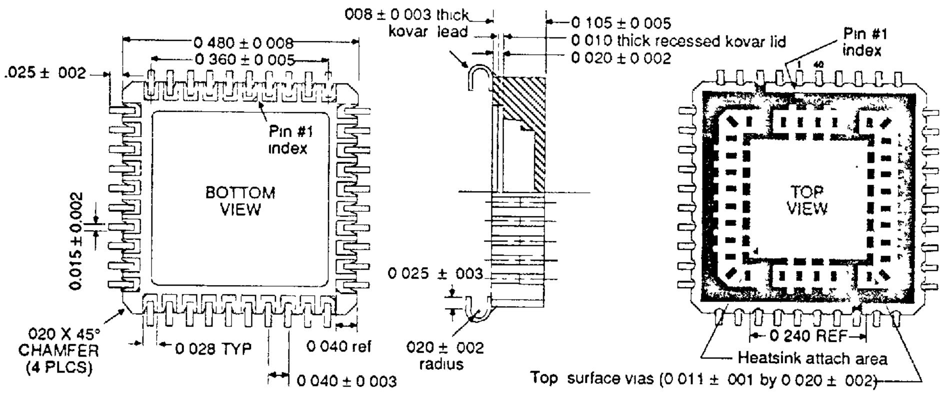
40 PIN PACKAGES

40 PIN LEADLESS CHIP CARRIER
TYPE L



40 PIN LEADED CHIP CARRIER
TYPE C

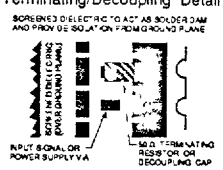


NOTES

(1) Footprint is JEDEC standard outline
(2) Top surface vias (for terminating resistors and decoupling capacitors) are not available on pins 3 4 17 18 23 24 37 and 38
(3) Top surface metal (not including vias) and pins 3 and 23 are fixed at VTT potential
(4) Recommended top surface chip resistors are 0 040 long by 0 020 wide by 0 010 thick typ 100 mw min nominal power rating (Mini-Systems MSR 21 or equivalent)
(5) Recommended top surface chip capacitors are 0 040 long by 0 030 wide by 0 020 thick typ 25V VDCW 1000 pf min (Johanson R09 case or equivalent)
(6) Recommended heatsinks are GBL P/Ns 90GHS 40 A and 90GHS 40 B
(7) Thermally conductive, electrically non-conductive epoxy is recommended for heatsink attachment (Ablestick 789 4 or 561K, or Thermalloy Thermabond™ or equivalent.)
(8) L40 and C40 packages are dimensionally identical except for contact finger width

TOP SURFACE LEGEND	
Metalized Ceramic	■
Screened Dielectric	□
Bare Ceramic.	□

Top Surface Terminating/Decoupling Detail

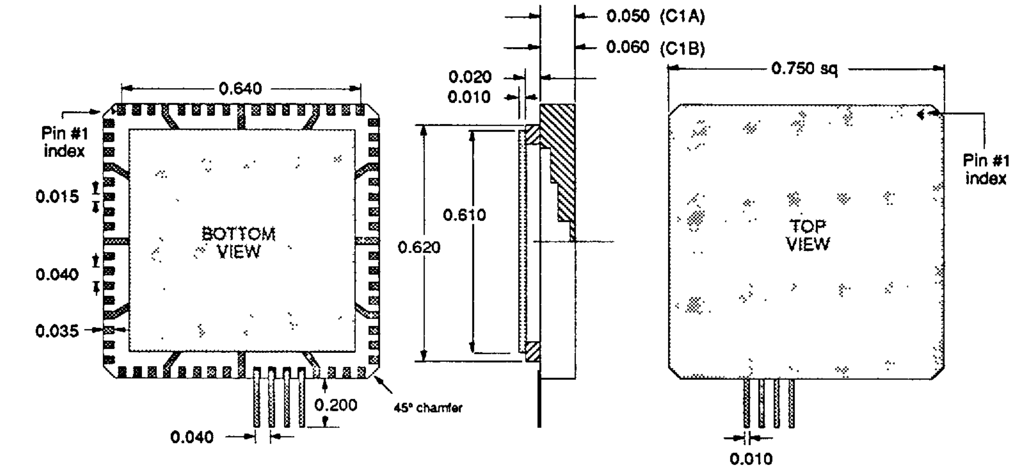


T-90-20

GigaBit Logic

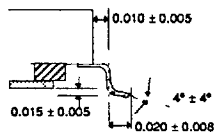
68 & 132 PIN PACKAGES

68 PIN LEADED CHIP CARRIER
TYPE C1

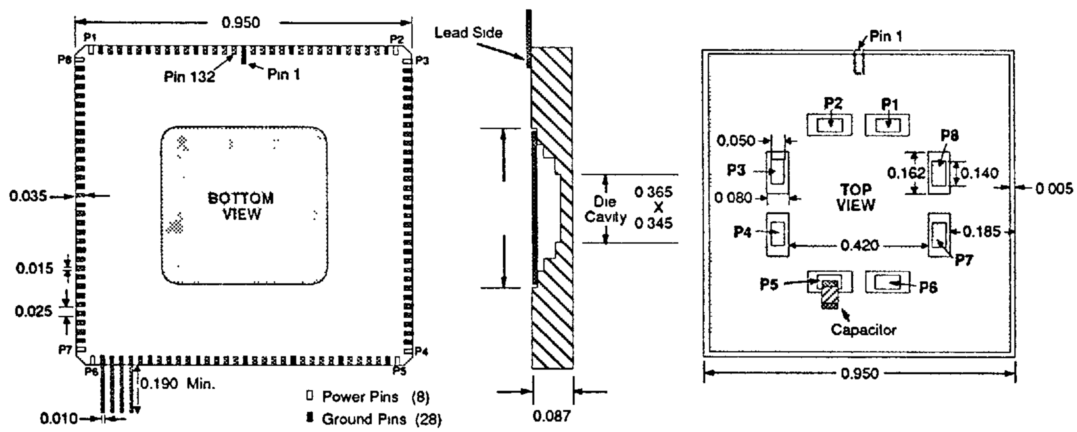


1. All dimensions in inches.
2. C1A PACKAGE: Package lid, top, and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).
3. C1B PACKAGE: Package lid and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).
4. Tolerance on all dimensions is ± 1 % but not larger than ± 0.005. Tolerance on 0.640 end pad to end pad dimension is ± 0.003.

GULLWING LEADS



132 PIN LEADED CHIP CARRIER
TYPE C3



All dimensions in inches

- Power Pins (8)
- Ground Pins (28)
- Signal pins (96)