



Dual 2-Wide 2-3-Input “OR-AND/OR-AND-INVERT” Gate

**ELECTRICALLY TESTED PER:
MPG 10H517**

The 10H517 is a general purpose logic element designed for use in data control, such as digital multiplexing or data distribution. Pin 9 is common to both gates. This MECL 10H part is a functional pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply current.

- Propagation Delay, 1.0 ns Typical
- 160 mW Max/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

FUNCTION	PIN ASSIGNMENTS			BURN-IN (CONDITION C)
	DIL	FLATS	LCC	
V _{CC1}	1	5	2	GND
A _{OUT}	2	6	3	51 Ω to V _{TT}
$\overline{A_{OUT}}$	3	7	4	51 Ω to V _{TT}
A _{1IN}	4	8	5	OPEN
A _{1IN}	5	9	7	OPEN
A _{2IN}	6	10	8	OPEN
A _{2IN}	7	11	9	OPEN
V _{EE}	8	12	10	V _{EE}
A _{2IN} , B _{2IN}	9	13	12	OPEN
B _{2IN}	10	14	13	OPEN
B _{2IN}	11	15	14	OPEN
B _{1IN}	12	16	15	OPEN
B _{1IN}	13	1	17	OPEN
$\overline{B_{OUT}}$	14	2	18	51 Ω to V _{TT}
B _{OUT}	15	3	19	51 Ω to V _{TT}
V _{CC2}	16	4	20	GND

BURN - IN CONDITIONS:

V_{TT} = - 2.0 V MAX/ - 2.2 V MIN

V_{EE} = - 5.7 V MAX/ - 5.2 V MIN

Military 10H517

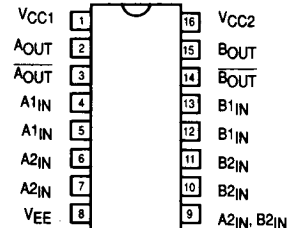


AVAILABLE AS

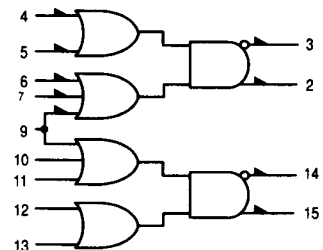
- 1) JAN: N/A
2) SMD: N/A
3) 883: 10H517/BXAJC
X = CASE OUTLINE AS FOLLOWS:

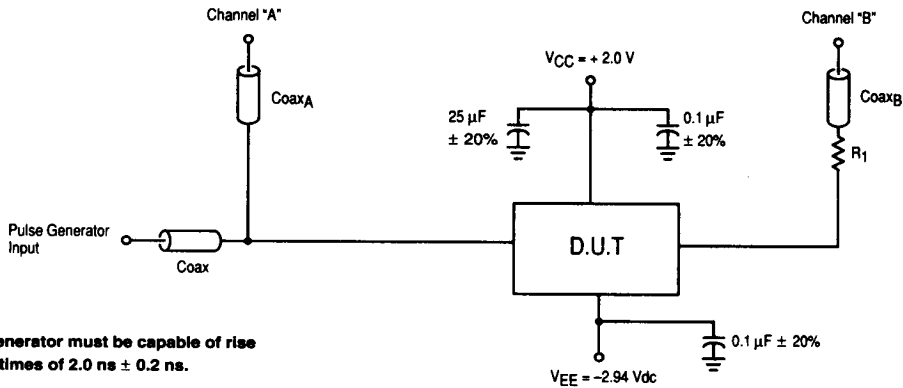
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter “M” appears before
the slash on LCC.



LOGIC DIAGRAM





Pulse generator must be capable of rise and fall times of $2.0 \text{ ns} \pm 0.2 \text{ ns}$.

NOTES

1. Length of Coax_A and Coax_B should be equal for equal time delay.
2. Unused outputs should be loaded 100Ω to ground.
3. 2:1 divider may be used.
4. $t_r = t_f = 1.0 \text{ ns} \pm 0.1 \text{ ns}$ measured at (20% - 80%).
5. $P_W \geq 20 \text{ ns}$.
6. $P_{RF} = 1.00 \text{ MHz}$.
7. $R_1 = 50 \Omega$ resistor in series with 50Ω coax constituting the 100Ω load.

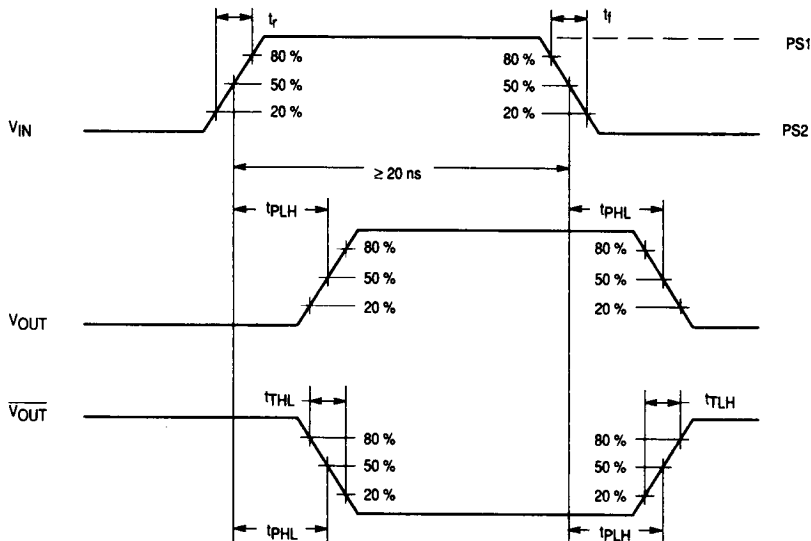


Figure 1. Switching Test Circuit and Waveforms

10H517 QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to -2.0 volts.

Test Temperature	Test Voltage Values (Volts)									
	V _{IH}	V _{IL}	V _{IHA}	V _{ILA}	PS ₁	PS ₂	VEE ₁	VEE ₂	VEEL	VEEL
T _A = 25 °C	-0.78	-1.95	-1.13	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94	-2.94
T _A = 125 °C	-0.63	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94	-2.94
T _A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW									
		+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments VCC = 0 V, Output Load = 100 Ω to - 2.0 V									
		Subgroup 1		Subgroup 2		Subgroup 3												
		Min	Max	Min	Max	Min	Max		V _{IH}	V _{IL}	V _{IHA}	V _{ILA}	VEE1	VEE2	V _{CC}	P. U. T.		
V _{OH}	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	V	4 - 7 9 - 13				8		1, 16	2, 3, 14, 15		
V _{OL}	Low Output Voltage	-1.95	-1.58	-1.95	-1.565	-1.95	-1.61	V	4 - 7 9 - 13				8		1, 16	2, 3, 14, 15		
V _{OHA}	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	V	4 - 7 9 - 13		4 - 7 9 - 13	4 - 7 9 - 13	8	8	1, 16	2, 3, 14, 15		
V _{OLA}	Low Output Voltage	-1.95	-1.58	-1.95	-1.565	-1.95	-1.61	V	4 - 7 9 - 13		4 - 7 9 - 13	4 - 7 9 - 13	8	8	1, 16	2, 3, 14, 15		
I _{EE}	Power Supply Current	-26		-29		-29		mA					8		1, 16	8		
I _{IH1}	Input Current High		320		510		510	μA	4, 5, 12, 13				8		1, 16	4, 5, 12, 13		
I _{IH2}	Input Current High		365		590		590	μA	6, 7, 10, 11				8		1, 16	6, 7, 10, 11		
I _{IH3}	Input Current High		460		755		755	μA	9				8		1, 16	9		
I _{IL}	Input Current Low	0.3		0.3		0.5		μA		4 - 7 9 - 13			8		1, 16	7, 9 - 13		

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Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments VCC = 2.0 V, Output Load = 100 Ω to GND							
		Subgroup 9		Subgroup 10		Subgroup 11										
		Min	Max	Min	Max	Min	Max									
t _{TLH}	Rise Time	0.5	1.6	0.5	1.7	0.5	1.5	ns	V _{IN}	V _{OUT}	V _{CC}	VEEL	PS ₁	P.U.T.		
t _{THL}	Fall Time	0.5	1.6	0.5	1.7	0.5	1.5	ns	4, 6, 11 12	2, 14, 15	1, 16	8	4, 6 11, 12	2, 3, 14, 15		
t _{pHL}	Propagation Delay High to Low	0.54	1.62	0.6	1.8	0.54	1.62	ns	4, 6, 11 12	2, 14, 15	1, 16	8	4, 6 11, 12	2, 3, 14, 15		
t _{pLH}	Propagation Delay Low to High	0.54	1.62	0.6	1.8	0.54	1.62	ns	4, 6, 11 12	2, 14, 15	1, 16	8	4, 6 11, 12	2, 3, 14, 15		