DS3140-1.0

MV8870 / MV8870-1

INTEGRATED DTMF RECEIVER

The MV8870 / MV8870-1 is a complete DTMF receiver integrating both the bandsplit filter and digital decoder functions, fabricated in GPS's double-poly ISO2-CMOS technology. The filter section uses switched capacitor techniques for high and low group filters; the decoder uses digital counting techniques to detect and decode all 16 DTMF tone pairs into a 4-bit code.

External component count is minimised by on-chip provision of a differential input amplifier, clock oscillator and latched 3-state bus interface.

The MV8870 and MV8870-1 are functionally identical, but differ in Electrical Characteristics.

FEATURES

- Complete DTMF Receiver
- Low Power Consumption
- Internal Gain Setting Amplifier
- Adjustable Guard Time
- Central Office Quality

APPLICATIONS

- Receiver Systems for BT or CEPT Specifications
- Paging Sytems
- Repeater Systems / Mobile Radio
- Credit Card Systems
- Remote Control

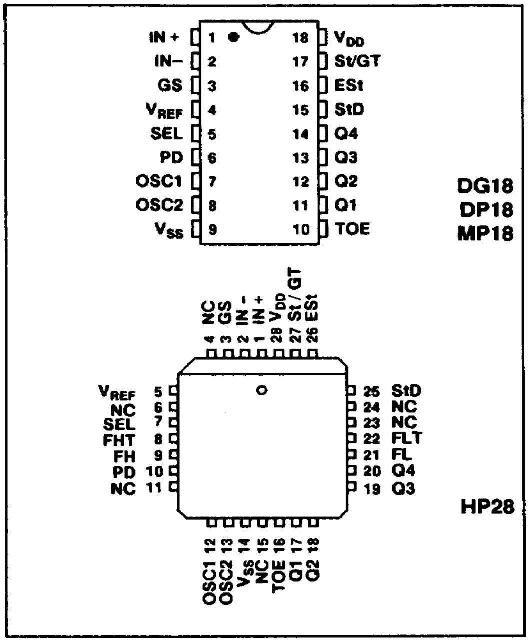


Fig.1 Pin connections - top view

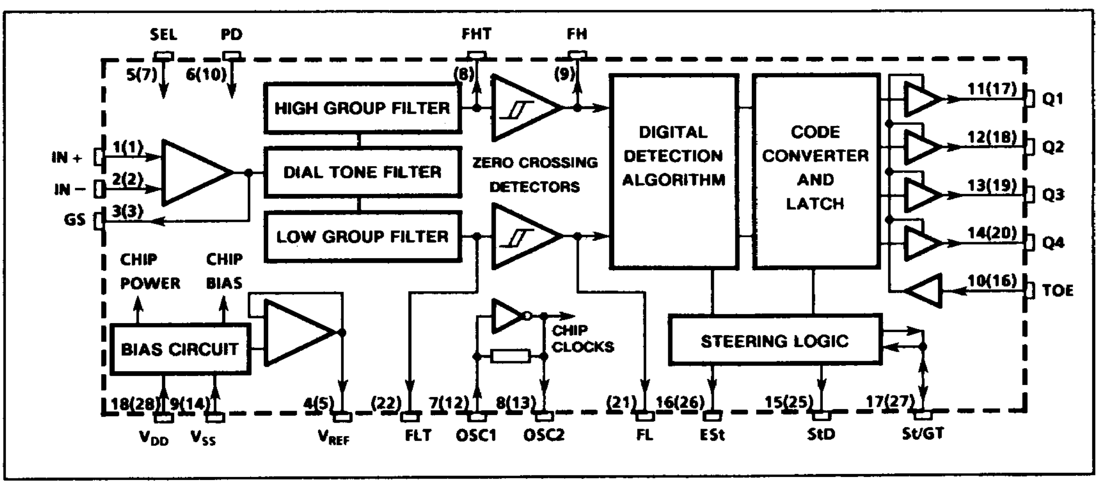


Fig. 2 Functional block diagram (Pin numbers in brackets refer to HP package)

FUNCTIONAL DESCRIPTION

The MV8870 / MV8870-1 monolithic DTMF receiver offers small size, low power consumption and high performance. Its architecture consists of a bandsplit filter section, which separates the high and low tone groups, followed by a digital counting section which verifies the frequency and duration of the received tones before passing the corresponding code to the output bus.

Filter Section

Separation of the low-group and high-group tones is achieved by applying the DTMF signal to the inputs of two sixth-order switched capacitor band-pass filters, the bandwidths of which correspond to the low and high group frequencies. The filter section also incorporates notches at 350 and 440 Hz for exceptional dial tone rejection (see Fig.3). Each filter is followed by a single order switched capacitor filter section which smooths the signals prior to limiting. Limiting is performed by high-gain comparators which are provided with hysteresis to prevent detection of unwanted low-level signals. The outputs of the comparators provide full rail logic swings at the frequencies of the incoming DTMF signals.

For testing and monitoring, the high and low group filter and zero crossing detector outputs are made available via FHT, FH, FLT and FL (HP package only).

Decoder Section

Following the filter section is a decoder employing digital counting techniques to determine the frequencies of the incoming tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals such as voice while providing tolerance to small frequency deviations and variations. This averaging algorithm has been developed to ensure an optimum combination of immunity to talk-off and tolerance to the presence of interfering frequencies (third tones) and noise. When the detector recognises the simultaneous presence of two valid tones (this is referred to as the 'Signal Condition' in some industry specifications) the Early Steering output (ESt) will go to an active state. Any subsequent loss of signal condition will cause the ESt pin to go to its inactive state (see Fig.5).

Steering Circuit

Before registration of a decoded tone-pair, the receiver checks for a valid signal duration (referred to as character recognition condition). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes the voltage at the St/GT pin ($V_{St/GT}$) to rise as the capacitor discharges (see Figs.4 and 5).

Provided signal condition is maintained (ESt remains high) for the validation period (t_{GTP}), $V_{St/GT}$ reaches the threshold (V_{TSt}) of the steering logic which allows it to register the tone pair and strobe the corresponding 4-bit code into the output latch (see Fig.6). At this point the St/GT pin is activated as an output and drives $V_{St/GT}$ to V_{DD} (see Fig.5).

St/GT continues to drive high as long as ESt remains high. After a short delay (t_{DP}) to allow the output latch to settle, the delayed steering output pin (StD) goes high to indicate that the code for a new received tone-pair is available. The contents of the output latch are output onto the output bus (Q1 to Q4 pins) when the three-state output enable (TOE) pin is high.

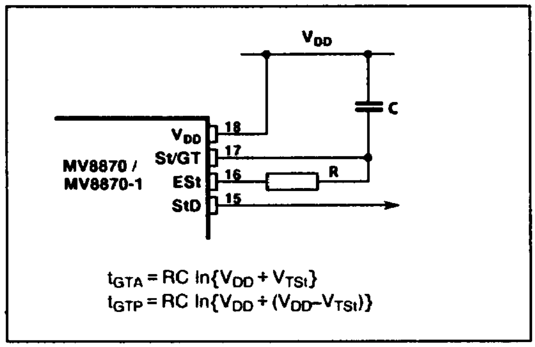


Fig. 4 Basic Steering Circuit

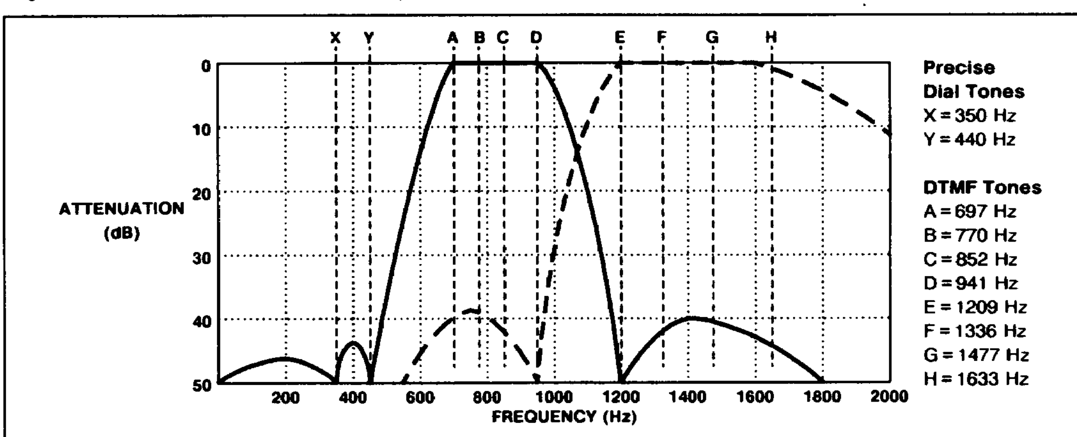


Fig. 3 Filter response

The steering circuit works in reverse to validate the interdigit pause between signals. Thus as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (drop-out) too short to be considered a valid pause. This facility, together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

APPLICATIONS

A simple application circuit is shown in Fig.7. This has a symmetric guard time circuit, a single-ended analog input and a dedicated crystal oscillator.

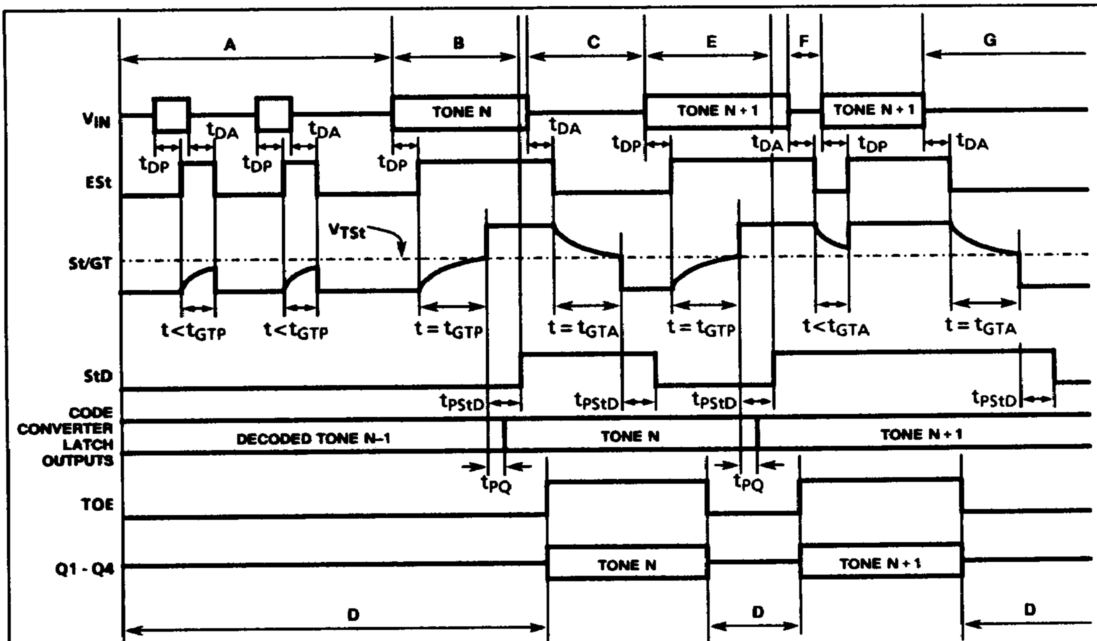
Guard Time Adjustment

In many situations not requiring seperate selection of tone duration and interdigit pause, the simple steering circuit shown in Fig.7 is applicable. Component values are chosen according to the formulae (see Figs. 4, 8a and 8b):-

$$t_{REC} = t_{DP} + t_{GTP}$$
$$t_{ID} = t_{DA} + t_{GTA}$$

The value of t_{DP} is a device parameter (see Dynamic Characteristics and Fig.5) and t_{REC} is the minimum signal duration to be recognised by the receiver. Likewise t_{DA} is a device parameter (Fig.5) and t_{ID} is the minimum time taken to recognise an interdigit pause. A value for C2 of 0.1µF is recommended for most applications, leaving R3 to be selected by the designer.

Different steering arrangements may be used to select independantly the guard times for tone present (t_{GTP}) and tone absent (t_{GTA}). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigit pause. Guard time adjustment also allows the designer to tailor system parameters such as talk-off and noise immunity. Increasing t_{REC} improves talk-off performance since it reduces the probability that tones simulated by speech will maintain signal conditions long enough to be registered. Alternatively a relatively short t_{REC} with a long t_{ID} would be appropriate for extremely noisy environments where fast acquisition time and immunity to tone drop-outs are required. Design information for guard time adjustment is shown in Figs. 8a and 8b.



EXPLANATION OF EVENTS

A. Tone bursts detected, but tone duration invalid and output latch unchanged.

B. Tone N detected, tone duration valid, output latch updated and new data signalled by StD.

C. End of tone N detected, tone absent duration valid, but output latch not updated until next valid tone.

D. Outputs switched to high impedance.

E. Tone N+1 detected, tone duration valid, tone decoded, output latch updated (although outputs are currently high impedance) and new data signalled by StD.

F. Acceptable dropout of tone N+1, tone absent duration invalid, StD and output latch unchanged.

G. End of tone N+1 detected, tone absent duration valid, StD goes low but output latch not updated until next valid tone.

NOTES

1. t_{DP} time for valid tone present is a device parameter (see Electrical Characteristics).
2. t_{DA} time for valid tone absent is a device parameter (see Electrical Characteristics).
3. t_{GTP} and t_{GTA} are adjustable via external RC network at pins 16 and 17 (see Fig.4).
4. t_{PStD} and t_{PQ} are propagation delays given in the Electrical Characteristics.

Fig. 5 Timing Diagram.

f_{LOW}	f_{HIGH}	DIGIT	TOE	SELECT = L				SELECT = H			
				Q4	Q3	Q2	Q1	Q4	Q3	Q2	Q1
697	1209	1	H	0	0	0	1	0	0	0	1
697	1336	2	H	0	0	1	0	0	0	1	0
697	1477	3	H	0	0	1	1	0	0	1	1
770	1209	4	H	0	1	0	0	0	1	0	0
770	1336	5	H	0	1	0	1	0	1	0	1
770	1477	6	H	0	1	1	0	0	1	1	0
852	1209	7	H	0	1	1	1	0	1	1	1
852	1336	8	H	1	0	0	0	1	0	0	0
852	1477	9	H	1	0	0	1	1	0	0	1
941	1209	0	H	1	0	1	0	0	0	0	0
941	1336	*	H	1	0	1	1	1	0	1	0
941	1477	#	H	1	1	0	0	1	0	1	1
697	1633	A	H	1	1	0	1	1	1	0	0
770	1633	B	H	1	1	1	0	1	1	0	1
852	1633	C	H	1	1	1	1	1	1	1	0
941	1633	D	H	0	0	0	0	1	1	1	1
-	-	Any	L	Z	Z	Z	Z	Z	Z	Z	Z

Fig. 6 Functional decode table

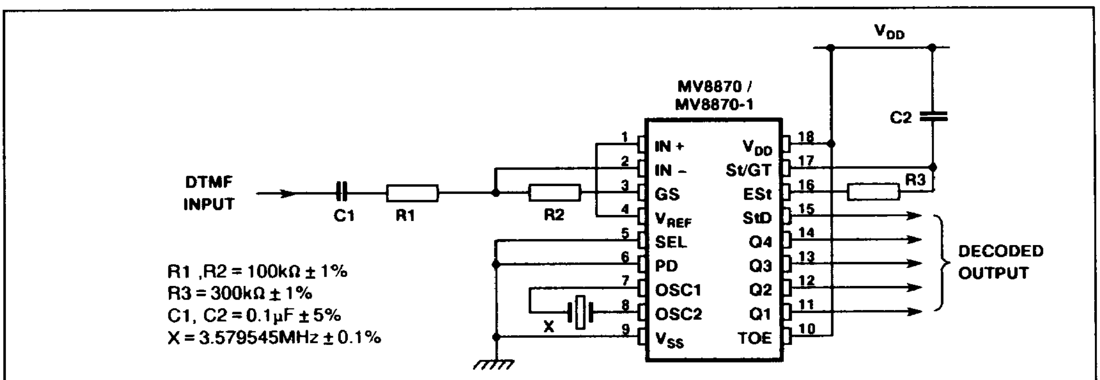


Fig. 7 Simple application circuit; single ended input.

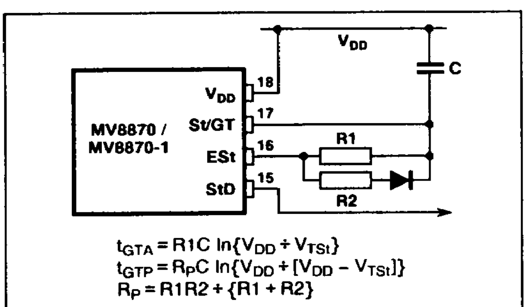


Fig. 8a Guard time adjustment ($t_{GTP} < t_{GTA}$)

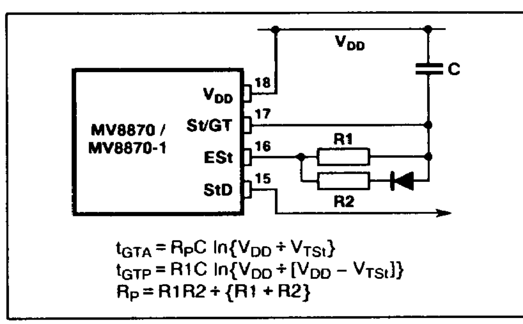


Fig. 8b Guard time adjustment ($t_{GTP} > t_{GTA}$)

Differential Input Configuration

The input arrangement of the MV8870 / MV8870-1 provides a differential input op. amp. and a bias source (V_{REF}) to bias the inputs at mid-rail. The gain may be adjusted through a feedback resistor from the op. amp. output (GS). In a single-ended configuration the input pins are connected as shown in Fig. 7 where the op. amp. is connected to give unity gain and the V_{REF} pin biases the input at (V_{DD} + 2).

Fig.9 shows the differential configuration. In this circuit gain is adjusted through the feedback resistor R5.

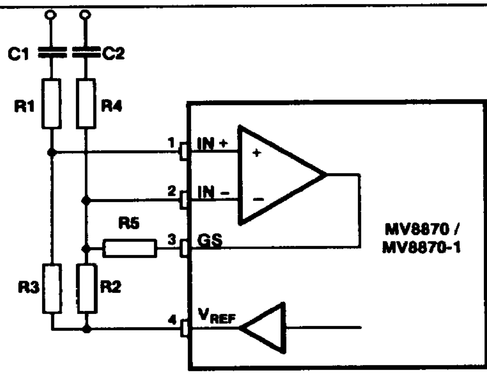
Crystal Oscillator

The internal clock circuit is completed with the addition of an external 3.58MHz crystal which is normally connected as shown in Fig. 7. However it is possible to configure several MV8870 / MV8870-1 devices to use only a single oscillator crystal.

The devices are chained together with the oscillator output of the first device in the chain capacitively coupled to the oscillator input of the second device and so on down the chain. The details are shown in Fig.10. Precision balancing capacitors are not required as problems of unbalanced loading are not a concern.

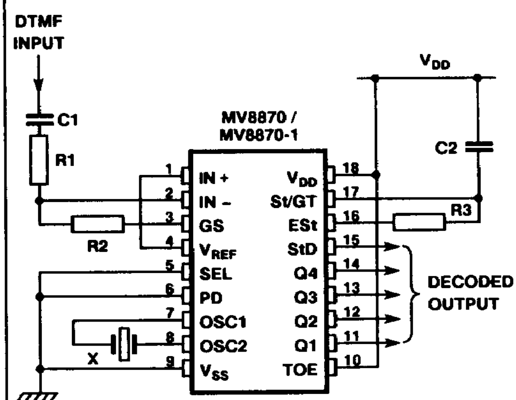
Receiver System For BT Specification POR 1151

The circuit shown in Fig.11 illustrates the use of the MV8870-1 in a typical receiver system. The BT specification defines the non-operate level as input signals below –34 dBm. This is obtained by choosing R1 and R2 to give 3dB of attenuation so that an input of –34 dBm corresponds to –37 dBm at the op. amp. output pin (GS). The tolerances on R3 and C2 give a tolerance on guard time of 6%. For better performance the non-symmetric guard time circuit shown in Fig.12 is recommended.



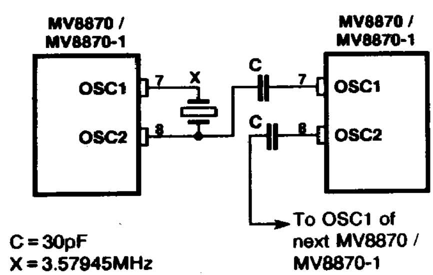
Differential Input Amplifier
C1 = C2 = 0.01µF
R1 = R4 = R5 = 100kΩ   Resistors are ± 1%
R2 = 60kΩ   Capacitors are ± 5%
R3 = R2R5 + (R2 + R5)
Voltage Gain ($A_V$diff) = R5 + R1
Input Impedance
$Z_{INDIFF} = 2[R1^2 + (1 + \omega C)^2]^{1/2}$

Fig. 9 Differential input configuration.



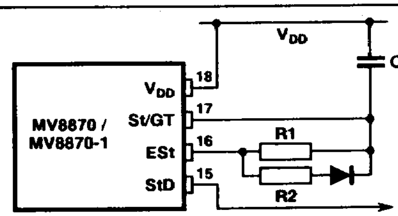
R1 = 102kΩ ± 1%
R2 = 71.5kΩ ± 1%
R3 = 390kΩ ± 1%
C1, C2 = 0.1µF ± 5%
X = 3.579545MHz ± 0.1%

Fig. 11 Single ended circuit for BT/CEPT Specs.



C = 30pF
X = 3.57945MHz

Fig. 10 Oscillator circuit



$t_{GTA} = R1C \ln\{V_{DD} + V_{TSt}\}$
$t_{GTP} = R_PC \ln\{V_{DD} + [V_{DD} - V_{TSt}]\}$
$R_P = R1R2 + (R1 + R2)$

R1 = 368kΩ ± 1%
R2 = 2.2MΩ ± 1%
C = 0.1µF ± 5%

Fig. 12 Non-symmetric guard time circuit.

PIN DESCRIPTIONS (Note 1)

Symbol	Pin no.	Pin name and description
IN +, IN –	1 (1) 2 (2)	**In Plus and Minus (Voltage Inputs).** These are respectively the non-inverting and inverting inputs to the front-end op-amp. The DTMF input is applied to these pins in normal operation.
GS	3 (3)	**Gain Select (Voltage Output).** This pin is connected to the output of the front-end op-amp. A feedback resistor between this pin and the inverting input (IN –) controls the front-end gain.
V_{REF}	4 (5)	**Reference Voltage (Voltage Output).** This pin outputs a voltage which is half-way between the power supply voltages (V_{SS} and V_{DD}). It can be used to bias the input signal.
SEL	5 (7)	**Select Input.** This pin determines the Q4..Q1 truth table as shown in Fig. 6
PD	6 (10)	**Power Down Input.** This pin is used to power down and inhibit the oscillator. It is active high and includes an internal pull-up resistor.
FHT	- (8)	**Filter High Tones.** Sine wave output from the high group filter circuit.
FH	- (9)	**High Frequency Output.** Square wave output from the high group zero crossing detector.
OSC1	7 (12)	**Oscillator 1 (Digital Input).** This is the input to the inverter of the oscillator circuit. There is an internal biasing resistor between this pin and the inverter output (OSC2). A 3.579545MHz crystal is normally connected externally between the two pins to complete the oscillator circuit.
OSC2	8 (13)	**Oscillator 2 (Digital Output).** This is the output of the inverter of the oscillator circuit. There is an internal biasing resistor between this pin and the inverter input (OSC1). A 3.579545MHz crystal is normally connected externally between the two pins to complete the oscillator circuit.
V_{SS}	9 (14)	**Negative Supply (Power Input).** This is the negative power supply for the device. It is normally 0V.
TOE	10 (16)	**Three-State Output Enable (Digital Input with Pull-up).** If this pin is high then the decoder outputs (Q1 to Q4) are enabled. If it is low then the outputs go into their high-impedance state. There is an internal pull-up at this pin.
Q1 Q2 Q3 Q4	11 (17) 12 (18) 13 (19) 14 (20)	**Q1 to Q4 (Three-State Outputs).** When the TOE pin is high these pins output the code in the output latch which corresponds to the last valid tone-pair detected. They go into their high-impedance state when the TOE pin is low.
FL	- (21)	**Low Frequency Output.** Square wave output from the low group zero crossing detector.
FLT	- (22)	**Filter Low Tones.** Sine wave output from the low group filter circuit.
StD	15 (25)	**Delayed Steering (Digital Output).** This pin follows the ESt and St/GT pins. It goes high to indicate that a new tone-pair has been detected and the corresponding code has been loaded into the output latch. It goes low to indicate that a new tone-pair is expected.
ESt	16 (26)	**Early Steering (Digital Output).** This pin goes high when the digital detection algorithm decides that there is a valid DTMF input. It goes low as soon as the algorithm decides that there is no valid DTMF input. In normal use this pin is used to drive an external guard time circuit which in turn drives the St/GT pin.
St/GT	17 (27)	**Steering / Guard Time (Voltage Input / Digital Output).** This pin follows the ESt pin. When ESt pin changes state this pin acts as an input and monitors the voltage developed here by the ESt pin acting through the external guard time circuit. When the voltage reaches the internally generated V_{TSt} level then this pin acts as an output and pulls itself fully to the state of the ESt pin. When this pin goes fully high a new code is loaded into the output latch and the StD pin goes high. When this pin goes fully low the device prepares itself for a new tone-pair and the StD pin goes low.
V_{DD}	18 (28)	**Positive Supply (Power Input).** This is the positive power supply for the device. It is normally 5V.

Note: 1. Figures in brackets are for HP28 package.

RECOMMENDED OPERATING RANGE

Characteristic	Symbol	Value (MV8870)			Value (MV8870-1)			Units	Conditions
		Min	Typ	Max	Min	Typ	Max		
Positive supply voltage	V_{DD}	4.75	5.0	5.25	4.75	5.0	5.25	V	
Operating temperature	T_{OP}	-40	+25	+80	-40	+25	+80	°C	

ELECTRICAL CHARACTERISTICS Over Recommended Operating Range (unless otherwise specified)

Test conditions (unless otherwise stated):

Voltages measured with respect to ground (V_{SS}).

Typical figures are for design aid only; they are not guaranteed and are not subject to production testing.

Static Characteristics

Characteristic	Symbol	Value (MV8870)			Value (MV8870-1)			Units	Conditions
		Min	Typ	Max	Min	Typ	Max		
Power dissipation	P_D		15	35		15	37	mW	$f_0 = 3.579545$MHz
V_{DD} supply current	I_{DD}		3.0	7.0		3.0	7.0	mA	
Input high voltage (OSC1 & TOE)	V_{IH}	3.5		V_{DD}	3.5		V_{DD}	V	
Input low voltage (OSC1 and TOE)	V_{IL}	0		1.5	0		1.5	V	
Input leakage current (OSC1, IN+ and IN–)	I_I		100			100		nA	$0 \leq V_{PIN} \leq V_{DD}$
Internal pull-up current (TOE)	I_{PU}		7.5	15.0		7.5	15.0	µA	$0 \leq V_{PIN} \leq V_{DD}$
Steering threshold voltage (St/GT)	V_{TSt}	2.2	2.35	2.5	2.2	2.35	2.5	V	
Low level output voltage	V_{OL}		0.03			0.03		V	No Load
High level output voltage	V_{OH}		4.97			4.97		V	No Load
Output low sink current (OSC2, Q1-Q4, StD and ESt)	I_{OL}	1.0	2.5		1.0	2.5		mA	$V_{PIN} = 0.4$V
Output high source current (OSC2, Q1-Q4, StD and ESt)	I_{OH}	0.4	0.8		0.4	0.8		mA	$V_{PIN} = 4.6$V
Reference voltage	V_{REF}	2.4		2.7	2.4		2.8	V	No Load
V_{REF} output resistance	R_{REF}		10.0			10.0		kΩ	
Pin capacitance	C_P		7.0	15.0		7.0	15.0	pF	Pin to supplies

Dynamic Characteristics : Input Op Amp

Characteristic	Symbol	Value (MV8870)			Value (MV8870-1)			Units	Conditions
		Min	Typ	Max	Min	Typ	Max		
Input impedance (IN + and IN–)	R_{IN}		10			10		MΩ	1kHz
Input offset voltage (IN + and IN–)	V_{OS}		25			25		mV	
Input leakage current	I_{IN}		100			100		nA	$V_{SS} < V_{IN} < V_{DD}$
Power supply rejection	PSRR		60			60		dB	1kHz
Common mode range	V_{CM}		3.0			3.0		V	No Load
Common mode rejection	CMRR		60			60		dB	$V_{IN} = V_{REF} \pm 1.3V$
DC open loop voltage gain	A_{VOL}		65			65		dB	
Open loop unity gain bandwidth	f_C		1.5			1.5		MHz	
Output voltage swing (GS)	V_O		4.5			4.5		V_{p-p}	R_{OUT} to $V_{SS} \geq 100k\Omega$
Output capacitive load (GS)	C_{OUT}			100			100	pF	
Output resistive load (GS)	R_{OUT}	50			50			kΩ	

Dynamic Characteristics : Oscillator Circuit

Characteristic	Symbol	Value (MV8870 and MV8870-1)			Units	Conditions
		Min	Typ	Max		
Crystal/clock frequency (OSC1 and OSC2)	f_O	3.579	3.579545	3.5831	MHz	
Oscillator input rise time (OSC1) - external clock	t_{OR}			110	ns	See Fig. 13
Oscillator input high time (OSC1) - external clock	t_{OH}	110		170	ns	See Fig. 13
Oscillator input fall time (OSC1) - external clock	t_{OF}			110	ns	See Fig. 13
Oscillator Input Low Time (OSC1 Pin) - external clock	t_{OL}	110		170	ns	See Fig. 13
Oscillator Output Load (OSC2)	C_{LO}			30	pF	

Dynamic Characteristics : Detector

Characteristic	Symbol	Value (MV8870)			Value (MV8870-1)			Units	Notes
		Min	Typ	Max	Min	Typ	Max		
Valid input level (GS)	V_{VL} P_{VL}	77.7 –29		2458 1.0	61.7 –31		2458 1.0	mV_{p-p} dBm	1, 2, 3, 5, 6, 9
Invalid input level (GS)	V_{IL} P_{IL}						30.8 –37	mV_{p-p} dBm	1, 2, 3, 5, 6, 9
Acceptable positive twist	T_{AP}		10		6.0	10		dB	2, 3, 6, 9
Acceptable negative twist	T_{AN}		10		6.0	10		dB	2, 3, 6, 9
Frequency deviation accept	Δ_{FA}	–1.5 –2.0		+1.5 +2.0	–1.5 –2.0		+1.5 +2.0	% Hz	2, 3, 5, 9
Frequency deviation rejected as too low	Δ_{FRL}		–5.0	–3.5		–5.0	–3.5	%	2, 3, 5, 9
Frequency deviation rejected as too high	Δ_{FRH}	3.5	5.0		3.5	5.0		%	2, 3, 5, 9
Third tone tolerance	P_{TTT}	–16				–18		dB	2, 3, 4, 5, 9, 12
Noise tolerance	P_{NT}		–12			–12		dB	2, 3, 4, 5, 7, 9, 10
Dial tone tolerance	P_{DTT}		+22			+22		dB	2, 3, 4, 5, 8, 9, 11
Tone present detect time	t_{DP}	5	11	14	5	11	14	ms	
Tone absent detect time	t_{DA}	0.5	4.0	8.5	0.5	4.0	8.5	ms	

NOTES
1. dBm = decibels above or below a reference power of 1mW into a 600Ω load.
2. Digit sequence consists of all DTMF tones.
3. Tone duration = 40ms, tone pause = 40ms.
4. Signal condition consists of nominal DTMF frequencies.
5. Both tones in composite signal have equal amplitudes.
6. Tone pair is deviated by ±(1.5% + 2Hz).
7. Bandwidth limited (3kHz) Gaussian noise.
8. The precise dial tone frequencies are (350Hz and 440Hz) ±2%.
9. For an error rate of better than 1 in 10,000.
10. Referenced to lowest frequency component in DTMF signal.
11. Referenced to the minimum valid input level.
12. Refer to Fig. 11. Input DTMF Tone Level at – 25dBm (– 28dBm at GS pin). Interference Frequency Range is 480 to 3400Hz.

Dynamic Characteristics : Decoder

Characteristic	Symbol	Value (MV8870/MV8870-1)			Units	Conditions
		Min	Typ	Max		
Propagation delay (St/GT to Q)	t_{PQ}		8	11	µs	TOE high. See Fig. 14
Propagation delay (St/GT to StD)	t_{PStD}		12		µs	See Fig. 14
Output data set-up time (Q to StD)	t_{QStD}		3.4		µs	TOE high. See Fig. 14
Enable propagation delay (TOE to Q)	t_{PTE}		50	60	ns	R_L = 10kΩ(pulldown) C_L = 50pF. See Fig. 15
Disable propagation delay (TOE to Q)	t_{PTD}		300		ns	R_L = 10kΩ(pulldown) C_L = 50pF. See Fig. 15

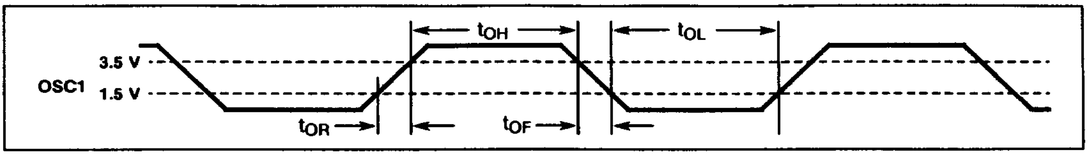


Fig. 13 Timing - external oscillator input.

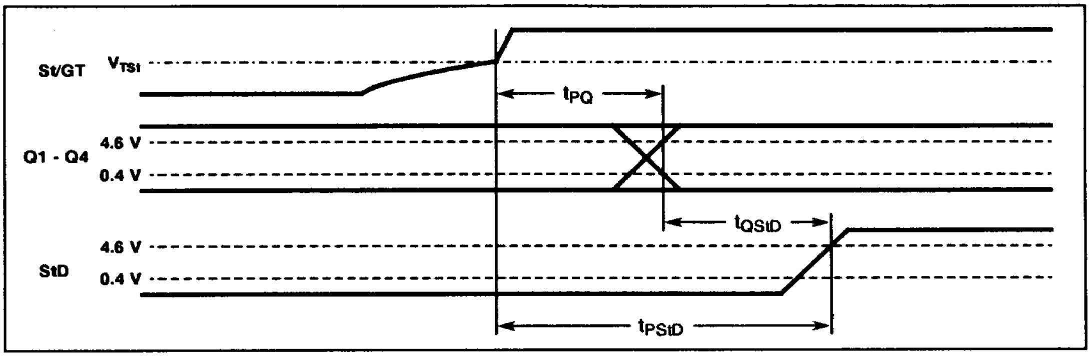


Fig. 14 Timing - decoded data.

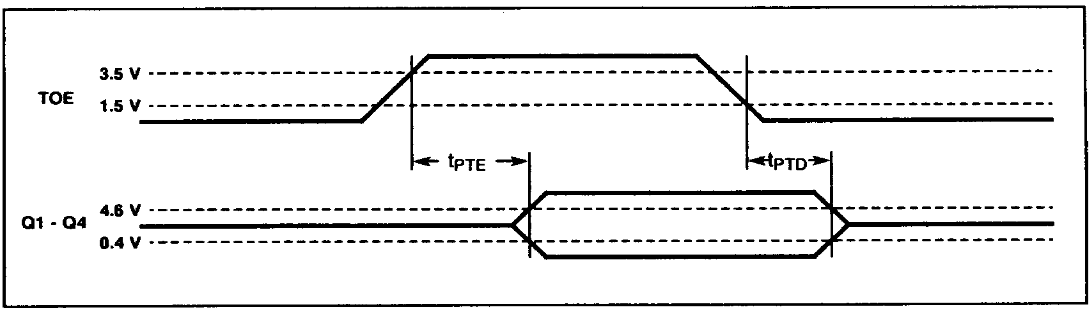


Fig. 15 Timing - Output enable and disable .

ABSOLUTE MAXIMUM RATINGS* Voltages are with respect to the negative power supply (V_{SS})

Parameter	Symbol	Value (MV8870)		Value (MV8870-1)		Units
		Min	Max	Min	Max	
Positive supply voltage (Pin 18)	V_{DD}		+6.0		+6.0	V
Voltage on any pin (other than supplies)	V_{MAX}	−0.3	V_{DD} + 0.3	−0.3	V_{DD} + 0.3	V
Current at any pin (other than supplies)	I_{MAX}		10		10	mA
Storage temperature	T_{STG}	−65	+150	−65	+150	°C
Package power dissipation	P_P		1000†		1000†	mW

* Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
†Derate parameter above +75°C at 16mW/°C, all leads soldered to board.