



Integrated Device Technology, Inc.

3.3V CMOS 16-BIT BIDIRECTIONAL TRANSCEIVERS

IDT54/74FCT163245/A/C

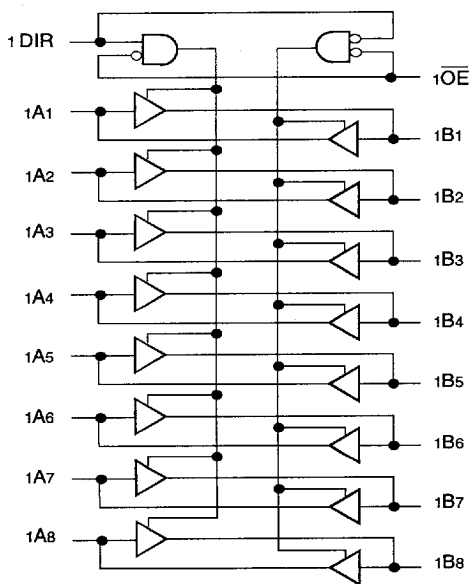
FEATURES:

- 0.5 MICRON CMOS Technology
- **Typical tsk(o) (Output Skew) < 250ps**
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- 25 mil Center SSOP and Cerpack Packages and
19.6 mil pitch TSSOP Package
- Extended commercial range of -40°C to +85°C
- Vcc = 3.3V ±0.3V, Normal Range or
Vcc = 2.7 to 3.6V, Extended Range
- CMOS power levels (0.4μW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Military product compliant to MIL-STD-883, Class B
- Low Ground Bounce (0.3V typ.)
- Inputs (except I/O) can be driven by 3.3V or 5V
components

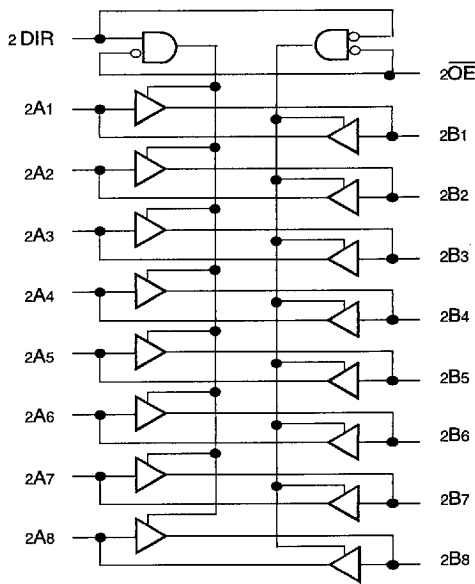
DESCRIPTION:

The FCT163245/A/C 16-bit transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power transceivers are ideal for synchronous communication between two busses (A and B). The Direction and Output Enable controls are designed to operate these devices as either two independent 8-bit transceivers or one 16-bit transceiver. The direction control pin (xDIR) controls the direction of data flow. The output enable pin (xOE) overrides the direction control and disables both ports. All inputs are designed with hysteresis for improved noise margin.

FUNCTIONAL BLOCK DIAGRAM



2554 drw 01



2554 drw 02

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MILITARY AND COMMERCIAL TEMPERATURE RANGES

JUNE 1996

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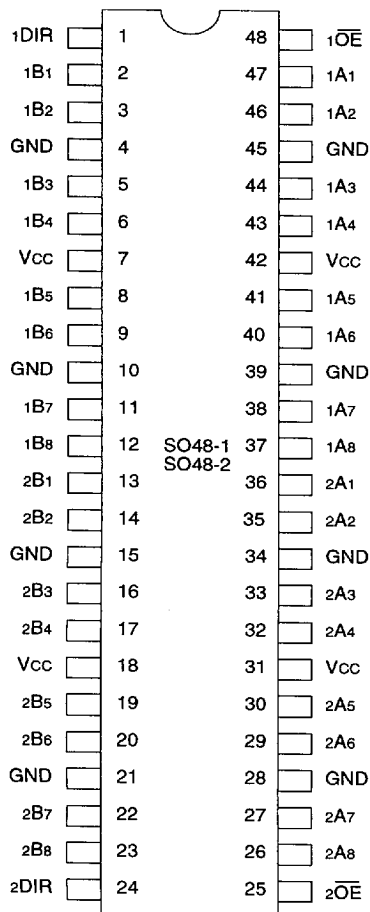
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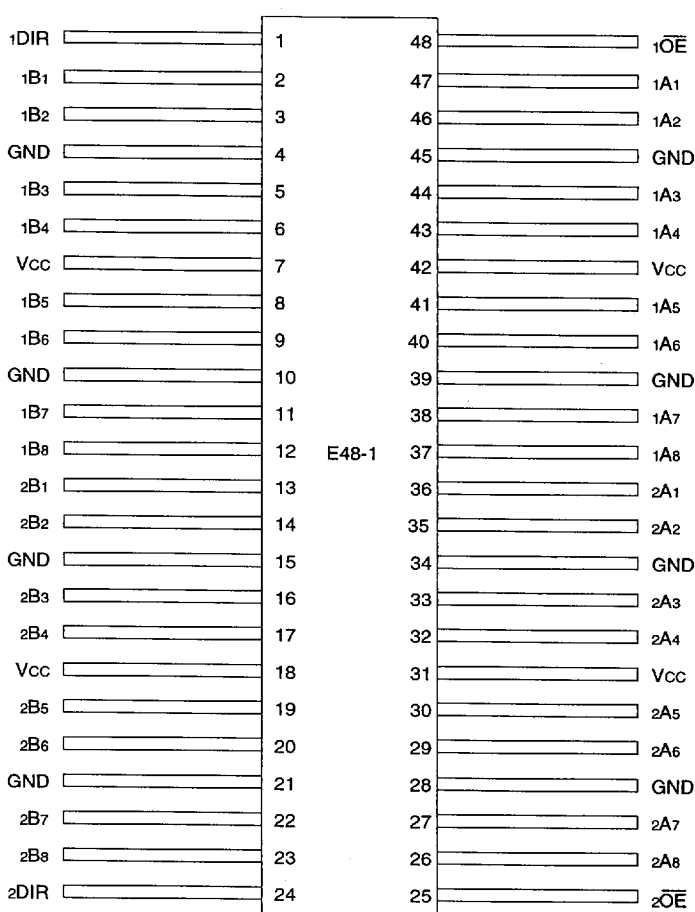
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PIN CONFIGURATIONS



2554 drw 03



2554 drw 04

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PIN DESCRIPTION

Pin Names	Description
xOE	Output Enable Input (Active LOW)
xDIR	Direction Control Input
xAx	Side A Inputs or 3-State Outputs
xBx	Side B Inputs or 3-State Outputs

2554 tbl 01

FUNCTION TABLE⁽¹⁾

Inputs		Outputs
xOE	xDIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

2554 tbl 02

NOTE:

1. H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	−0.5 to +4.6	−0.5 to +4.6	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
VTERM ⁽⁴⁾	Terminal Voltage with Respect to GND	−0.5 to Vcc + 0.5	−0.5 to Vcc + 0.5	V
TA	Operating Temperature	−40 to +85	−55 to +125	°C
TBIAS	Temperature Under Bias	−55 to +125	−65 to +135	°C
TSTG	Storage Temperature	−55 to +125	−65 to +150	°C
PT	Power Dissipation	1.0	1.0	W
IOUT	DC Output Current	−60 to +60	−60 to +60	mA

2554 lmk 03

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals.
3. Input terminals.
4. Output and I/O terminals.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	3.5	6.0	pF
Ci/O	I/O Capacitance	VOUT = 0V	3.5	8.0	pF

2554 lmk 04

NOTE:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 2.7\text{V}$ to 3.6V ; Military: $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 2.7\text{V}$ to 3.6V

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
	Input HIGH Level (I/O pins)			2.0	—	$V_{CC}+0.5$	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		-0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins) ⁽⁶⁾	$V_{CC} = \text{Max.}$	$V_I = 5.5\text{V}$	—	—	± 1	μA
	Input HIGH Current (I/O pins) ⁽⁶⁾		$V_I = V_{CC}$	—	—	± 1	
I_{IL}	Input LOW Current (Input pins) ⁽⁶⁾		$V_I = \text{GND}$	—	—	± 1	
	Input LOW Current (I/O pins) ⁽⁶⁾		$V_I = \text{GND}$	—	—	± 1	
I_{OZH}	High Impedance Output Current (3-State Output pins) ⁽⁶⁾	$V_{CC} = \text{Max.}$	$V_O = V_{CC}$	—	—	± 1	μA
I_{OZL}			$V_O = \text{GND}$	—	—	± 1	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
I_{ODH}	Output HIGH Current	$V_{CC} = 3.3\text{V}, V_{IN} = V_{IH}$ or $V_{IL}, V_O = 1.5\text{V}^{(3)}$		-36	-60	-110	mA
I_{ODL}	Output LOW Current	$V_{CC} = 3.3\text{V}, V_{IN} = V_{IH}$ or $V_{IL}, V_O = 1.5\text{V}^{(3)}$		50	90	200	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$	$I_{OH} = -0.1\text{mA}$	$V_{CC}-0.2$	—	—	V
		$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -3\text{mA}$	2.4	3.0	—	
		$V_{CC} = 3.0\text{V}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -6\text{mA MIL.}$ $I_{OH} = -8\text{mA COM'L.}$	2.4 ⁽⁵⁾	3.0	—	
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 0.1\text{mA}$	—	—	0.2	V
			$I_{OL} = 16\text{mA}$	—	0.2	0.4	
			$I_{OL} = 24\text{mA}$	—	0.3	0.55	
		$V_{CC} = 3.0\text{V}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 24\text{mA}$	—	0.3	0.50	
I_{OS}	Short Circuit Current ⁽⁴⁾	$V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$		-60	-135	-240	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = \text{Max.},$ $V_{IN} = \text{GND}$ or V_{CC}	COM'L.	—	0.1	10	μA
			MIL.	—	0.1	100	

2554 Ink 05

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 3.3\text{V}, +25^{\circ}\text{C}$ ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- This parameter is guaranteed but not tested.
- $V_{OH} = V_{CC} - 0.6\text{V}$ at rated current.
- The test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^{\circ}\text{C}$.

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POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$	$V_{IN} = V_{CC} - 0.6V^{(3)}$	—	2.0	30	μA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $\overline{xOE} = xDIR = GND$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	50	75	$\mu A / \text{MHz}$
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_i = 10\text{MHz}$ 50% Duty Cycle $\overline{xOE} = xDIR = GND$ One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	0.5	0.8	mA
			$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = GND$	—	0.5	0.8	
		$V_{CC} = \text{Max.}$ Outputs Open $f_i = 2.5\text{MHz}$ 50% Duty Cycle $\overline{xOE} = xDIR = GND$ Sixteen Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	2.0	3.0 ⁽⁵⁾	
			$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = GND$	—	2.0	3.3 ⁽⁵⁾	

2554 tbl 06

NOTES:

- For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 3.3V$, $+25^\circ C$ ambient.
- Per TTL driven input; all other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} \cdot D_H \cdot N_T + I_{CCD} \cdot (f_{CP} \cdot N_{CP} / 2 + f_i \cdot N_I)$
 $I_{CC} = \text{Quiescent Current (} I_{CCL}, I_{CCH} \text{ and } I_{CCZ} \text{)}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input}$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$
 $f_i = \text{Input Frequency}$
 $N_I = \text{Number of Inputs at } f_i$

SWITCHING CHARACTERISTICS OVER OPERATING RANGE⁽⁴⁾

Symbol	Parameter	Condition ⁽¹⁾	FCT163245				FCT163245A				FCT163245C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH	Propagation Delay A to B, B to A	CL = 50pF RL = 500Ω	1.5	7.0	1.5	7.5	1.5	4.6	1.5	4.9	1.5	4.1	—	—	ns
tpZH	Output Enable Time xOE to A or B		1.5	9.5	1.5	10.0	1.5	6.2	1.5	6.5	1.5	5.8	—	—	ns
tpHZ	Output Disable Time xOE to A or B		1.5	7.5	1.5	10.0	1.5	5.0	1.5	6.0	1.5	4.8	—	—	ns
tpZH	Output Enable Time xDIR to A or B ⁽⁵⁾		1.5	9.5	1.5	10.0	1.5	6.2	1.5	6.5	1.5	5.8	—	—	ns
tpHZ	Output Disable Time xDIR to A or B ⁽⁵⁾		1.5	7.5	1.5	10.0	1.5	5.0	1.5	6.0	1.5	4.8	—	—	ns
tsk(o)	Output Skew ⁽³⁾		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	—	ns

- NOTES:
- 2554 tbi 07
1. See test circuit and waveforms.

2. Minimum limits are guaranteed but not tested on Propagation Delays.

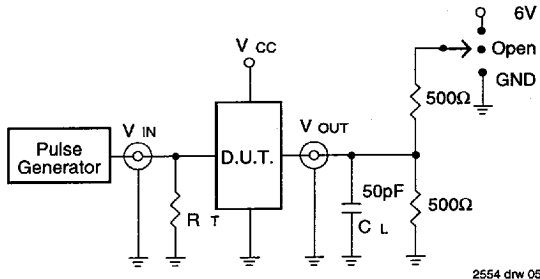
3. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

4. Propagation Delays and Enable/Disable times are with Vcc = 3.3V ± 0.3V, Normal Range. For Vcc = 2.7V to 3.6V, Extended Range, all Propagation Delays and Enable/Disable times should be degraded by 20%.

5. This parameter is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other tests	Open

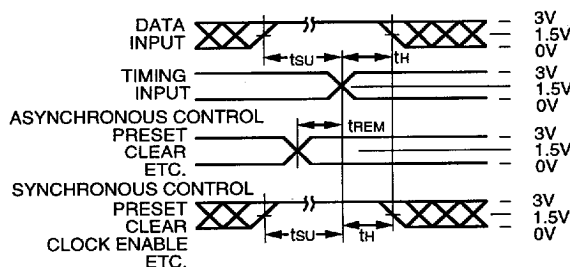
DEFINITIONS:

C_L = Load capacitance; includes jig and probe capacitance.

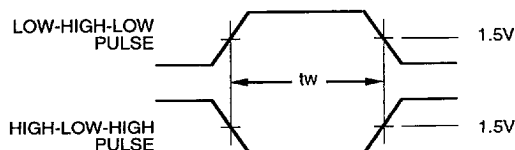
R_T = Termination resistance; should be equal to Z_{OUT} of the Pulse Generator.

2554 Ink 08

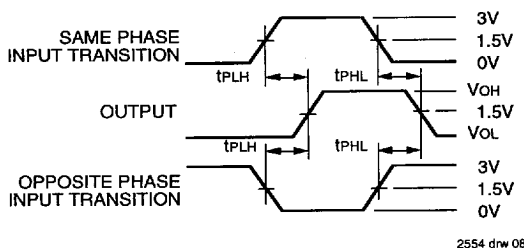
SET-UP, HOLD AND RELEASE TIMES



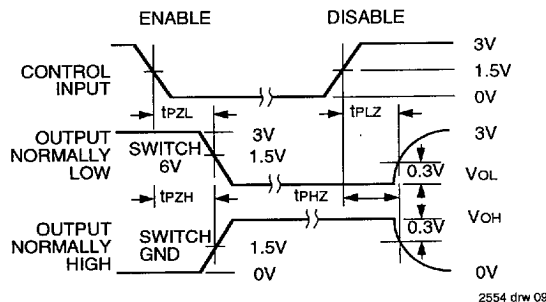
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_F \leq 2.5\text{ns}$; $t_R \leq 2.5\text{ns}$.
- If V_{CC} is below 3V, input voltage swings should be adjusted not to exceed V_{CC} .

ORDERING INFORMATION

IDT	XX	FCT	XXXX	X	X	
Temp. Range		Device Type		Package	Process	
					Blank B	Commercial MIL-STD-883, Class B
					PV PA E	Shrink Small Outline Package (SO48-1) Thin Shrink Small Outline Package (SO48-2) CERPACK (E48-1)
				163245 163245A 163245C		Non-Inverting 16-Bit Bidirectional Transceiver
				54 74		-55°C to +125°C -40°C to +85°C

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