



# 32x72 bits PC100 SDRAM Registered DIMM

with PLL, based on 32Mx4 SDRAM with LVTTL, 4 banks & 4K Refresh

## HYM71V75S3201 N-Series

### DESCRIPTION

The Hyundai HYM71V75S3201 N-Series are 32Mx72bits ECC Synchronous DRAM Modules. The modules are composed of eighteen 32Mx4bit CMOS Synchronous DRAMs in 400mil 54pin TSOP-II package, two 18bits driver ICs in 56pin TSSOP package, one PLL clock driver in 24pin TSSOP package and one 2Kbit EEPROM in 8pin TSSOP package on a 168pin glass-epoxy printed circuit board. One 0.22uF and one 0.0022uF decoupling capacitors per each SDRAM are mounted on the PCB.

The HYM71V75S3201 N-Series are Dual In-line Memory Modules suitable for easy interchange and addition of 256Mbytes memory. The HYM71V75S3201 N-Series are offering fully synchronous operation referenced to a positive edge of the clock. All inputs and outputs are synchronized with the rising edge of the clock input. The data paths are internally pipelined to achieve very high bandwidth. The DIMM /CAS latency in registered mode is one clock later than the device /CAS latency because of the register.

### FEATURES

- PC100MHz support
- 168pin SDRAM Registered DIMM
- Serial Presence Detect with EEPROM
- 1.70" (43.18mm) Height PCB with Double Sided components
- Single 3.3 ± 0.3V power supply
- All devices pins are compatible with LVTTL interface
- Data mask function by DQM
- SDRAM internal banks : four banks
- Module bank : one physical bank
- Auto refresh and self refresh
- 4096 refresh cycles / 64ms
- Programmable Burst Length and Burst Type
  - 1, 2, 4, 8 or Full Page for Sequential Burst
  - 1, 2, 4 or 8 for Interleave Burst
- Programmable /CAS Latency : 2, 3 Clocks

### ORDERING INFORMATION

| PART NO.            | MAX. FREQUENCY | INTERNAL BANK | REF. | POWER  | SDRAM PACKAGE | PLATING |
|---------------------|----------------|---------------|------|--------|---------------|---------|
| HYM71V75S3201TN-8   | 125MHz         | 4 Banks       | 4K   | Normal | TSOP-II       | Gold    |
| HYM71V75S3201TN-10P | 100MHz         |               |      |        |               |         |
| HYM71V75S3201TN-10S | 100MHz         |               |      |        |               |         |

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### PIN DESCRIPTION

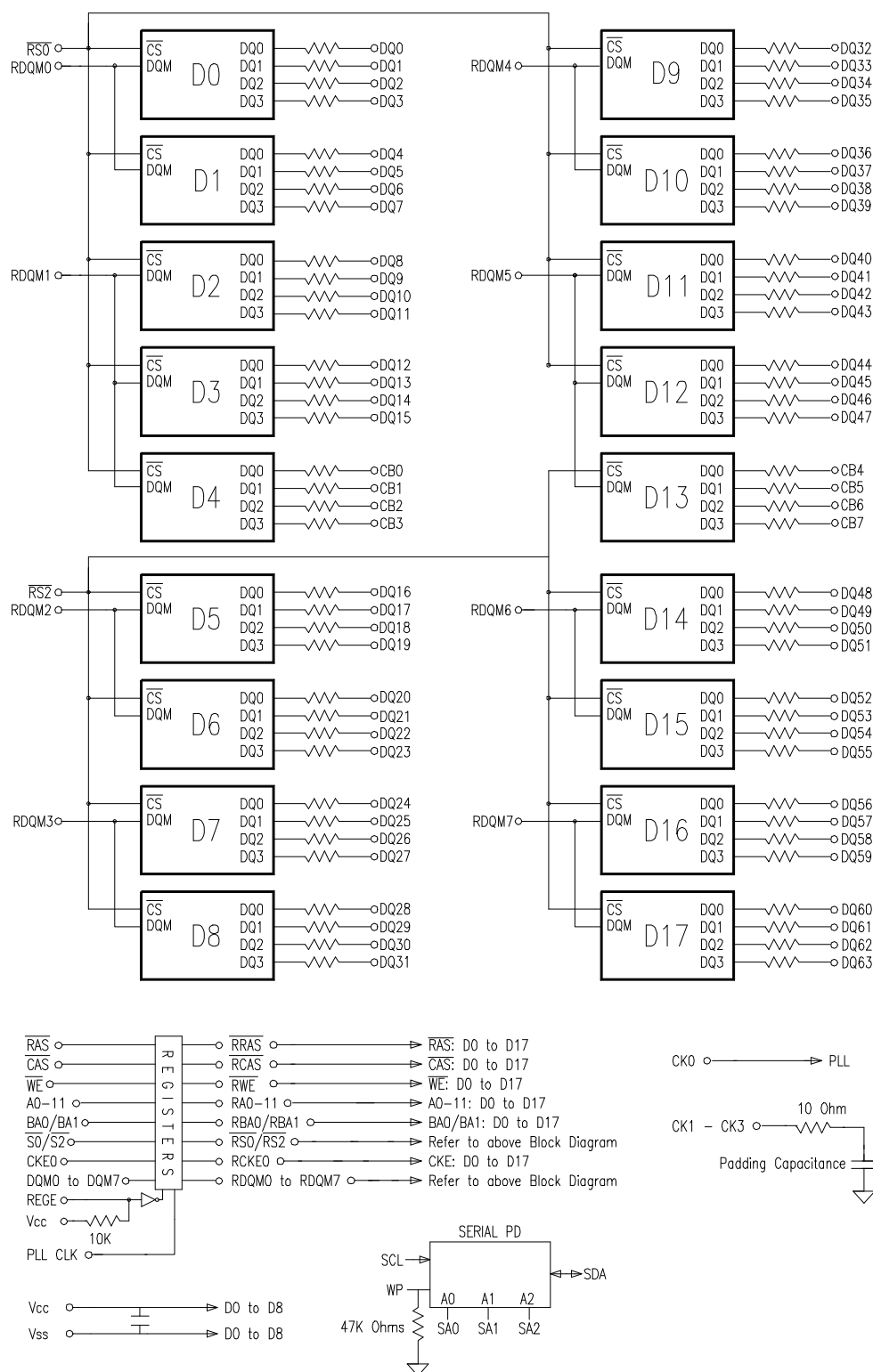
| PIN NAME  | DESCRIPTION            |                                                                                                                                              |
|-----------|------------------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| CK0~CK3   | Clock Inputs           | The System Clock Input. All other inputs are registered to the SDRAM on the rising edge of CLK.                                              |
| CKE0      | Clock Enable           | Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh.          |
| /S0, /S2  | Chip Select            | Enables or disables all inputs except CK, CKE and DQM.                                                                                       |
| BA0, BA1  | SDRAM Bank Address     | Select bank to be activated during /RAS activity.<br>Select bank to be read/written during /CAS activity                                     |
| A0~A11    | Address Inputs         | Row address : RA0~RA11, Column address : CA0~CA9, CA11<br>Auto-precharge flag : A10                                                          |
| /RAS      | Row Address Strobe     | /RAS define the operation.<br>Refer to the function truth table for details.                                                                 |
| /CAS      | Column Address Strobe  | /CAS define the operation.<br>Refer to the function truth table for details.                                                                 |
| /WE       | Write Enable           | /WE define the operation.<br>Refer to the function truth table for details.                                                                  |
| REGE      | Register Enable        | Register Enable pin which permits the DIMM to operation in Buffered Mode when REGE input is Low, in Registered Mode when REGE input is High. |
| DQM0~DQM7 | Data Input/Output Mask | Controls output buffers in read mode and masks input data in write mode.                                                                     |
| DQ0~DQ63  | Data Input/Output      | Multiplexed data input/output pins                                                                                                           |
| CB0~CB7   | ECC Data Input/Output  | Error Checking and Correction Bits                                                                                                           |
| VCC       | Power Supply (3.3V)    | Power supply for internal circuits and input/output buffers                                                                                  |
| VSS       | Ground                 | Ground                                                                                                                                       |
| SCL       | SPD Clock Input        | Serial Presence Detect Clock Input                                                                                                           |
| SDA       | SPD Data Input/Output  | Serial Presence Detect Data input/output                                                                                                     |
| SA0~SA2   | SPD Address Input      | Serial Presence Detect Address input                                                                                                         |
| WP        | Write Protect for SPD  | Write Protect for Serial Presence Detect on DIMM                                                                                             |
| NC        | No Connect             | No Connect or Don't Use                                                                                                                      |

### PIN ASSIGNMENTS

| FRONT SIDE       |        | BACK SIDE |      | FRONT SIDE |      | BACK SIDE |      |
|------------------|--------|-----------|------|------------|------|-----------|------|
| PIN NO.          | NAME   | PIN NO.   | NAME | PIN NO.    | NAME | PIN NO.   | NAME |
| 1                | VSS    | 85        | VSS  | 41         | VCC  | 125       | *CK1 |
| 2                | DQ0    | 86        | DQ32 | 42         | CK0  | 126       | NC   |
| 3                | DQ1    | 87        | DQ33 | 43         | VSS  | 127       | VSS  |
| 4                | DQ2    | 88        | DQ34 | 44         | NC   | 128       | CKE0 |
| 5                | DQ3    | 89        | DQ35 | 45         | /S2  | 129       | NC   |
| 6                | VCC    | 90        | VCC  | 46         | DQM2 | 130       | DQM6 |
| 7                | DQ4    | 91        | DQ36 | 47         | DQM3 | 131       | DQM7 |
| 8                | DQ5    | 92        | DQ37 | 48         | NC   | 132       | NC   |
| 9                | DQ6    | 93        | DQ38 | 49         | VCC  | 133       | VCC  |
| 10               | DQ7    | 94        | DQ39 | 50         | NC   | 134       | NC   |
| Architecture Key |        |           |      | 51         | NC   | 135       | NC   |
|                  |        |           |      | 52         | CB2  | 136       | CB6  |
| 11               | DQ8    | 95        | DQ40 | 53         | CB3  | 137       | CB7  |
| 12               | VSS    | 96        | VSS  | 54         | VSS  | 138       | VSS  |
| 13               | DQ9    | 97        | DQ41 | 55         | DQ16 | 139       | DQ48 |
| 14               | DQ10   | 98        | DQ42 | 56         | DQ17 | 140       | DQ49 |
| 15               | DQ11   | 99        | DQ43 | 57         | DQ18 | 141       | DQ50 |
| 16               | DQ12   | 100       | DQ44 | 58         | DQ19 | 142       | DQ51 |
| 17               | DQ13   | 101       | DQ45 | 59         | VCC  | 143       | VCC  |
| 18               | VCC    | 102       | VCC  | 60         | DQ20 | 144       | DQ52 |
| 19               | DQ14   | 103       | DQ46 | 61         | NC   | 145       | NC   |
| 20               | DQ15   | 104       | DQ47 | 62         | NC   | 146       | NC   |
| 21               | CB0    | 105       | CB4  | 63         | NC   | 147       | REGE |
| 22               | CB1    | 106       | CB5  | 64         | VSS  | 148       | VSS  |
| 23               | VSS    | 107       | VSS  | 65         | DQ21 | 149       | DQ53 |
| 24               | NC     | 108       | NC   | 66         | DQ22 | 150       | DQ54 |
| 25               | NC     | 109       | NC   | 67         | DQ23 | 151       | DQ55 |
| 26               | VCC    | 110       | VCC  | 68         | VSS  | 152       | VSS  |
| 27               | /WE    | 111       | /CAS | 69         | DQ24 | 153       | DQ56 |
| 28               | DQM0   | 112       | DQM4 | 70         | DQ25 | 154       | DQ57 |
| 29               | DQM1   | 113       | DQM5 | 71         | DQ26 | 155       | DQ58 |
| 30               | /S0    | 114       | NC   | 72         | DQ27 | 156       | DQ59 |
| 31               | NC     | 115       | /RAS | 73         | VCC  | 157       | VCC  |
| 32               | VSS    | 116       | VSS  | 74         | DQ28 | 158       | DQ60 |
| 33               | A0     | 117       | A1   | 75         | DQ29 | 159       | DQ61 |
| 34               | A2     | 118       | A3   | 76         | DQ30 | 160       | DQ62 |
| 35               | A4     | 119       | A5   | 77         | DQ31 | 161       | DQ63 |
| 36               | A6     | 120       | A7   | 78         | VSS  | 162       | VSS  |
| 37               | A8     | 121       | A9   | 79         | *CK2 | 163       | *CK3 |
| 38               | A10/AP | 122       | BA0  | 80         | NC   | 164       | NC   |
| 39               | BA1    | 123       | A11  | 81         | WP   | 165       | SA0  |
| 40               | VCC    | 124       | VCC  | 82         | SDA  | 166       | SA1  |
| Voltage Key      |        |           |      | 83         | SCL  | 167       | SA2  |
|                  |        |           |      | 84         | VCC  | 168       | VCC  |

**Note :** \*. CK1~CK3 are connected with termination R/C. (Refer to the Block Diagram.)

## BLOCK DIAGRAM



**Note :** 1. The serial resistor values of DQs are 10 Ohms.  
2. The padding capacitance of termination R/C for CK1–CK3 is 12pF.

### SERIAL PRESENCE DETECT

| BYTE NUMBER   | FUNCTION DESCRIBED                                           | FUNCTION                                                                                                  |      |      | VALUE             |      |      | NOTE |
|---------------|--------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------|------|------|-------------------|------|------|------|
|               |                                                              | -8                                                                                                        | -10P | -10S | -8                | -10P | -10S |      |
| BYTE0         | # of Bytes Written into Serial Memory at Module Manufacturer | 128 Bytes                                                                                                 |      |      | 80h               |      |      |      |
| BYTE1         | Total # of Bytes of SPD Memory Device                        | 256 Bytes                                                                                                 |      |      | 08h               |      |      |      |
| BYTE2         | Fundamental Memory Type                                      | SDRAM                                                                                                     |      |      | 04h               |      |      |      |
| BYTE3         | # of Row Addresses on This Assembly                          | 12                                                                                                        |      |      | 0Ch               |      |      | 1    |
| BYTE4         | # of Column Addresses on This Assembly                       | 11                                                                                                        |      |      | 0Bh               |      |      |      |
| BYTE5         | # of Module Banks on This Assembly                           | 1 Bank                                                                                                    |      |      | 01h               |      |      |      |
| BYTE6         | Data Width of This Assembly                                  | 72 Bits                                                                                                   |      |      | 48h               |      |      |      |
| BYTE7         | Data Width of This Assembly (Continued)                      | -                                                                                                         |      |      | 00h               |      |      |      |
| BYTE8         | Voltage Interface Standard of This Assembly                  | LVTTL                                                                                                     |      |      | 01h               |      |      |      |
| BYTE9         | SDRAM Cycle Time @ /CAS Latency=3                            | 8ns                                                                                                       | 10ns | 10ns | 80h               | A0h  | A0h  | 9    |
| BYTE10        | Access Time from Clock @ /CAS Latency=3                      | 6ns                                                                                                       | 6ns  | 6ns  | 60h               | 60h  | 60h  |      |
| BYTE11        | DIMM Configuration Type                                      | ECC                                                                                                       |      |      | 02h               |      |      |      |
| BYTE12        | Refresh Rate/Type                                            | 15.625µs<br>/ Self Refresh Supported                                                                      |      |      | 80h               |      |      |      |
| BYTE13        | Primary SDRAM Width                                          | x4                                                                                                        |      |      | 04h               |      |      |      |
| BYTE14        | Error Checking SDRAM Width                                   | x4                                                                                                        |      |      | 04h               |      |      |      |
| BYTE15        | Minimum Clock Delay Back to Back Random Column Address       | tCCD = 1 CLK                                                                                              |      |      | 01h               |      |      |      |
| BYTE16        | Burst Lengths Supported                                      | 1,2,4,8,Full Page                                                                                         |      |      | 8Fh               |      |      | 2    |
| BYTE17        | # of Banks on Each SDRAM Device                              | 4 Banks                                                                                                   |      |      | 04h               |      |      |      |
| BYTE18        | SDRAM Device Attributes, CAS # Latency                       | /CAS Latency=2,3                                                                                          |      |      | 06h               |      |      |      |
| BYTE19        | SDRAM Device Attributes, CS # Latency                        | /CS Latency=0                                                                                             |      |      | 01h               |      |      |      |
| BYTE20        | SDRAM Device Attributes, Write Latency                       | /WE Latency=0                                                                                             |      |      | 01h               |      |      |      |
| BYTE21        | SDRAM Module Attributes                                      | Registered Inputs, with PLL                                                                               |      |      | 16h               |      |      |      |
| BYTE22        | SDRAM Device Attributes, General                             | +/-10% voltage tolerance, Burst Read Single bit Write, Precharge All, Auto Precharge, Early RAS Precharge |      |      | 0Eh               |      |      |      |
| BYTE23        | SDRAM Cycle Time @ /CAS Latency=2                            | 10ns                                                                                                      | 10ns | 12ns | A0h               | A0h  | C0h  | 9    |
| BYTE24        | Access Time from Clock @ /CAS Latency=2                      | 6ns                                                                                                       | 6ns  | 6ns  | 60h               | 60h  | 60h  |      |
| BYTE25        | SDRAM Cycle Time @ /CAS Latency=1                            | -                                                                                                         | -    | -    | 00h               | 00h  | 00h  |      |
| BYTE26        | Access Time from Clock @ /CAS Latency=1                      | -                                                                                                         | -    | -    | 00h               | 00h  | 00h  |      |
| BYTE27        | Minimum Row Precharge Time (tRP)                             | 20ns                                                                                                      | 20ns | 20ns | 14h               | 14h  | 14h  |      |
| BYTE28        | Minimum Row Active to Row Active Delay (tRRD)                | 16ns                                                                                                      | 20ns | 20ns | 10h               | 14h  | 14h  |      |
| BYTE29        | Minimum /RAS to /CAS Delay (tRCD)                            | 20ns                                                                                                      | 20ns | 20ns | 14h               | 14h  | 14h  |      |
| BYTE30        | Minimum /RAS Pulse width (tRAS)                              | 48ns                                                                                                      | 50ns | 50ns | 30h               | 32h  | 32h  |      |
| BYTE31        | Module Bank Density                                          | 256MB                                                                                                     |      |      | 40h               |      |      |      |
| BYTE32        | Command and Address Signal Input Setup Time                  | 2ns                                                                                                       | 2ns  | 2ns  | 20h               | 20h  | 20h  |      |
| BYTE33        | Command and Address Signal Input Hold Time                   | 1ns                                                                                                       | 1ns  | 1ns  | 10h               | 10h  | 10h  |      |
| BYTE34        | Data Signal Input Setup Time                                 | 2ns                                                                                                       | 2ns  | 2ns  | 20h               | 20h  | 20h  |      |
| BYTE35        | Data Signal Input Hold Time                                  | 1ns                                                                                                       | 1ns  | 1ns  | 10h               | 10h  | 10h  |      |
| BYTE36<br>~61 | Superset Information (may be used in future)                 | -                                                                                                         |      |      | 00h               |      |      |      |
| BYTE62        | SPD Revision                                                 | Intel SPD 1.2A                                                                                            |      |      | 12h               |      |      | 3, 8 |
| BYTE63        | Checksum for Bytes 0~62                                      | -                                                                                                         |      |      | 31h               | 57h  | 77h  |      |
| BYTE64        | Manufacturer JEDEC ID Code                                   | Hyundai JEDEC ID                                                                                          |      |      | ADh               |      |      |      |
| BYTE65<br>~71 | ....Manufacturer JEDEC ID Code                               | Unused                                                                                                    |      |      | FFh               |      |      |      |
| BYTE72        | Manufacturing Location                                       | HEI (Korea)<br>HEA (United States)<br>HEU (Europe)                                                        |      |      | 01h<br>02h<br>03h |      |      |      |

Continued

| BYTE<br>NUMBER  | FUNCTION<br>DESCRIBED                              | FUNCTION         |      |      | VALUE |      |      | NOTE |
|-----------------|----------------------------------------------------|------------------|------|------|-------|------|------|------|
|                 |                                                    | -8               | -10P | -10S | -8    | -10P | -10S |      |
| BYTE73          | Manufacturer' s Part Number (Component)            | 7 (SDRAM)        |      |      | 37h   |      |      | 4, 5 |
| BYTE74          | Manufacturer' s Part Number (128Mb based)          | 1                |      |      | 31h   |      |      | 4, 5 |
| BYTE75          | Manufacturer' s Part Number (Voltage Interface)    | V (3.3V, LVTTTL) |      |      | 56h   |      |      | 4, 5 |
| BYTE76          | Manufacturer' s Part Number (Data Width)           | 7                |      |      | 37h   |      |      | 4, 5 |
| BYTE77          | ....Manufacturer' s Part Number (Data Width)       | 5                |      |      | 35h   |      |      | 4, 5 |
| BYTE78          | Manufacturer' s Part Number (Module Type)          | S                |      |      | 53h   |      |      | 4, 5 |
| BYTE79          | Manufacturer' s Part Number (Memory Depth)         | 3                |      |      | 33h   |      |      | 4, 5 |
| BYTE80          | ....Manufacturer' s Part Number (Memory Depth)     | 2                |      |      | 32h   |      |      | 4, 5 |
| BYTE81          | Manufacturer' s Part Number (Refresh)              | 0 (4K Refresh)   |      |      | 30h   |      |      | 4, 5 |
| BYTE82          | Manufacturer' s Part Number (Internal Banks)       | 1 (4 Banks)      |      |      | 31h   |      |      | 4, 5 |
| BYTE83          | Manufacturer' s Part Number (Package Type)         | T (TSOPII)       |      |      | 54h   |      |      | 4, 5 |
| BYTE84          | Manufacturer' s Part Number (Module Type)          | N (x4 based)     |      |      | 4Eh   |      |      | 4, 5 |
| BYTE85          | Manufacturer' s Part Number (Hyphen)               | - (Hyphen)       |      |      | 2Dh   |      |      | 4, 5 |
| BYTE86          | Manufacturer' s Part Number (Min. Cycle Time)      | 8                | 1    | 1    | 38h   | 31h  | 31h  | 4, 5 |
| BYTE87          | ....Manufacturer' s Part Number (Min. Cycle Time)  | Blank            | 0    | 0    | 20h   | 30h  | 30h  |      |
| BYTE88          | ....Manufacturer' s Part Number (Min. Cycle Time)  | Blank            | P    | S    | 20h   | 50h  | 53h  | 4, 5 |
| BYTE89<br>~90   | Manufacturer' s Part Number                        | Blanks           |      |      | 20h   |      |      | 4, 5 |
| BYTE91          | Revision Code (for Component)                      | Process Code     |      |      | -     |      |      | 4, 6 |
| BYTE92          | ....Revision Code (for PCB)                        | Process Code     |      |      | -     |      |      | 4, 6 |
| BYTE93          | Manufacturing Date                                 | Work Week        |      |      | -     |      |      | 3, 6 |
| BYTE94          | ....Manufacturing Date                             | Year             |      |      | -     |      |      | 3, 6 |
| BYTE95<br>~98   | Assembly Serial Number                             | Serial Number    |      |      | -     |      |      | 6    |
| BYTE99<br>~125  | Manufacturer Specific Data (may be used in future) | None             |      |      | 00h   |      |      |      |
| BYTE126         | System Frequency Support                           | 100MHz           |      |      | 64h   |      |      | 7, 8 |
| BYTE127         | Intel Specification Details for 100MHz Support     | Refer to Note7   |      |      | 87h   | 87h  | 85h  | 7, 8 |
| BYTE128<br>~256 | Unused Storage Locations                           | -                |      |      | 00h   |      |      |      |

- Note:** 1. The bank address is excluded.  
2. 1,2,4,8 for Interleave Burst Type  
3. BCD adopted.  
4. ASCII adopted.  
5. Basically HYUNDAI writes Part No. except for `HYM` in Byte 73-90 to use the limited 18 bytes from byte 73 to 90 efficiently.  
6. Not fixed but dependent.  
7. CLK0 connected on the DIMM, TBD junction temp, CL2(3) support, Intel defined Concurrent Auto Precharge support  
8. Refer to Intel SPD Specification Rev.1.2A.

### ABSOLUTE MAXIMUM RATINGS

| PARAMETER                          | SYMBOL    | RATING     | UNIT     |
|------------------------------------|-----------|------------|----------|
| Ambient Temperature                | TA        | 0 ~ 70     | °C       |
| Storage Temperature                | TSTG      | -55 ~ 125  | °C       |
| Voltage on any Pin relative to VSS | VIN, VOUT | -1.0 ~ 4.6 | V        |
| Voltage on VDD relative to VSS     | VDD, VDDQ | -1.0 ~ 4.6 | V        |
| Short Circuit Output Current       | IOS       | 50         | MA       |
| Power Dissipation                  | PD        | 9          | W        |
| Soldering Temperature · Time       | TSOLDER   | 260 · 10   | °C · Sec |

**Note :** Operation at above absolute maximum can adversely affect device reliability.

### DC OPERATING CONDITION

(TA = 0 to 70°C)

| PARAMETER            | SYMBOL | MIN  | TYP. | MAX       | UNIT | NOTE |
|----------------------|--------|------|------|-----------|------|------|
| Power Supply Voltage | VCC    | 3.0  | 3.3  | 3.6       | V    | 1    |
| Input High Voltage   | VIH    | 2.0  | 3.0  | VCC + 0.3 | V    | 1, 2 |
| Input Low Voltage    | VIL    | -0.3 | 0    | 0.8       | V    | 1, 3 |

**Note :** 1. All voltage are referenced to VSS = 0V.  
 2. VIH (max) is acceptable 5.6V AC pulse width with ≤ 3ns of duration.  
 3. VIL (min) is acceptable -2.0V AC pulse width with ≤ 3ns of duration.

### AC OPERATING CONDITION

(TA = 0 to 70°C, VDD = 3.3 ± 0.3V, VSS = 0V)

| PARAMETER                                           | SYMBOL    | VALUE     | UNIT |
|-----------------------------------------------------|-----------|-----------|------|
| AC Input High / Low Level Voltage                   | VIH / VIL | 2.4 / 0.4 | V    |
| Input Timing Measurement Reference Level Voltage    | Vtrip     | 1.4       | V    |
| Input Rise / Fall Time                              | tR / tF   | 1         | ns   |
| Output Timing Measurement Reference Level Voltage   | Voutref   | 1.4       | V    |
| Output Load Capacitance for Access Time Measurement | CL        | *Note     | pF   |

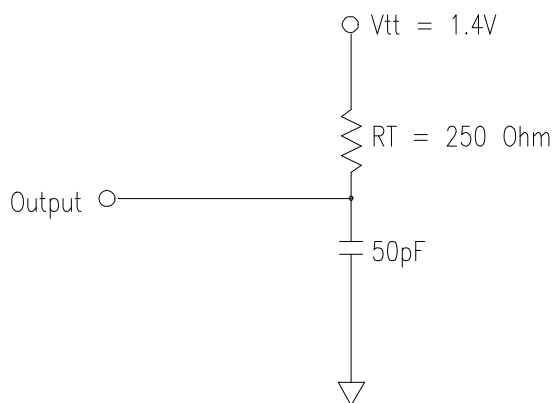
**Note :** \*. Output load to measure access time is equivalent to two TTL gates and one capacitor (50pF).  
 For details, refer to AC/DC output circuit.

### CAPACITANCE

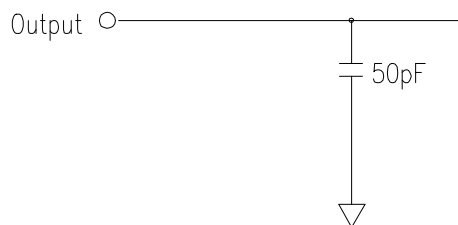
(TA = 25°C, f = 1MHz)

| PARAMETER                     | PIN               | SYMBOL | MIN | MAX | TYP. | UNIT |
|-------------------------------|-------------------|--------|-----|-----|------|------|
| Input Capacitance             | CK0               | CIN1   | -   | 40  | -    | pF   |
|                               | CKE0              | CIN2   | -   | 16  | -    | pF   |
|                               | /S0, /S1          | CIN3   | -   | 16  | -    | pF   |
|                               | A0~A11, BA0, BA1  | CIN4   | -   | 16  | -    | pF   |
|                               | /RAS, /CAS, /WE   | CIN5   | -   | 16  | -    | pF   |
|                               | DQM0~DQM7         | CIN6   | -   | 16  | -    | pF   |
| Data Input/Output Capacitance | DQ0~DQ63, CB0~CB7 | CI/O   | -   | 15  | -    | pF   |

### OUTPUT LOAD CIRCUIT



DC Output Load Circuit



AC Output Load Circuit

### DC CHARACTERISTICS I

(TA = 0 to 70°C, VDD = 3.3 ± 0.3V)

| PARAMETER              | SYMBOL | MIN | MAX | UNIT | NOTE       |
|------------------------|--------|-----|-----|------|------------|
| Input Leakage Current  | ILI    | -10 | 10  | uA   | 1          |
| Output Leakage Current | ILO    | -1  | 1   | uA   | 2          |
| Output High Voltage    | VOH    | 2.4 | -   | V    | IOH = -4mA |
| Output Low Voltage     | VOL    | -   | 0.4 | V    | IOL = +4mA |

**Note :** 1. VIN = 0 to 3.6V. All other pins are not tested under VIN = 0V.  
2. DOUT is disabled. VOUT = 0 to 3.6V.

### DC CHARACTERISTICS II

(TA = 0 to 70°C, VDD = 3.3 ± 0.3V, VSS = 0V)

| PARAMETER                                           | SYMBOL | TEST CONDITION                                                                                                                         |        | SPEED |      |      | UNIT | NOTE |
|-----------------------------------------------------|--------|----------------------------------------------------------------------------------------------------------------------------------------|--------|-------|------|------|------|------|
|                                                     |        |                                                                                                                                        |        | -8    | -10P | -10S |      |      |
| Operating Current                                   | IDD1   | Burst Length = 1, One bank active<br>tRC ≥ tRC(min), IOL = 0mA                                                                         |        | 2480  | 2480 | 2480 | mA   | 1    |
| Precharge Standby Current<br>in Power Down Mode     | IDD2P  | CKE ≤ VIL(max), tCK = min                                                                                                              |        | 356   |      |      | mA   |      |
|                                                     | IDD2PS | CKE ≤ VIL(max), tCK = ∞                                                                                                                |        | 117   |      |      | mA   |      |
| Precharge Standby Current<br>in Non Power Down Mode | IDD2N  | CKE ≥ VIH(min), /CS ≥ VIH(min), tCK = min<br>Input signals are changed one time during<br>2clks. All other pins ≥ VDD – 0.2V or ≤ 0.2V |        | 760   |      |      | mA   |      |
|                                                     | IDD2NS | CKE ≥ VIH(max), tCK = ∞<br>Input signals are stable.                                                                                   |        | 270   |      |      | mA   |      |
| Active Standby Current<br>in Power Down Mode        | IDD3P  | CKE ≤ VIL(max), tCK = min                                                                                                              |        | 446   |      |      | mA   |      |
|                                                     | IDD3PS | CKE ≤ VIL(max), tCK = ∞                                                                                                                |        | 216   |      |      | mA   |      |
| Active Standby Current<br>in Non Power Down Mode    | IDD3N  | CKE ≥ VIH(min), /CS ≥ VIH(min), tCK = min<br>Input signals are changed one time during<br>2clks. All other pins ≥ VDD – 0.2V or ≤ 0.2V |        | 1120  |      |      | mA   |      |
|                                                     | IDD3NS | CKE ≥ VIH(max), tCK = ∞<br>Input signals are stable.                                                                                   |        | 810   |      |      | mA   |      |
| Burst Mode Operating<br>Current                     | IDD4   | tCK ≥ tCK(min), IOL = 0mA<br>All banks active                                                                                          | CL = 3 | 2410  | 2480 | 2480 | mA   | 1    |
|                                                     |        |                                                                                                                                        | CL = 2 | 2480  | 2480 | 2300 |      |      |
| Auto Refresh Current                                | IDD5   | tRRC ≥ tRRC(min), All banks active                                                                                                     |        | 5060  |      |      | mA   | 2    |
| Self Refresh Current                                | IDD6   | CKE ≤ 0.2V                                                                                                                             |        | 276   |      |      | mA   |      |

**Note :** 1. IDD1 and IDD4 depend on output loading and cycle rates. Specified values are measured with the output open.  
2. Min. of tRRC (Refresh /RAS cycle time) is shown at AC CHARACTERISTICS II.

### AC CHARACTERISTICS I

(AC operating conditions unless otherwise noted)

| PARAMETER                         |                  | SYMBOL | -8  |      | -10P |      | -10S |      | UNIT | NOTE |
|-----------------------------------|------------------|--------|-----|------|------|------|------|------|------|------|
|                                   |                  |        | MIN | MAX  | MIN  | MAX  | MIN  | MAX  |      |      |
| System Clock Cycle Time           | /CAS Latency = 3 | tCK3   | 8   | 1000 | 10   | 1000 | 10   | 1000 | ns   | 1    |
|                                   | /CAS Latency = 2 | tCK2   | 10  |      | 10   |      | 12   |      |      |      |
| Clock High Pulse Width            |                  | tCHW   | 3   | -    | 3    | -    | 3    | -    | ns   | 2    |
| Clock Low Pulse Width             |                  | tCLW   | 3   | -    | 3    | -    | 3    | -    | ns   | 2    |
| Access Time from Clock            | /CAS Latency = 3 | tAC3   | -   | 6    | -    | 6    | -    | 6    | ns   | 3    |
|                                   | /CAS Latency = 2 | tAC2   | -   | 6    | -    | 6    | -    | 6    |      |      |
| Data-Out Hold Time                |                  | tOH    | 3   | -    | 3    | -    | 3    | -    | ns   |      |
| Data-Input Setup Time             |                  | tDS    | 2   | -    | 2    | -    | 2    | -    | ns   | 2    |
| Data-Input Hold Time              |                  | tDH    | 1   | -    | 1    | -    | 1    | -    | ns   | 2    |
| Address Setup Time                |                  | tAS    | 2   | -    | 2    | -    | 2    | -    | ns   | 2    |
| Address Hold Time                 |                  | tAH    | 1   | -    | 1    | -    | 1    | -    | ns   | 2    |
| CKE Setup Time                    |                  | tCKS   | 2   | -    | 2    | -    | 2    | -    | ns   | 2    |
| CKE Hold Time                     |                  | tCKH   | 1   | -    | 1    | -    | 1    | -    | ns   | 2    |
| Command Setup Time                |                  | tCS    | 2   | -    | 2    | -    | 2    | -    | ns   | 2    |
| Command Hold Time                 |                  | tCH    | 1   | -    | 1    | -    | 1    | -    | ns   | 2    |
| CLK to Data Output in Low-Z time  |                  | tOLZ   | 1   | -    | 1    | -    | 1    | -    | ns   |      |
| CLK to Data Output in High-Z time | /CAS Latency = 3 | tOHZ3  | 3   | 6    | 3    | 6    | 3    | 6    | ns   |      |
|                                   | /CAS Latency = 2 | tOHZ2  | 3   | 6    | 3    | 6    | 3    | 6    |      |      |

**Note :**

1. In a registered DIMM, data is delayed an additional clock cycle due to the register (that is, Device CL + 1 = DIMM CL).
2. Assume tR / tF (input rise and fall time ) is 1ns. If tR & tF > 1ns, then [(tR+tF)/2-1]ns should be added to the parameter
3. Access times to be measured with input signals of 1v/ns edge rate, from 0.8v to 2.0v.  
If tR > 1ns, then (tR/2-0.5)ns should be added to the parameter

### AC CHARACTERISTICS II

| PARAMETER                      |                  | SYMBOL | -8  |      | -10P |      | -10S |      | UNIT | NOTE |
|--------------------------------|------------------|--------|-----|------|------|------|------|------|------|------|
|                                |                  |        | MIN | MAX  | MIN  | MAX  | MIN  | MAX  |      |      |
| /RAS Cycle Time                | Operation        | tRC    | 68  | -    | 70   | -    | 70   | -    | ns   |      |
|                                | Auto Refresh     | tRRC   | 68  |      | 70   |      | 70   |      |      |      |
| /RAS to /CAS Delay             |                  | tRCD   | 20  | -    | 20   | -    | 20   | -    | ns   |      |
| /RAS Active Time               |                  | tRAS   | 48  | 100K | 50   | 100K | 50   | 100K | ns   |      |
| /RAS Precharge Time            |                  | tRP    | 20  | -    | 20   | -    | 20   | -    | ns   |      |
| /RAS to /RAS Bank Active Delay |                  | tRRD   | 16  | -    | 20   | -    | 20   | -    | ns   |      |
| /CAS to /CAS Delay             |                  | tCCD   | 1   | -    | 1    | -    | 1    | -    | CLK  |      |
| Write Command to Data-in Delay |                  | tWTL   | 1   | -    | 1    | -    | 1    | -    | CLK  | 1    |
| Data-in to Precharge Command   |                  | tDPL   | 0   | -    | 0    | -    | 0    | -    | CLK  | 1    |
| Data-in to Active Command      |                  | tDAL   | 3   | -    | 2    | -    | 2    | -    | CLK  | 1    |
| DQM to Data-out Hi-Z           |                  | tDQZ   | 3   | -    | 3    | -    | 3    | -    | CLK  | 1    |
| DQM to Data-in Mask            |                  | tDQM   | 0   | -    | 0    | -    | 0    | -    | CLK  |      |
| MRS to New Command             |                  | tMRD   | 2   | -    | 2    | -    | 2    | -    | CLK  |      |
| Precharge to Data Output Hi-Z  | /CAS Latency = 3 | tPROZ3 | 4   | -    | 4    | -    | 4    | -    | CLK  | 1    |
|                                | /CAS Latency = 2 | tPROZ2 | 3   | -    | 3    | -    | 3    | -    |      |      |
| Power Down Exit Time           |                  | tPDE   | 1   | -    | 1    | -    | 1    | -    | CLK  |      |
| Self Refresh Exit Time         |                  | tSRE   | 1   | -    | 1    | -    | 1    | -    | CLK  | 2    |
| Refresh Time                   |                  | tREF   | -   | 64   | -    | 64   | -    | 64   | ms   |      |

**Note :** 1. Timing delay due to the register is considered in a registered DIMM.  
 2. A new command can be given tRRC after self refresh exit.

### OPERATING OPTION TABLE

#### HYM71V75S3201TN-8

|                 | /CAS<br>LATENCY | tRCD  | tRAS  | tRC   | tRP   | tAC | tOH |
|-----------------|-----------------|-------|-------|-------|-------|-----|-----|
| 125MHz (8.0ns)  | 3CLKS           | 3CLKS | 6CLKS | 9CLKS | 3CLKS | 6ns | 3ns |
| 100MHz (10.0ns) | 2CLKS           | 2CLKS | 5CLKS | 7CLKS | 2CLKS | 6ns | 3ns |
| 83MHz (12.0ns)  | 2CLKS           | 2CLKS | 4CLKS | 6CLKS | 2CLKS | 6ns | 3ns |

#### HYM71V75S3201TN-10P

|                 | /CAS<br>LATENCY | tRCD  | tRAS  | tRC   | tRP   | tAC | tOH |
|-----------------|-----------------|-------|-------|-------|-------|-----|-----|
| 100MHz (10.0ns) | 2CLKS           | 2CLKS | 5CLKS | 7CLKS | 2CLKS | 6ns | 3ns |
| 83MHz (12.0ns)  | 2CLKS           | 2CLKS | 5CLKS | 7CLKS | 2CLKS | 6ns | 3ns |
| 66MHz (15.0ns)  | 2CLKS           | 2CLKS | 4CLKS | 6CLKS | 2CLKS | 6ns | 3ns |

#### HYM71V75S3201TN-10S

|                 | /CAS<br>LATENCY | tRCD  | tRAS  | tRC   | tRP   | tAC | tOH |
|-----------------|-----------------|-------|-------|-------|-------|-----|-----|
| 100MHz (10.0ns) | 3CLKS           | 2CLKS | 5CLKS | 7CLKS | 2CLKS | 6ns | 3ns |
| 83MHz (12.0ns)  | 2CLKS           | 2CLKS | 5CLKS | 7CLKS | 2CLKS | 6ns | 3ns |
| 66MHz (15.0ns)  | 2CLKS           | 2CLKS | 4CLKS | 6CLKS | 2CLKS | 6ns | 3ns |

**Note :** DIMM /CAS Latency = Device CL + 1 (Registered mode)

### COMMAND TRUTH TABLE

|                          |       | CKEn-1 | CKEn | /CS | /RAS | /CAS | /WE | DQM | ADDR    | A10/<br>AP | BA | NOTE |
|--------------------------|-------|--------|------|-----|------|------|-----|-----|---------|------------|----|------|
| Mode Register Set        |       | H      | X    | L   | L    | L    | L   | X   | OP code |            |    |      |
| No Operation             |       | H      | X    | H   | X    | X    | X   | X   | X       |            |    |      |
|                          |       |        |      | L   | H    | H    | H   |     |         |            |    |      |
| Bank Active              |       | H      | X    | L   | L    | H    | H   | X   | RA      |            | V  |      |
| Read                     |       | H      | X    | L   | H    | L    | H   | X   | CA      | L          | V  |      |
| Read with Autoprecharge  |       |        |      |     |      |      |     |     |         | H          |    |      |
| Write                    |       | H      | X    | L   | H    | L    | L   | X   | CA      | L          | V  |      |
| Write with Autoprecharge |       |        |      |     |      |      |     |     |         | H          |    |      |
| Precharge All Banks      |       | H      | X    | L   | L    | H    | L   | X   | X       | H          | X  |      |
| Precharge Selected Bank  |       |        |      |     |      |      |     |     |         | L          | V  |      |
| Burst Stop               |       | H      | X    | L   | H    | H    | L   | X   | X       |            |    |      |
| DQM                      |       | H      | X    |     |      |      |     | V   | X       |            |    |      |
| Auto Refresh             |       | H      | H    | L   | L    | L    | H   | X   | X       |            |    |      |
| Self Refresh             | Entry | H      | L    | L   | L    | L    | H   | X   | X       |            |    | 1    |
|                          | Exit  | L      | H    | H   | X    | X    | X   | X   |         |            |    |      |
| Precharge<br>Power Down  | Entry | H      | L    | H   | X    | X    | X   | X   | X       |            |    |      |
|                          |       |        |      | L   | H    | H    | H   |     |         |            |    |      |
|                          | Exit  | L      | H    | H   | X    | X    | X   | X   |         |            |    |      |
|                          |       |        |      | L   | H    | H    | H   |     |         |            |    |      |
| Clock Suspend            | Entry | H      | L    | H   | X    | X    | X   | X   | X       |            |    |      |
|                          |       |        |      | L   | V    | V    | V   |     |         |            |    |      |
|                          | Exit  | L      | H    | X   |      |      |     | X   |         |            |    |      |

**Note :** 1. Existing Self Refresh occurs by asynchronously bringing CKE from low to high.

2. X = Don't care, H = Logic High, L = logic Low, BA = Bank Address, CA = Column Address, OP code = Operand code, NOP = No operation

## PACKAGE DIMENSIONS

