BURR-BROWN®

DAC870/883B SERIES

MODEL NUMBERS:

DAC870V/883B	DAC870U/883B
DAC870VL/883B	DAC870UL/883B
DAC870V	DAC870U
DAC870VL	DAC870UL

REVISION B
JANUARY, 1989

12-Bit −55°C to +125°C Military DIGITAL-TO-ANALOG CONVERTER

FEATURES

- HI-REL MANUFACTURE
- COMPLETELY SPECIFIED, −55°C to +125°C
- ACCURATE
  - ±1/2LSB max Linearity, over temperature
  - ±25ppm/°C max Gain Drift
  - ±0.3% Total Error, over temperature
  - Monotonic, over temperature
- MIL-STD-883 SCREENING
- DAC87 PIN-COMPATIBLE
- COMPLETE—INTERNAL REFERENCE AND OUTPUT AMPLIFIER

DESCRIPTION

The DAC870 Series is a high performance, 12-bit, TTL-compatible, −55°C to +125°C digital-to-analog converter in either a 24-pin ceramic side-brazed package or a 28-terminal leadless chip carrier, and it is manufactured on a separate Hi-Rel production line. It is pin-compatible with DAC87 converters and has five user-selected output ranges. Each DAC is a complete device with an internal output amplifier and an ultra-stable reference.

The DAC870 Series is designed for high accuracy, wide temperature applications. The total accuracy without external trim adjustments is ±0.25% of FSR, decreasing to only ±0.4% of FSR over −55°C to +125°C. With external offset and gain trim adjustments at +25°C, the total accuracy is less than ±0.3% of FSR over −55°C to +125°C. Gain drift is less than 25ppm/°C. Linearity error, contributed mostly by the internal current switches and resistive ladder, is reduced by laser trimming to less than ±1/2LSB over temperature. Differential linearity is less than ±1LSB over temperature, thereby guaranteeing monotonicity from −55°C to +125°C.

There are two electrical performance grades and two product assurance levels, allowing a wide application/budget choice. The DAC870V model/grade features excellent performance from −55°C to +125°C and finds wide military, aerospace, and industrial applications. The DAC870U model/grade features excellent performance from −25°C to +85°C, and guarantees specifications from −55°C to +125°C. Applications include test equipment, shipboard, ground support, and shirt-sleeve environments where operation is between −25°C and +85°C but full temperature operation must be assured.

Two product assurance levels are available: standard; /883B (100% screened, plus PDA = 5%, plus groups A and B testing on each inspection lot, plus Groups C and D performed as required by MIL-STD-883. See paragraph 1.2.2 for more details. Each device is manufactured in a Hi-Rel environment with clean room conditions which assures "built-in" quality.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-511B

DETAILED SPECIFICATION
MICROCIRCUITS, LINEAR
DIGITAL-TO-ANALOG CONVERTER
MONOLITHIC, SILICON

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a 12-bit voltage output digital-to-analog converter hybrid microcircuit.

1.2 Part Number. The complete part number is as shown below.

DAC870	V	L	/883B
Basic model number	Grade (see 1.2.1)	Package (see 1.2.3)	Hi-Rel product designator (see 1.2.2)

1.2.1 Device type. The device is a single, 12-bit, voltage output digital-to-analog converter. The input coding is complementary binary. The device may be externally pin-connected for either Complementary Straight Binary (CSB) or Complementary Offset Binary (COB) coding (see Tables V and VI).

There are two electrical performance grades. The V grade designation is the premium grade and features specifications and tests from −55°C to +125°C. The U grade designation features specifications and tests from −25°C to +85°C and operation from −55°C to +125°C.

Electrical specifications are shown in Table I; electrical tests are shown in Tables II and III.

1.2.2 Device class. The Hi-Rel product designator portion of the part number distinguishes the product assurance levels available as follows:

Hi-Rel product designator	Requirements
/883B	Standard model plus 100% MIL-STD-883 class B screening, with 5% PDA, plus quality conformance inspection (QCI) consisting of Groups A and B performed on each inspection lot, plus Groups C and D performed as required by MIL-STD-883.
(NONE)	Standard model including 100% electrical testing.

1.2.3 Case outline. Two case outlines are available.

1.2.3.1 24-pin ceramic side-brazed (DIP). No package identifier is utilized to specify the 24-pin ceramic side-brazed package, which is MIL-M-38510, Appendix C, designator D-3, configuration 3. Figure 1 depicts the case outline for this package type.

1.2.3.2 28-terminal leadless chip carrier (LCC). The "L" package identifier is utilized to specify the 28-terminal square leadless chip carrier package, which is MIL-M-38510, Appendix C, designator C-4. Figure 1 depicts the case outline for this configuration.

1.2.4 Absolute maximum ratings.

Supply voltage, V_{CC}	±20VDC
Supply voltage, V_{DD}	0VDC to +18VDC
Data input voltage	−1VDC to +7VDC
Output short circuit duration	Continuous to ground
Storage temperature range	−65°C to +165°C
Lead temperature (soldering, 10sec)	+300°C
Junction temperature	T_J = +165°C

1.2.5 Recommended operating conditions.

Supply voltage range	V_{CC}: ±14.5VDC to ±15.5VDC V_{DD}: ±4.75VDC to +5.25VDC
Ambient temperature range	−55°C to +125°C

1.2.6 Power and thermal characteristics.

Package	Case outline	Maximum allowable power dissipation	Maximum θ J-C
24-lead DIP	Figure 1	850mW	48°C/W
28-terminal LCC	Figure 1	950mW	42°C/W

2. APPLICABLE DOCUMENTS

2.1 The following documents form a part of this specification to the extent specified herein.

SPECIFICATION
MILITARY
MIL-M-38510 - Microcircuits, General Specification for.

STANDARD
MILITARY
MIL-STD-883 - Test Methods and Procedures for Microcircuits.

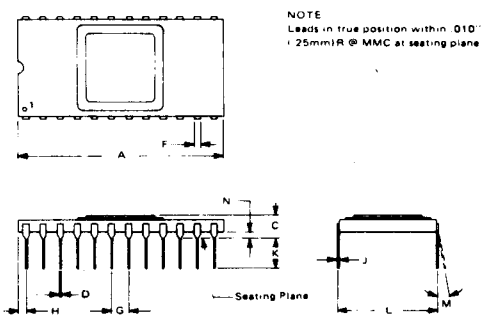
3. REQUIREMENTS

3.1 General. Burr-Brown uses production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with this specification.

3.1.1 Detail specifications. The individual item requirements are specified herein. In the event of conflicting requirements the order of precedence will be the purchase order, this specification, and then the reference documents.

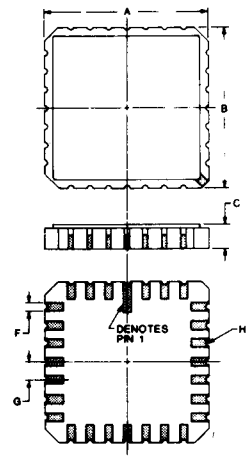
3.2 Design, construction, and physical dimensions.

3.2.1 Package, metals, and other materials. The packages, metal surfaces, and other materials are in accordance with MIL-M-38510.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.185	1.215	30.10	30.86
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	—	10°		10°
N	.025	.060	0.64	1.52

(a) 24-pin side braze; package ID: (none)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.442	.458	11.23	11.63
B	.442	.458	11.23	11.63
C	.064	.100	1.63	2.54
F	.022	.028	0.56	0.71
G	.050 BASIC		1.27 BASIC	
H	.008R TYP.		0.20R TYP.	

(b) 28-terminal LCC; package ID: "L"

FIGURE 1. Case Outlines.

3.2.2 Design documentation. The design documentation is in accordance with MIL-M-38510.

3.2.3 Internal conductors and internal lead wires. The internal conductors and internal lead wires are in accordance with MIL-M-38510.

3.2.4 Lead material and finish. The lead material and finish is in accordance with MIL-M-38510 and is solderable per MIL-STD-883, method 2003.

3.2.5 Die thickness. The die thickness is in accordance with MIL-M-38510.

3.2.6 Physical dimensions. The physical dimensions are in accordance with paragraph 1.2.3 herein.

3.2.7 Circuit diagram and terminal connections. The circuit diagram and terminal connections for the ceramic side-brazed package are shown in Figure 2 and the circuit diagram and terminal connections for the leadless chip carrier package are shown in Figure 3.

3.2.8 Glassivation. The microcircuit dice are glassivated.

3.3 Electrical performance characteristics. The electrical performance characteristics are specified in Table I and apply over the full operating ambient temperature range of −55°C to +125°C unless otherwise specified.

3.3.1 Offset and gain error adjustment. The DAC is capable of being externally adjusted to zero offset error and to zero gain error using the circuits in Figure 4. See applications information paragraph 7.3.

3.3.2 Input coding. The input coding is complementary binary. The digital input code to yield the corresponding output voltage for the various output ranges is specified in Table IV.

3.3.3 Output range. The output range is specified in Table VI when externally connected as shown therein.

3.4 Electrical tests. Electrical tests are shown in Table II. The subgroups of Table III which constitute the minimum electrical tests for screening, qualification, and quality conformance, are shown in Table II.

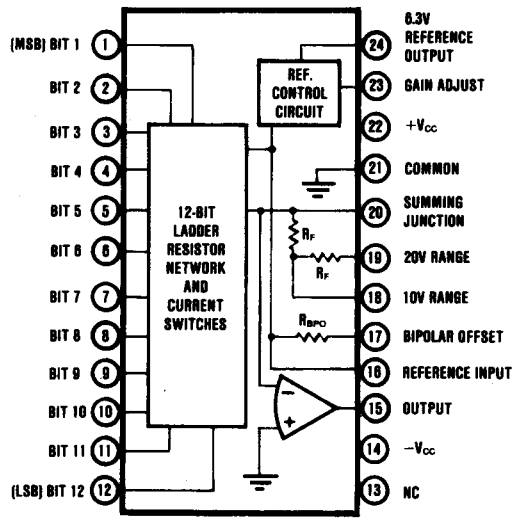


FIGURE 2. Terminal Connections (24-pin Ceramic Side Braze).

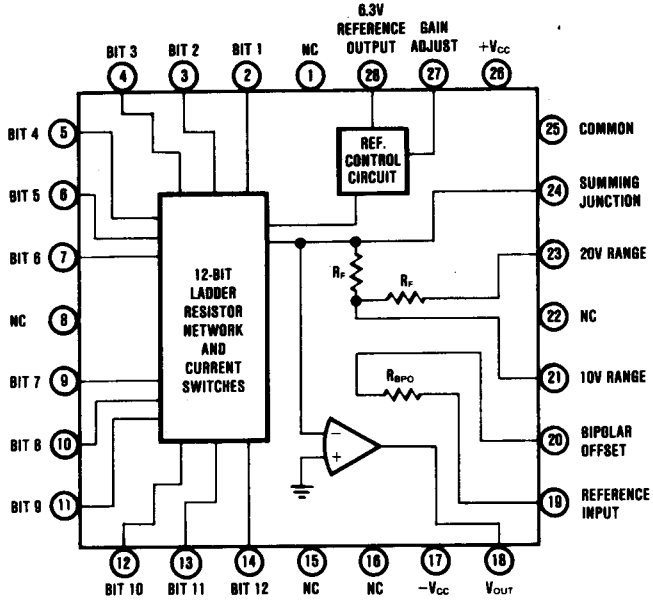
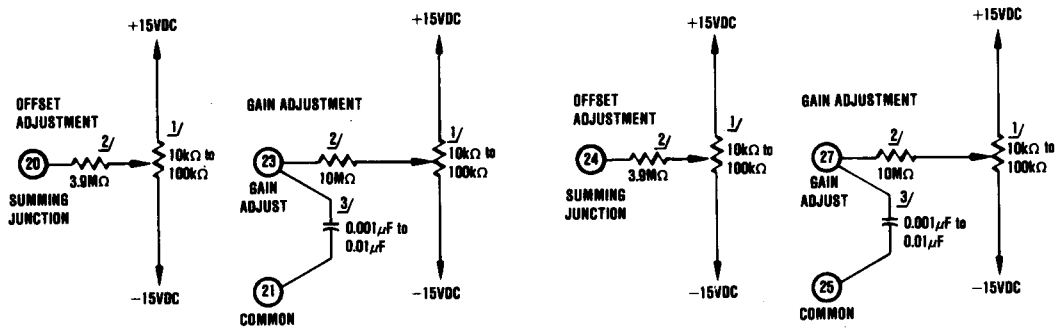


FIGURE 3. Terminal Connections (28-terminal LCC).



1/ ≤100ppm/°C.
2/ ±20% carbon composition or better. Locate close to the DAC870 to prevent noise pickup.
3/ Ceramic.

FIGURE 4. Offset and Gain Error Adjustment Circuits.

TABLE I. Electrical Performance Characteristics.

CHARACTERISTICS	CONDITIONS [1]	LIMITS						UNITS [2]
		DAC870V/883B DAC870V	DAC870VL/883B DAC870VL		DAC870U/883B DAC870U	DAC870UL/883B DAC870UL		
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION		12			12			Bits
DIGITAL INPUTS								
Input voltage: Logic "1"	$T_A = +25°C$	2.0		5.5	•		•	V
	$-55°C \le T_A \le +125°C$	2.4		5.5	•		•	V
Logic "0"	$T_A = +25°C$	0		0.8	•		•	V
	$-55°C \le T_A \le +125°C$	0		0.4	•		•	V
Input Current: Logic "1"	$V_{IN} = 2.4V$			+40			•	µA
Logic "0"	$V_{IN} = 0.4V$	−1.6		0	•		•	mA
ACCURACY								
Total error, untrimmed [3]: Unipolar	$T_A = +25°C$			±0.25			•	% of FSR
	$-25°C \le T_A \le +85°C$						±0.25	% of FSR
	$-55°C \le T_A \le +125°C$			±0.40				% of FSR
Bipolar	$T_A = +25°C$			±0.25			•	% of FSR
	$-25°C \le T_A \le +85°C$						±0.25	% of FSR
	$-55°C \le T_A \le +125°C$			±0.40				% of FSR
Total error, trimmed [3,4]: Unipolar	$T_A = +25°C$		±0.006	±0.0122		•	•	% of FSR
	$-25°C \le T_A \le +85°C$						±0.15	% of FSR
	$-55°C \le T_A \le +125°C$			±0.30				% of FSR
Bipolar	$T_A = +25°C$		±0.006	±0.0122		•	•	% of FSR
	$-25°C \le T_A \le +85°C$						±0.15	% of FSR
	$-55°C \le T_A \le +125°C$			±0.30				% of FSR
Linearity error	$T_A = +25°C$		±0.25	±0.50		•	•	LSB
	$-25°C \le T_A \le +85°C$						±0.50	LSB
	$-55°C \le T_A \le +125°C$			±0.50			±3	LSB
Differential linearity error [5]	$T_A = +25°C$		±0.50	±0.75		•	•	LSB
	$-25°C \le T_A \le +85°C$						±1.0	LSB
	$-55°C \le T_A \le +125°C$			±1.0			±3	LSB
Monotonicity temperature range [5]		−55		+125	−25		+85	°C
Offset error [6]: Unipolar [7]	$T_A = +25°C$			±0.10			•	% of FSR
	$-25°C \le T_A \le +85°C$						±0.118	% of FSR
	$-55°C \le T_A \le +125°C$			±0.15				% of FSR
Bipolar [7]	$T_A = +25°C$			±0.10			•	% of FSR
	$-25°C \le T_A \le +85°C$						±0.15	% of FSR
	$-55°C \le T_A \le +125°C$			±0.15				% of FSR
Offset temperature sensitivity [7]: Unipolar	−25°C to +85°C						±3	ppm of FSR/°C
	−55°C to +125°C			±3				ppm of FSR/°C
Bipolar	−25°C to +85°C						±15	ppm of FSR/°C
	−55°C to +125°C			±15			±45	ppm of FSR/°C
Gain error [6,8]: Unipolar [7]	$T_A = +25°C$			±0.15			•	% of FSR
	$-25°C \le T_A \le +85°C$						±0.20	% of FSR
	$-55°C \le T_A \le +125°C$			±0.25				% of FSR
Bipolar [7]	$T_A = +25°C$			±0.15			•	% of FSR
	$-25°C \le T_A \le +85°C$						±0.20	% of FSR
	$-55°C \le T_A \le +125°C$			±0.25				% of FSR
Gain temperature sensitivity [7]: Unipolar	−25°C to +85°C						±20	ppm/°C
	−55°C to +125°C			±25				ppm/°C
Bipolar	−25°C to +85°C						±20	ppm/°C
	−55°C to +125°C			±25			±75	ppm/°C
Gain adjustment range		0.15			•			% of FSR
DYNAMIC CHARACTERISTICS								
Slew rate		10			•			V/µsec
Settling time	ΔV_O = 20V to ±1/2LSB		5	7		•	•	µsec
	ΔV_O = 10V to ±1/2LSB		3	6		•	•	µsec
	ΔV_O = 1LSB to ±1/2LSB		1.5	3		•	•	µsec
ANALOG OUTPUT								
Output voltage range [9]				±10			•	V
Output current [10]		±5			•			mA
Output resistance, DC			0.05	0.2		•	•	Ω
Output short circuit current	$T_A = +25°C$	±5		±40	•		•	mA

TABLE I. Electrical Performance Characteristics (cont).

CHARACTERISTICS	CONDITIONS 1/	LIMITS DAC870V/883B DAC870V MIN	LIMITS DAC870V/883B DAC870VL/883B DAC870VL TYP	LIMITS DAC870V/883B DAC870VL/883B DAC870VL MAX	LIMITS DAC870U/883B DAC870U MIN	LIMITS DAC870U/883B DAC870UL/883B DAC870UL TYP	LIMITS DAC870U/883B DAC870UL/883B DAC870UL MAX	UNITS 2
INTERNAL REFERENCE								
Internal reference voltage (V_R)		±6.23	±6.3	±6.37	*	*	*	V
Internal reference temperature sensitivity	−25°C to +85°C						±20	ppm of V_R/°C
	−55°C to +125°C			±25				ppm of V_R/°C
Output current from internal reference	for specified V_R	1.5			*			mA
POWER SUPPLY								
Power supply range: $+V_{CC}$		+13.5	+15	+16.5	*	*	*	V
$-V_{CC}$		−13.5	−15	−16.5	*	*	*	V
Power supply sensitivity: $\pm V_{CC}$	$\pm V_{CC}$ = 15V ±0.5V		±0.002	±0.004		*	*	% of FSR/%V_{CC}
Power supply current (quiescent): $+V_{CC}$	$-55°C \le T_A \le +125°C$			+30			*	mA
$-V_{CC}$				-30			*	mA
TEMPERATURE RANGE								
Operating		−55		+125	*		*	°C
Storage		−65		+150	*		*	°C

* Specification same as DAC870V

NOTES:

1/ $\pm V_{CC}$ = 15V, V_{DD} = 5V, $-55°C \le T_A \le +125°C$, unless otherwise specified.

2/ FSR = Full Scale Range (Example: The FSR is 20V for ±10V range, 10V for ±5V range, and 10V for 0 to +10V range.) LSB = Least Significant Bit.

3/ Total error includes all errors at any fixed power supply voltage within the recommended supply voltage range, including the internal reference, linearity error, offset error, and gain error.

4/ Offset and gain externally trimmed to zero error at T_A = +25°C.

5/ Monotonicity is assured by testing differential linearity to ±1LSB maximum.

6/ Externally adjustable to zero.

7/ The reference error is included.

8/ The offset error is specified separately and is not included herein.

9/ The output voltage range is determined by external conditions (see Table VI).

10/ Limit is assured by testing output resistance where $R_{LOAD} = 2k\Omega$.

11/ Power dissipation is an additional 100mW, when V_{DD} is operated at +15V.

TABLE II. Electrical Test Requirements.

(The individual tests within the subgroups appear in Table III)

Models / MIL-STD-883 test requirements (hybrid class)	DAC870V/883B DAC870VL/883B DAC870V DAC 870VL	DAC870U/883B DAC870UL/883B DAC70U DAC870UL
	Subgroups (see Table III)	
Interim electrical parameters (preburn-in) (method 5004)	1	1
Final electrical test parameters (method 5004)	1*, 2, 3	1, 2, 2U, 3, 3U
Group A test requirements (method 5005) 1/	1, 2, 3, 4	1, 2, 2U, 3, 3U
Group C end point electrical parameters (method 5005) 1/	1	1

*PDA applies to subgroup 1 (see 4.3.d)

1/Applies to /883B models only.

3.5 Marking. Marking is in accordance with MIL-M-38510. The following marking is placed on each microcircuit as a minimum:

a. Part number (see paragraph 1.2)
b. Inspection lot identification code 1/
c. Manufacturer's identification (BURR-BROWN®)
d. Manufacturer's designating symbol (CEBS)
e. Country of origin

3.6 Workmanship. These microcircuits are manufactured, processed, and tested in a workmanlike manner. Workmanship is in accordance with good engineering practices, workmanlike instructions, inspection and test procedures and training, prepared in fulfillment of Burr-Brown's product assurance program.

3.6.1 Rework provisions. Rework provisions, including rebonding for the /883B Hi-Rel product designation, are in accordance with MIL-M-38510.

1/ A 4-digit code, indicating year and week of seal, and a 4- or 5-digit lot identifier are marked on each unit.

3.7 Traceability. Traceability for the /883B product designation is in accordance with MIL-M-38510. Each microcircuit is traceable to the production lot and to the component vendor's component lot.

3.8 Product and process change. Burr-Brown will not implement any major change to the design, materials, construction, or manufacturing process which may affect the performance, quality or interchangeability of the microcircuit without full or partial requalification.

3.9 Screening. Screening for the /883B Hi-Rel product designation, is in accordance with MIL-STD-883, method 5004, class B, except as modified in paragraph 4.3 herein.

Screening for the standard model includes Burr-Brown QC4118 internal visual inspection, stabilization bake, fine leak, gross leak, constant acceleration (condition E), temperature cycle (condition C), and external visual per MIL-STD-883, method 2009.

For the /883B Hi-Rel product designation, all microcircuits will have passed the screening requirements prior to qualification or quality conformance inspection.

3.10 Qualification. Qualification is not required. See paragraph 4.2 herein.

3.11 Quality conformance inspection. Quality conformance inspection for the /883B Hi-Rel product designation, is in accordance with MIL-M-38510, except as modified in paragraph 4.4 herein. The microcircuit inspection lot will have passed quality conformance inspection prior to microcircuit delivery.

TABLE III. Group A Inspection.

SUBGROUP	PARAMETERS	TEST CIRCUIT FIGURE	CONDITIONS [1]	LIMITS DAC870 "V" Grade MIN	LIMITS DAC870 "V" Grade MAX	LIMITS DAC870 "U" Grade MIN	LIMITS DAC870 "U" Grade MAX	UNITS
1	Offset error, bipolar	5	±10V range (ideal value = −10.000V)		±20		*	mV
T_A = +25°C	Gain error, bipolar	5	±10V range (ideal value = +9.995117V) [2]		±30		*	mV
	Linearity error, bipolar	5	±10V range [3,4]					
			For + bit errors		+2.44		*	mV
			For − bit errors		−2.44		*	mV
	Differential linearity error, bipolar	5	±10V range [4,5]		±3.66		*	mV
	Total error, untrimmed, bipolar	5			±50		*	mV
	Total error, trimmed, bipolar				—		—	
	Internal reference voltage	5		+6.23	+6.37	*	*	V
	Input voltage [6]	—	Logic "1", all inputs, V_{in} = 5.0VDC to 2.0VDC, measure ΔV_O		±4.0		±4.0	mV
		—	Logic "0", all inputs, V_{in} = 0VDC to 0.8VDC, measure ΔV_O		±4.0		±4.0	mV
	Input current	—	Logic "1", each input, V_{in} = +2.4VDC		+40		*	µA
		—	Logic "0", each input, V_{in} = +0.4VDC	−1.6	0	*	*	mA
	Power supply current	5	No load $+V_{CC}$		30		*	mA
		5	No load $-V_{CC}$		30		*	
	Output resistance	5	$R_o = \frac{(V_O \text{ no load}) - (V_O \text{ 2k}\Omega \text{ load})^*}{5\text{mA}}$		0.2		*	Ω
	Output short circuit current	—	R_{load} = 1Ω, V_O = +FS and −FS	±5	±40	*	*	mA
	Power supply sensitivity	5	±10V range, V_O = +FS, ΔV_{CC} = +0.5V and −0.5V		±2.0		*	mV
	Gain adjustment range	4	±10V range	±30		*		mV
	Offset error, unipolar	5	0 to +10V range (ideal value = 0.00V)		±10		*	mV
	Gain error, unipolar	5	0 to +10V range (ideal value = +9.997559V) [2]		±15		*	mV
	Total error, untrimmed, unipolar	5	0 to +10V range		±25		*	mV
2	Offset error, bipolar (V_{OE})	5	±10V range (ideal value =−10.000V)		±30			mV
T_A = +125°C	Gain error, bipolar (G_E)	5	±10V range (ideal value = +9.995117V) [2]		±50			mV
	Offset temperature sensitivity, Bipolar	—	±10V range, $\frac{\Delta V_{OE}}{\Delta T} = \frac{V_{OE125} - V_{OE25}}{100°C}$		±0.30		±9.0	mV/°C
	Gain temperature sensitivity, Bipolar	—	±10V range, $\frac{\Delta G_E}{\Delta T} = \frac{G_{E125} - G_{E25}}{100°C}$		±0.50		±1.50	mV/°C
	Linearity error, bipolar	5	±10V range, [3,4]					
			For + bit errors		+2.44		+14.64	mV
			For − bit errors		−2.44		−14.64	mV
	Differential linearity error, bipolar	5	±10V range [4,5]		±4.88		±14.64	mV
	Total error, untrimmed, bipolar	5	±10V range		±80			mV
	Total error, trimmed, bipolar	5	±10V range [7]		±60			mV
	Internal reference voltage	5		+6.23	+6.37			V
	Internal reference temperature sensitivity	—	$\frac{\Delta V_R}{\Delta T} = \frac{V_{R125} - V_{R25}}{100°C}$		±157			µV/°C

TABLE III. Group A Inspection (cont).

SUBGROUP	PARAMETERS	TEST CIRCUIT FIGURE	CONDITIONS [1]	LIMITS DAC870 "V" Grade MIN	LIMITS DAC870 "V" Grade MAX	LIMITS DAC870 "U" Grade MIN	LIMITS DAC870 "U" Grade MAX	UNITS
2U $T_A = +85°C$	Offset error, bipolar (V_{OE})	5	±10V range (ideal value = −10.000V)				±30	mV
	Gain error, bipolar (G_E)	5	±10V range (ideal value = +9.995117V) [2]				±40	mV
	Offset temperature sensitivity, Bipolar	—	±10V range, $\frac{\Delta V_{OE}}{\Delta T} = \frac{V_{OE85} - V_{OE25}}{60°C}$				±0.15	mV/°C
	Gain temperature sensitivity, Bipolar	—	±10V range, $\frac{\Delta VG_E}{\Delta T} = \frac{G_{E85} - G_{E25}}{60°C}$				±0.40	mV/°C
	Linearity error, bipolar	5	±10V range, [3] [4]					
			For + bit errors				+2.44	mV
			For − bit errors				−2.44	mV
	Differential linearity error, bipolar	5	±10V range [4] [5]				±4.88	mV
	Total error, untrimmed, bipolar	5	±10V range				±50	mV
	Total error, trimmed, bipolar	5	±10V range [7]				±30	mV
	Internal reference voltage	5				+6.23	+6.37	V
	Internal reference temperature sensitivity	—	$\frac{\Delta V_R}{\Delta T} = \frac{V_{R85} - V_{R25}}{60°C}$				±126	μV/°C
3 $T_A = -55°C$	Offset error, bipolar	5	±10V range (ideal value = −10.000V)		±30			mV
	Gain error, bipolar	5	±10V range (ideal value = +9.995117V) [2]		±50			mV
	Offset temperature sensitivity, Bipolar	—	±10V range, $\frac{\Delta V_{OE}}{\Delta T} = \frac{V_{OE25} - V_{OE-55}}{80°C}$		±0.30		±.90	mV/°C
	Gain temperature sensitivity, Bipolar	—	±10V range, $\frac{\Delta G_E}{\Delta T} = \frac{G_{E25} - G_{E-55}}{80°C}$		±0.50		±1.50	mV/°C
	Linearity error, bipolar	5	±10V range, [3] [4]					
			For + bit errors		+2.44		+14.64	mV
			For − bit errors		−2.44		−14.64	mV
	Differential linearity error, bipolar	5	±10V range [4] [5]		±4.88		±14.64	mV
	Total error, untrimmed, bipolar	5	±10V range		±80			mV
	Total error, trimmed, bipolar	5	±10V range [7]		±60			mV
	Internal reference voltage	5		+6.23	+6.37			V
	Internal reference temperature sensitivity	—	$\frac{\Delta V_R}{\Delta T} = \frac{V_{R25} - V_{R-55}}{80°C}$		±157			μV/°C
3U $T_A = -55°C$	Offset error, bipolar	5	±10V range (ideal value = −10.000V)				±30	mV
	Gain error, bipolar	5	±10V range (ideal value = +9.995117V) [2]				±40	mV
	Offset temperature sensitivity, Bipolar	—	±10V range, $\frac{\Delta V_{OE}}{\Delta T} = \frac{V_{OE25} - V_{OE-25}}{50°C}$				±0.30	mV/°C
	Gain temperature sensitivity, Bipolar	—	±10V range, $\frac{\Delta G_E}{\Delta T} = \frac{G_{E25} - G_{E-25}}{50°C}$				±0.40	mV/°C
	Linearity error, bipolar	5	±10V range, [3] [4]					
			For + bit errors				+2.44	mV
			For − bit errors				−2.44	mV
	Differential linearity error, bipolar	5	±10V range [4] [5]				±4.88	mV
	Total error, untrimmed, bipolar	5	±10V range				±50	mV
	Total error, trimmed, bipolar	5	±10V range [7]				±30	mV
	Internal reference voltage	5				+6.23	+6.37	V
	Internal reference temperature sensitivity	—	$\frac{\Delta V_R}{\Delta T} = \frac{V_{R25} - V_{R-25}}{50°C}$				±126	μV/°C
4 $T_A = +25°C$	Settling Time	6	T_O ±1/2LSB, ΔV_O = 20V		7		•	μsec
	Slew Rate	6	ΔV_O = 20V, 10% to 90%	10		•		V/μsec

NOTES:
1/ $\pm V_{CC}$ = 15VDC, V_{DD} = 5VDC, Logic 1 = 4V, Logic 0 = 0.2V, no load, unless otherwise specified.
2/ Offset error corrected to zero.
3/ The individual bit errors that are positive are switched on and compared to 1/2LSB. The individual bit errors that are negative are switched on and compared to 1/2LSB. This guarantees ±1/2LSB maximum linearity error.
4/ Offset error and gain error correction factors for the Device Under Test (DUT), if any, are applied to the DUT output voltage before comparing the DUT output voltage to the ideal output voltage. This is the basis for linearity error and differential linearity error relative to a straight line through the end points of the transfer function.
5/ Differential linearity error is tested at all combinations of the four most significant bits.
6/ Total error, trimmed, (bipolar) is the same as linearity error, bipolar.
7/ Offset and gain errors adjusted to zero at T_A = +25°C.

TABLE IV. Ideal Output Voltage vs Digital Input Code.

Output Range	Digital Input Code [Complementary 12-Bit Binary]		
	1111 1111 1111	0111 1111 1111	0000 0000 0000
−2.5V to +2.5V	−2.500V	0	+2.498779V
−5V to +5V	−5.000V	0	+4.997559V
−10V to +10V	−10.000V	0	+9.995117V
0 to +5V	0	+2.500V	+4.998779V
0 to +10V	0	+5.000V	+9.997559V

NOTES:
1. One LSB = 1.2207mV for a 5-volt full scale range. One LSB = 2.4414mV for a 10-volt full scale range. One LSB = 4.8828mV for a 20-volt full scale range.
2. Digital input codes are shown with the MSB listed first.

TABLE V. Output Range Selection.

24-pin Side Braze Package				
Output Range	Required External Pin Connections			
−2.5V to +2.5V	15 to 18	17 to 20	19 to 20	16 to 24
−5V to +5V	15 to 18	17 to 20	19 NC	16 to 24
−10V to +10V	15 to 19	17 to 20	19 to 15	16 to 24
0 to +5V	15 to 18	17 to 21	19 to 20	16 to 24
0 to +10V	15 to 18	17 to 21	19 NC	16 to 24
28-Terminal LCC Package				
Output Range	Required External Pin Connections			
−2.5V to +2.5V	18 to 21	20 to 24	23 to 24	19 to 28
−5V to +5V	18 to 21	20 to 24	23 NC	19 to 28
−10V to +10V	18 to 23	20 to 24	23 to 18	19 to 28
0 to +5V	18 to 21	20 to 25	23 to 24	19 to 28
0 to +10V	18 to 21	20 to 25	23 NC	19 to 28

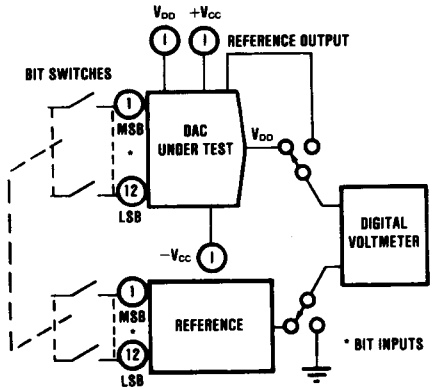


FIGURE 5. Test Circuit—Simplified.

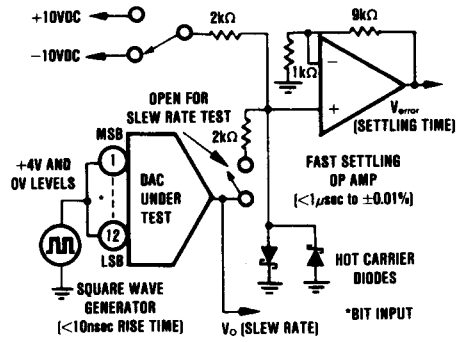


FIGURE 6. Slew Rate and Settling Time Test Circuit.

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures are in accordance with MIL-M-38510 and MIL-STD-883, method 5005, except as modified herein.

4.2 Qualification. Qualification is not required unless specifically required by contract or purchase order. When so required, qualification will be in accordance with the inspection routine of MIL-M-38510, paragraph 4.4.2.1. The inspections to be performed are those specified herein for groups A, B, C and D inspections (see paragraphs 4.4.1, 4.4.2, 4.4.3, and 4.4.4).

Burr-Brown has performed and successfully completed qualification inspection as described above. The most recent report is available from Burr-Brown.

4.3 Screening. Screening, the 883B Hi-Rel product designation, is in accordance with MIL-STD-883B, method 5004, class B, and is conducted on all devices. The following additional criteria apply:

a. Interim and final test parameters are specified in Table II.

b. Burn-in test (MIL-STD-883, method 1015) conditions:
   (1) Test condition D
   (2) Test circuit is Figure 7 herein
   (3) T_A = +125°C minimum
   (4) Test duration is 160 hours minimum

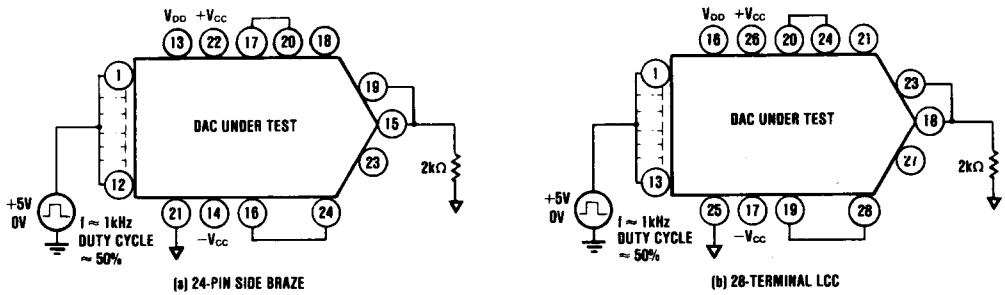


FIGURE 7. Test Circuit-Burn-in and Operating Life Test.

c. Percent defective allowable (PDA). The PDA, for /MIL product designation only, is 5 percent and includes both parametric and catastrophic failures. It is based on failures from group A, subgroup 1 test, after cool-down as final electrical test in accordance with MIL-STD-883, method 5004, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from preburn-in screening failures may be excluded from the PDA. If interim electrical parameter tests are omitted, all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1, after burn-in are used to determine the percent defective for each manufacturing lot, and the lot is accepted or rejected based on the PDA.

d. External visual inspection need not include measurement of case and lead dimensions.

4.4 Quality conformance inspection. Groups A and B inspections of MIL-STD-883, method 5005, are performed on each inspection lot. Groups C and D inspections of MIL-STD-883, are performed as required by MIL-STD-883. unless specified by contract or purchase order.

A report of the most recent groups C and D inspections is available from Burr-Brown.

4.4.1 Group A inspection. Group A inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005, and as specified in Table II herein.

4.4.2 Group B inspection. Group B inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005 (class B).

4.4.3 Group C inspection. Group C inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005 (class B), and as follows:

a. Operating life test (MIL-STD-883, method 1005) conditions:
   (1) Test condition D
   (2) Test circuit is Figure 5 herein
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 1000 hours minimum
b. End point electrical parameters are specified in Table II herein.

4.4.4 Group D inspection. Group D inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005 (class B) and as follows:

a. End point electrical parameters are specified in Table II herein.

4.4.5 Inspection of packaging. Inspection of packaging shall be in accordance with MIL-M-38510.

4.5 Methods of examination and test. Methods of examination and test are specified in the appropriate tables. Electrical test circuits are as prescribed herein or in the referenced test methods of MIL-STD-883.

4.5.1 Voltage and current. All voltage values given, except the input offset voltage (or differential voltage) are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use in applications where the use of screened parts is required or desirable.

6.3 Ordering data. The contract or purchase order should specify the following:

a. Complete part number (see paragraph 1.2).
b. Requirement for certificate of compliance, if desired.

6.4 Definitions.

Offset error. Offset error is the difference between the ideal analog output voltage and the actual output voltage, when all the input bits are off (digital input code: 1111 1111 1111).

Gain error. Gain error is the difference between the ideal analog output voltage span and the output voltage span, between when all the input bits are off (digital input code: 1111 1111 1111) and when all the input bits are on (digital input code: 0000 0000 0000).

Linearity error. Linearity error is the difference between the ideal analog output voltage and the actual output voltage, when the offset error and the gain error are equal to zero.

Differential linearity. Differential linearity is the difference between the ideal (1LSB) analog output voltage change, for a 1-bit change in digital input code and the actual output voltage change. A differential linearity of ±1LSB means that the output can change anywhere from 0LSB to 2LSB when the input changes from one adjacent input code to the next. Differential linearity of ±1LSB or less guarantees monotonicity.

Monotonicity. Monotonicity is the condition where the analog output increases or remains the same for a 1LSB increase in input codes.

Unipolar output. Unipolar is an output characteristic that displays zero volts output at one input extreme and full scale volts output at the other extreme.

Bipolar output. Bipolar is an output characteristic that displays full scale output voltage at one input extreme and the opposite full scale output voltage at the other input extreme.

6.5 Microcircuit group assignment. These microcircuits are assigned to Technology Group D with technology group number 856 as defined in MIL-M-38510, Appendix E.

6.6 Electrostatic sensitivity. CAUTION—these microcircuits may be damaged by electrostatic discharge. Precautions should be observed at all times.

7. APPLICATION INFORMATION

7.1 Power Supply Decoupling. For optimum performance and noise rejection, each power supply should be decoupled by connecting a 1μF tantalum or electrolytic capacitor from each power supply pin to the ground plane. Electrolytic capacitors, if used, should be paralleled with 0.01μF ceramic capacitors for best high frequency performance.

7.2 Power Supply Sensitivity. Power supply sensitivity is specified in Table I. Power supply sensitivity versus ripple frequency is shown in Figure 8.

7.3 External offset and gain error adjustment. The untrimmed accuracy of the DAC870 series is very good and is adequate for many applications. However, when the initial offset and gain errors are greater than what can be allowed in the application, the circuits shown in Figure 4 can be utilized to adjust the offset and gain errors to zero.

7.3.1 Offset adjustment. Apply the digital input code, 1111 1111 1111, which should produce zero volts output for the unipolar ranges, or minus full scale for the bipolar ranges. Adjust the offset potentiometer until the output, for the output range employed, is exactly the value indicated in Table IV.

7.3.2 Gain adjustment. Apply the digital input code, 0000 0000 0000, which should produce positive full scale. Adjust the gain potentiometer until the output is exactly as depicted in Table IV for the output range being utilized.

7.4 Reference supply. All models of the DAC870 are supplied with an internal 6.3V reference voltage supply. This voltage has a tolerance of ±1% and must be connected to the Reference Input for specified operation. This reference may be used externally also. The external current drain is limited to sourcing 2.5mA up to +85°C and 1mA up to +125°C exclusive of the current required by the bipolar offset circuit. An external buffer amplifier is recommended if this reference will be used to drive other system components, because variations in a load driven from the reference will result in bipolar offset variations of the DAC870 converter. Gain and bipolar offset adjustments should be made under constant load conditions. It should be noted that because of the design of the DAC870 an external reference voltage cannot be used with the DAC870.

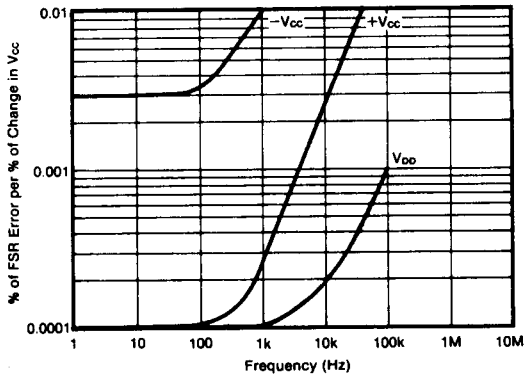


FIGURE 8. Power Supply Sensitivity vs Power Supply Ripple.