CS-510A/AR

2, 4, 6 Channel Read/Write Circuit for Center-tapped Ferrite Recording Heads

Description

The CS-510A is a bipolar monolithic integrated circuit designed for use with a center-tapped ferrite recording head. It provides a low noise read path, write current control, and data protection circuitry for as many as 6 channels. The CS-510A requires +5V and +12V power supplies and is available in a variety of packages.

The CS-510AR performs the same function as the CS-510A with the addition of internal 750 Ω damping resistors.

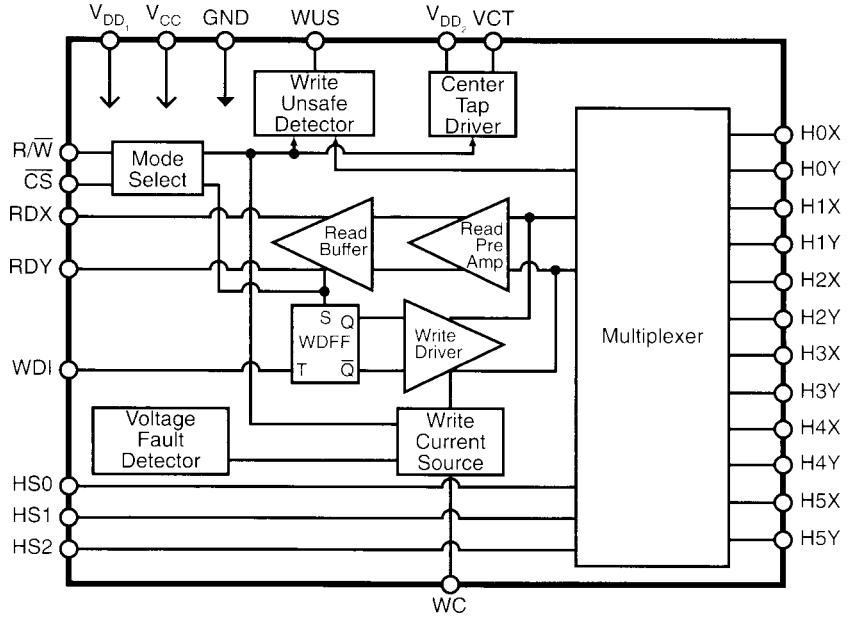
Features

- **+5V, +12V Power Supplies**
- **Single or Multi-platter Winchester Drives**
- **Designed for Center-tapped Ferrite Heads**
- **Programmable Write Current Source**
- **Easily Multiplexed for larger Systems**
- **Includes Write Unsafe Detection**
- **TTL Compatible Control Signals**
- **Power Supply Fault Protection**
- **1.5 nV/√Hz Maximum Input Noise Voltage**

Absolute Maximum Ratings (All voltages referenced to GND). Currents into device are positive.

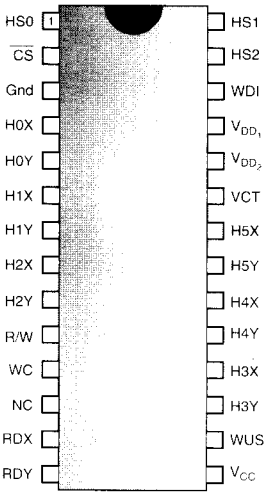
DC Supply Voltage (V_{DD_1})	-0.3 to +14V_{DC}
(V_{DD_2})	-0.3 to +14V_{DC}
(V_{CC})	-0.3 to +6 V_{DC}
Digital Input Voltage Range (V_{IN})	-0.3 to V_{CC} +0.3V_{DC}
Head Port Voltage Range (VH)	-0.3 to V_{DD_1} +0.3V_{DC}
WUS Pin Voltage Range (V_{WUS})	-0.3 to +14V_{DC}
Write Current (IW) Zero Peak	60mA
Output Current RDX, RDY (I_O)	-10mA
VCT	-60mA
WUS	+12mA
Storage Temperature Range(T_S)	-65 to 150°C
Lead Temperature PDIP (10 sec. Soldering)	260°C
Package Temperature PLCC, SO (20 Sec Reflow)	215°C

Block Diagram



Package Options

22 Lead PDIP
18, 24, 28 Lead SO Wide



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Recommended Operating Conditions

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Supply Voltage (V_{DD_1})		10.8	12.0	13.2	VDC
(V_{CC})		4.5	5.0	5.5	VDC
Head Inductance (Lh)		5		15	µH
Damping Resistor (RD) (510A only)		500		2000	ohms
RCT Resistor (RCT)*(1/4 Watt)	Iw = 40mA	142	150	158	ohms
Write Current (IW)		10		40	mA
Junction Temperature Range (T_J)		+25		+125	°C

*For Iw = 40mA, At other Iw levels refer to Applications Information that follows this specification.

DC Characteristics: Unless otherwise specified, $V_{DD_1} = V_{DD_2} = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $+25°C \leq T_J \leq +125°C$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Power Supply					
V_{CC} Supply Current					
Read/Idle	Read/Idle Mode			35	mA
Write	Write Mode			30	mA
V_{DD} Supply Current					
Idle (sum of V_{DD_1} and V_{DD_2})	Idle Mode			20	mA
Read	Read Mode			35	mA
Write	Write Mode			20+Iw	mA
Power Dissipation	T_J = +125°C				
Idle	Idle Mode			400	mW
Read	Read Mode			600	mW
Write	Write Mode, IW = 40mA, RCT = 0Ω			870	mW
■ Digital I/O					
VIL, Input Low Voltage				0.8	VDC
VIH, Input High Voltage		2.0			VDC
IIL, Input Low Current	VIL = 0.8V	-0.4			mA
IIH, Input High Current	VIH=2.0V			100	µA
VOL, WUS Output, Low Voltage	IOL = 8mA			0.5	VDC
IOH, WUS Output High Current	VOH = 5.0V			100	µA
■ Write Mode					
Center Tap Voltage (VCT)	Write Mode		6.0		VDC
Head Current (per side)	Write Mode, $0 \leq V_{CC} \leq 3.7V$ $0 \leq V_{DD_1} \leq 8.7V$	-200		200	µA
Write Current Range		10		40	mA
Write Current Constant "K"		2.375		2.625	
Iwc to Head Current Gain			0.99		mA/mA
Unselected Head Leakage Current				85	µA
RDX, RDY Output Offset Voltage	Write/Idle Mode	-20		+20	mV

DC Characteristics: continued

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Write Mode (continued)					
RDX, RDY Common Mode Output Voltage	Write/Idle Mode		5.3		VDC
RDX, RDY Leakage	RDX, RDY = 6V Write/Idle Mode	-100		100	µA
■ Read Mode					
Center Tap Voltage	Read Mode		4.0		VDC
Head Current (per side)	Read or Idle Mode $0 \le V_{CC} \le 5.5V$ $0 \le V_{DD_1} \le 13.2V$	-200		200	µA
Input Bias Current (per side)				45	µA
Output Offset Voltage	Read Mode	-440		+440	mV
Common Mode Output Voltage	Read Mode	4.5		6.5	VDC

Dynamic Characteristics and Timing: Unless otherwise specified, $V_{DD_1} = V_{DD_2} = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $+25°C \le T_J \le +125°C$, IW = 35mA, Lh = 10µH, Rd = 750Ω, f(WDI) = 5MHz, CL (RDX, RDY) ≤ 20pF.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Write Mode					
Differential Head Voltage Swing		7.0			V(pk)
Unselected Head Transient Current				2	mA(pk)
Differential Output Capacitance				15	pF
Differential Output Resistance	510A 510AR	10K 600		 960	Ω Ω
WDI Transition Frequency	WUS = low	250			kHz
■ Read Mode					
Differential Voltage Gain	V_{IN} = 1mVpp @ 300 kHz RL (RDX), RL (RDY) = 1kΩ	85		115	V/V
Dynamic Range	DC Input Voltage, VI, Where Gain Falls by 10%. V_{IN} = VI+0.5mVpp @ 300kHz	-3		+3	mV
Bandwidth (-3db)	Zs < 5Ω, V_{IN} = 1mVpp	30			MHz
Input Noise Voltage	BW = 15MHz, Lh = 0, Rh = 0			1.5	$nV/\sqrt{Hz}$
Differential Input Capacitance	f = 5MHz			20	pF
Differential Input Resistance	f = 5MHz 510A 510AR	2k 460		 860	Ω Ω
Common Mode Rejection Ratio	Vcm = VCT + 100mVpp @ 5MHz	50			db
Power Supply Rejection Ratio	100mVpp @ 5MHz on V_{DD_1}, V_{DD_2}, or V_{CC}	45			db
Channel Separation	Unselected Channels: V_{IN} = 100mVpp @ 5MHz & Selected Channel: V_{IN} = 0mVpp	45			db

Dynamic Characteristics and Timing: continued

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Read Mode (continued)					
Single Ended Output Resistance	f = 5MHz			30	Ω
Output Current	AC Coupled Load, RDX to RDY	2.1			mA
■ Switching Characteristics					
R/$\overline{W}$: R/$\overline{W}$ to Write	Delay to 90% of Write Current			1.0	µs
R/$\overline{W}$ to Read	Delay to 90% of 100mV 10MHz Read Signal Envelope or to 90% Decay of Write Current			1.0	µs
$\overline{CS}$: $\overline{CS}$ to Select	Delay to 90% of Write Current or to 90% of 100mV 10MHz Read Signal Envelope			1.0	µs
$\overline{CS}$ to Unselect	Delay to 90% Decay of Write Current			1.0	µs
HS0 HS1 to any Head HS2	Delay to 90% of 100mV 10MHz Read Signal Envelope			1.0	µs
WUS: Safe to Unsafe - TD1	Iw = 35mA	1.6		8.0	µs
Unsafe to Safe - TD2				1.0	µs
Head Current: Prop. Delay - TD3	Lh = 0µH, Rh = 0Ω From 50% Points			25	ns
Asymmetry	WDI has 50% Duty Cycle and 1ns Rise/Fall Time			2	ns
Rise/Fall Time	10% - 90% Points			20	ns

Package Pin Description

PACKAGE PIN #				PIN SYMBOL	FUNCTION
18L SO	22L PDIP	24L SO	28L SO		
18	22	24	1	HS0	Head Select
1	1	1	2	$\overline{CS}$	Chip Select
2	2	2	3	Gnd	Ground connection
4	3	3	4	H0X	X, Y Head connections
5	4	4	5	H0Y	X, Y Head connections
13	5	5	6	H1X	X, Y Head connections
12	6	6	7	H1Y	X, Y Head connections
	7	7	8	H2X	X, Y Head connections
	8	8	9	H2Y	X, Y Head connections
6	9	9	10	R/$\overline{W}$	Read/Write; high selects read mode
7	10	10	11	WC	Write current; used to set the magnitude of the write current
3		15, 16	12	NC	no connection
8	11	11	13	RDX	X, Y Read data; differential read signal out
9	12	12	14	RDY	X, Y, Read data; differential read signal out
10	13	13	15	V_{CC}	5V supply line
11	14	14	16	WUS	Write unsafe; a high level indicates an unsafe writing condition
	15	17	17	H3Y	X, Y Head connections

Package Pin Description: continued

PACKAGE PIN #				PIN SYMBOL	FUNCTION
18L SO	22L PDIP	24L SO	28L SO		
	16	18	18	H3X	X, Y Head connections
			19	H4Y	X, Y Head connections
			20	H4X	X, Y Head connections
			21	H5Y	X, Y Head connections
			22	H5X	X, Y Head connections
14	17	19	23	VCT	Voltage center tap; voltage source for head center tap
15	18	20	24	V_{DD_2}	Voltage supply line
16	19	21	25	V_{DD_1}	Voltage supply line
17	20	22	26	WDI	Write data in: negative transition toggles direction of head current
			27	HS2	Head Select
	21	23	28	HS1	Head Select

Circuit Description

The CS-510A has the ability to address up to 6 center-tapped ferrite heads and provide write drive or read amplification. Head selection and mode control are accomplished using the HSn, $\overline{CS}$, & R/$\overline{W}$ inputs as in tables 1 & 2. Internal pullups are provided for the $\overline{CS}$ & R/$\overline{W}$ inputs to force the device into a non-writing condition if either control line as opened accidentally.

Table 1: Mode Select

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	X	Idle

Table 2: Head Select

HS2	HS1	HS0	HEAD
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	X	None

0=Low Level 1=High level X=Don't Care

Write Mode

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects write mode which configures the CS-510A as a current switch and activates the Write Unsafe Detector circuitry. Write current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI). Note that a preceding read mode selection initializes the Write Data Flip-Flop, WDFF, to pass write current through the "X" side of the head. The zero-peak write current magnitude is programmed by an external resistor Rwc connected from pin WC to GND and is given by:

Iw = K/Rwc, where K = Write Current Constant

Write Unsafe Detection circuitry monitors voltage transitions at the selected head connections and flags any of the following conditions as a high level on the Write Unsafe, WUS, open collector output:

- Head open
- Head center tap open
- WDI frequency too low
- Device in Read mode
- Device not selected
- No write current

Two negative transitions on WDI, after the fault is corrected, will clear the WUS flag.

To further ensure Data security, a Voltage Fault detection circuit prevents application of write current during power loss or power sequencing.

To enhance Write to Read recovery time the change in RDX, RDY common mode voltage is minimized by biasing these outputs to a level within the read mode range when in Write Mode.

Power dissipation in write mode may be reduced by placing a resistor (RCT) between V_{DD_1} and V_{DD_2}. Optimum resistor value is 120Ω x 40/Iw (Iw in mA). At low write currents, (<15mA) read mode dissipation is higher than write mode and RCT, though recommended, may not be considered necessary. In this case V_{DD_2} is connected directly to V_{DD_1}.

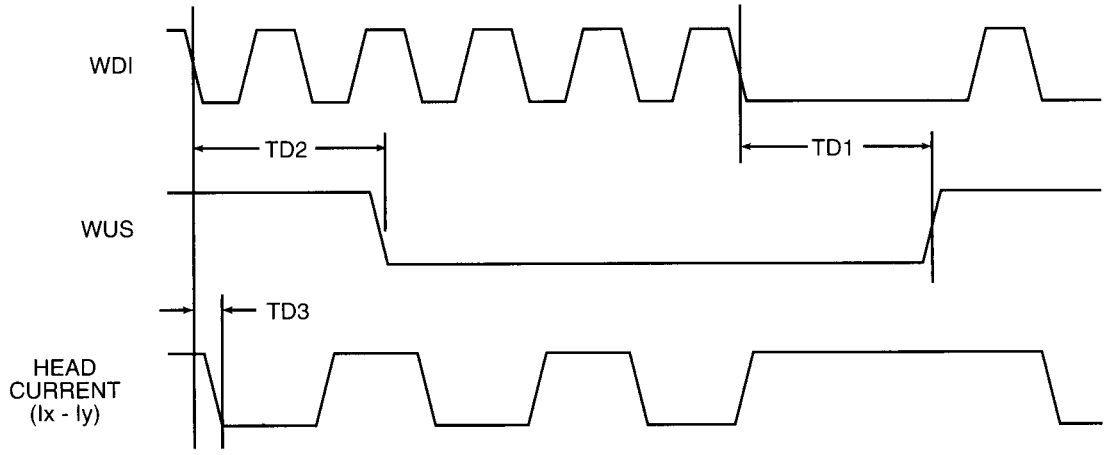
Read Mode

Taking $\overline{CS}$ low and R/$\overline{W}$ high selects read mode which configures the CS-510A as a low noise differential amplifier for the selected head. The RDX and RDY outputs are driven by emitter followers and are in phase with the "X" and "Y" head paths. These outputs should be AC coupled to the load. The internal write current source is gated off in Read mode eliminating the need for any external gating.

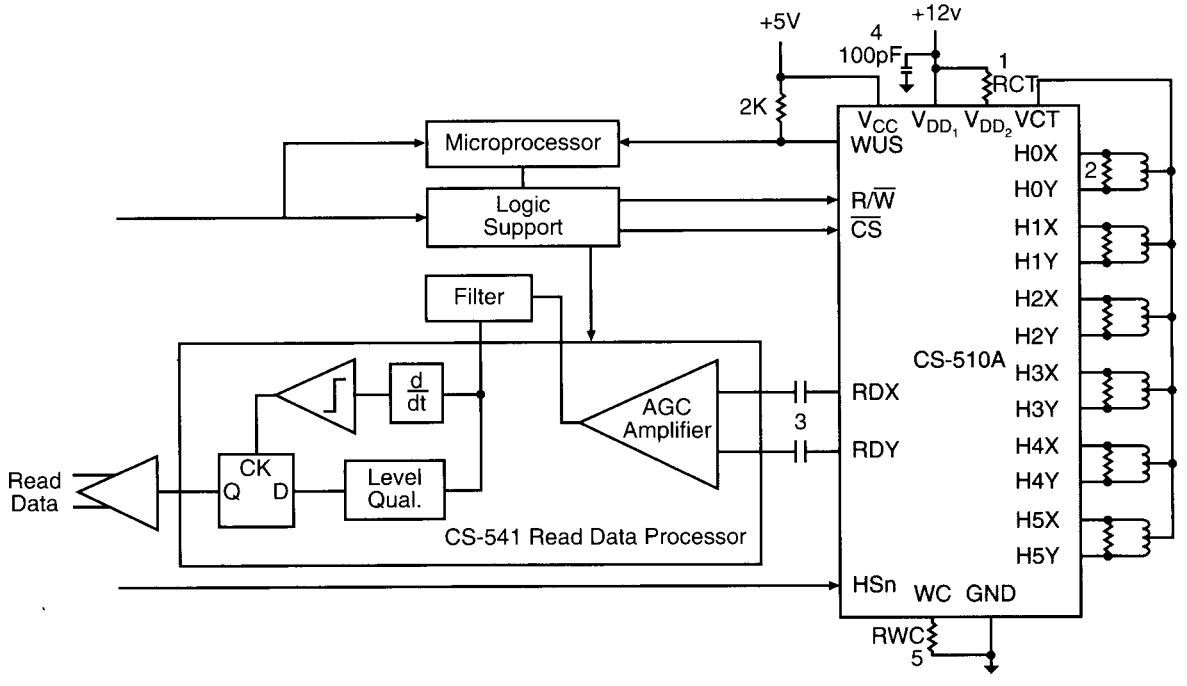
Idle Mode

Taking CS high selects the idle mode which switches the RDX, RDY outputs into a high impedance state and deactivates the internal write current source. This facilitates multi-device installations by allowing the read outputs to be wired OR'ed and the Write Current programming resistor to be common to all devices.

Write Mode Timing Diagram



Application Diagram



Notes:

1. An external resistor, RCT, given by; RCT = 120 (40/Iw) where Iw is the zero peak write current in mA, can be used to limit internal power dissipation. Otherwise connect V_{DD_2} to V_{DD_1}.

2. Damping resistors not required on 510AR versions.

3. Limit DC current from RDX and RDY to 100µA and load capacitance to 20pF. In multi-chip application these outputs can be wire-or'd.

4. The power bypassing capacitor must be located close to the 510A with its ground returned directly to device ground, with as short a path as possible.

5. To reduce ringing due to stray capacitance this resistor should be located close to the 510A. Where this is not desirable a series resistor can be used to buffer a long WC line. In multi-chip applications a single resistor common to all chips may be used.

Package Specification

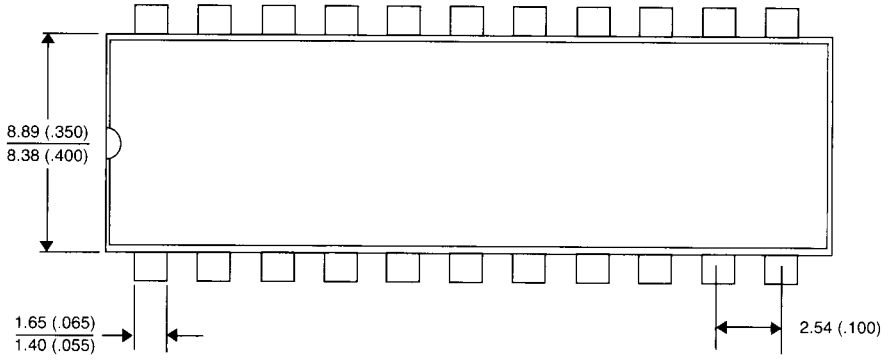
PACKAGE DIMENSIONS IN mm (INCHES)

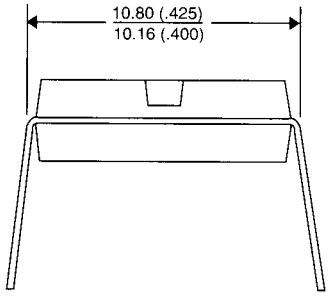
Lead Count	D			
	Metric		English	
	Max	Min	Max	Min
18L SO Wide	11.71	11.46	.461	.451
22L PDIP	27.94	27.69	1.1	1.09
24L SO Wide	15.54	15.29	.612	.602
28L SO Wide	18.06	17.81	.711	.701

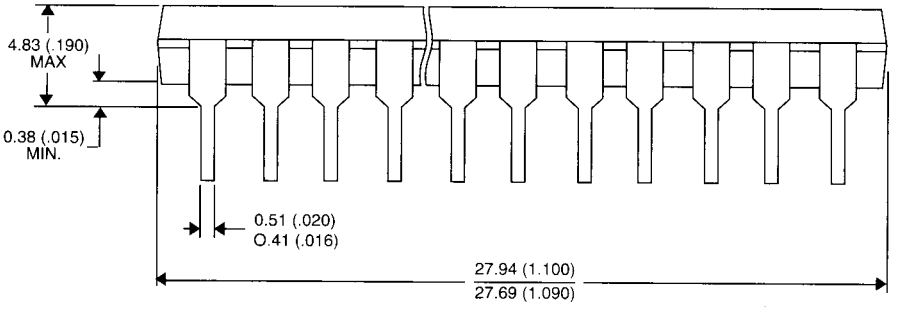
PACKAGE THERMAL DATA

Thermal Data	$R\Theta_{JA}$ typ	$R\Theta_{JC}$ typ	
18L SO Wide	100	21	°C/W
22L PDIP	60	24	°C/W
24L SO Wide	80	16	°C/W
28L SO Wide	75	15	°C/W

22L PDIP

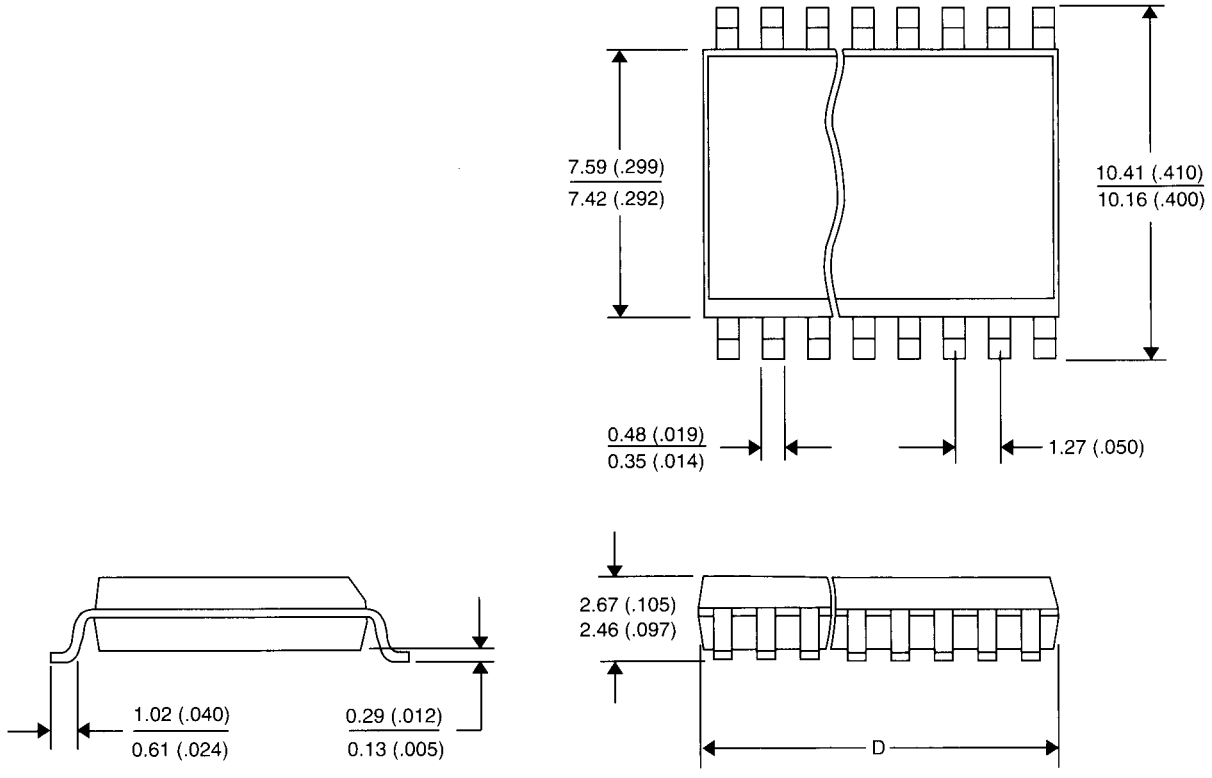






Package Specification: continued

18L, 20L, 24L and 28L SO Wide



Ordering Information

Part Number	Description
CS510A-2DW18	18 Lead SO
CS-510A-4N22	22 Lead PDIP
CS-510A-4DW24	24 Lead SO
CS-510A-6DW28	28 Lead SO
with internal damping resistors	
CS-510A-4RN22	22 Lead PDIP
CS510A-4RDW24	24 Lead SO

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