◇Structure Silicon monolithic integrated circuit
◇Product Series Lens control LSI
◇Type BU24025MWV
◇Applications Digital still cameras
◇Functions ・driver (1−5 channels) : Voltage control type H−bridge(Adaptable to STM 2 systems)
・driver (6,7 channels) : Current control type H−bridge

◇Absolute maximum ratings (Ta = 25℃)

Parameter	Symbol	Limits	Unit	Remark
Power supply voltage	DVDD	−0.3～4.5	V	
	MVCC	−0.3～7.0	V	
Input voltage	VIN	−0.3～DVDD+0.3	V	
Input/output current	IIN	±500	mA	Driver block (by MVCC pin)
		＋50	mA	by PIOUT pin
Storage temperature range	TSTG	−55～125	℃	
Operating temperature range	TOPE	−10～85	℃	
Permissible dissipation ∗1	PD	3000	mW	

This product is not designed for anti−radiation applications. ∗1 To use this product at a temperature higher than Ta=25℃, reduce 30mW per 1℃
(At mounting ROHM's standard board : 74.2mmx74.2mmx1.6ᵗmm/4 layer Board)

◇Operating conditions (Ta=25℃)

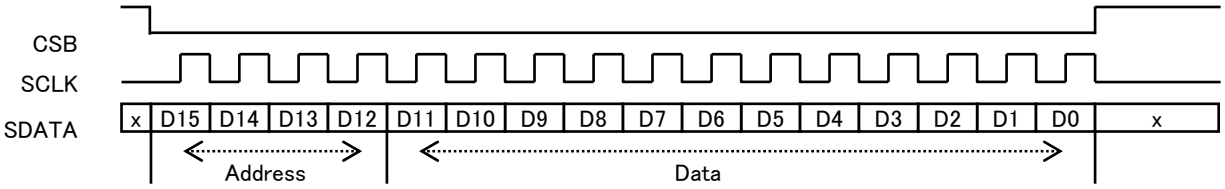
Parameter	Symbol	Limits	Unit	Remark
Digital power supply voltage	DVDD	2.7～3.6	V	DVDD≦MVCC
Driver power supply voltage	MVCC	2.7～5.5	V	
Clock operating frequency	FCLK	1～27.5	MHz	Reference clock

◇Electrical characteristics (Unless otherwise specified, Ta=25℃, DVDD=3.0V, MVCC=5.0V, DVSS=MGND = 0.0V)

Parameter	Symbol	Limits			Unit	Condition
		MIN.	TYP.	MAX.		
<Current consumption>						
Quiescence DVDD	ISSD	−	0.45	1.5	mA	CMD_RS=0
MVCC	ISSVM	−	50	100	μA	CMD_RS=0
Operation DVDD	IDDD	−	6	10	mA	
<Logic block>						
Low−level input voltage	VIL	DVSS	−	0.3DVDD	V	
High−level input voltage	VIH	0.7DVDD	−	DVDD	V	
Low−level input current	IIL	0	−	10	μA	VIL = DVSS
High−level input current	IIH	0	−	10	μA	VIH = DVDD
Low−level output voltage	VOL	DVSS	−	0.2DVDD	V	IOL = 1.0mA
High−level output voltage	VOH	0.8DVDD	−	DVDD	V	IOH = 1.0mA
<PI driving circuit>						
Output voltage	PIVO	−	0.16	0.50	V	IIH = 30mA
<Voltage driver block>						
ON−resistance	Ron	−	1.5	2.0	Ω	IO=±100 mA(the sum of high and low sides)
OFF−leak current	IOZ	−10	0	10	μA	Output Hiz setting
Average voltage accuracy between differential output pins	Vdiff	−5	−	+5	%	Vdiff setting: 010_1011
<Current driver block>						
ON−resistance	Ron	−	1.1	1.5	Ω	IO=±100 mA(the sum of high and low sides)
OFF−leak current	IOZ	−10	0	10	μA	Output Hiz setting
Output current	IO	190	200	210	mA	DAC setting: 1000_0000 RRNF=1 [Ω]

◇3-wire serial interface

Control commands are framed by 16-bit serial input (MSB first) and input through the CSB, SCLK, and SDATA pins. 4 higher-order bits specify addresses, while the remaining 12 bits specify data.
Data of every bit is input through the SDATA pin, retrieved on the rising edges of SCLK.
Data becomes valid in the CSB Low area. The loading timing is different in the resistor. (as shown in "Note4,5")



＜Register map＞

Address[3:0]				Data[11:0]											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	ModeA[1:0]		SelA[1:0]		0	Ach different output voltage[6:0]						
0	0	0	1	0	0	0	0	Ach Cycle[7:0]							
				0	0	1	0	Ach Cycle[15:8]							
				0	1	1	0	A_BEXC	0	0	A_BSL	A_AEXC	0	0	A_ASL
				1	1	1	0	0	0	APOS[1:0]		0	0	0	ASTOP
0	0	1	0	EnA	RtA	Ach Pulse[9:0]									
0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	ModeB[1:0]		SelB[1:0]		0	Bch different output voltage [6:0]						
1	0	0	1	0	0	0	0	Bch Cycle[7:0]							
				0	0	1	0	Bch Cycle[15:8]							
				0	1	1	0	B_BEXC	0	0	B_BSL	B_AEXC	0	0	B_ASL
				1	0	0	0	0	0	3_chop[1:0]		0	0	4_chop[1:0]	
				1	0	1	3_PWM_Ct[1:0]		3ch PWM_Duty[6:0]						
				1	1	0	4_PWM_Ct[1:0]		4ch PWM_Duty[6:0]						
				1	1	1	0	0	0	BPOS[1:0]		0	0	0	BSTOP
1	0	1	0	EnB	RtB	Bch Pulse[9:0]									
1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	Chopping[1:0]		CacheM	0	0	Isel	P_CTRL	CLK_DIV[2:0]		
1	1	0	1	0	0	0	0	0	0	0	0	0	0	PI_CTRL1	PI_CTRL2
				0	0	1	0	0	0	0	0	5_Sel[1:0]		5_Chop[1:0]	
				0	1	0	5_PWM_Ct[1:0]		5ch PWM_Duty[6:0]						
1	1	1	0	0	0	0	0	Current driver reference voltage adjustment6 (DAC6 output value) [7:0]							
				0	1	0	0	7ch_S	0	7_PWM_Ct[1:0]		6ch_S	0	6_PWM_Ct[1:0]	
				1	0	0	0	Current driver reference voltage adjustment7 (DAC7 output value) [7:0]							
				1	1	0	0	0	0	0	0	0	0	0	CMD_RS
Addresses other than those above				Setting prohibited											

(Note 1) The notations A, B, in the register map correspond to Ach, Bch respectively.

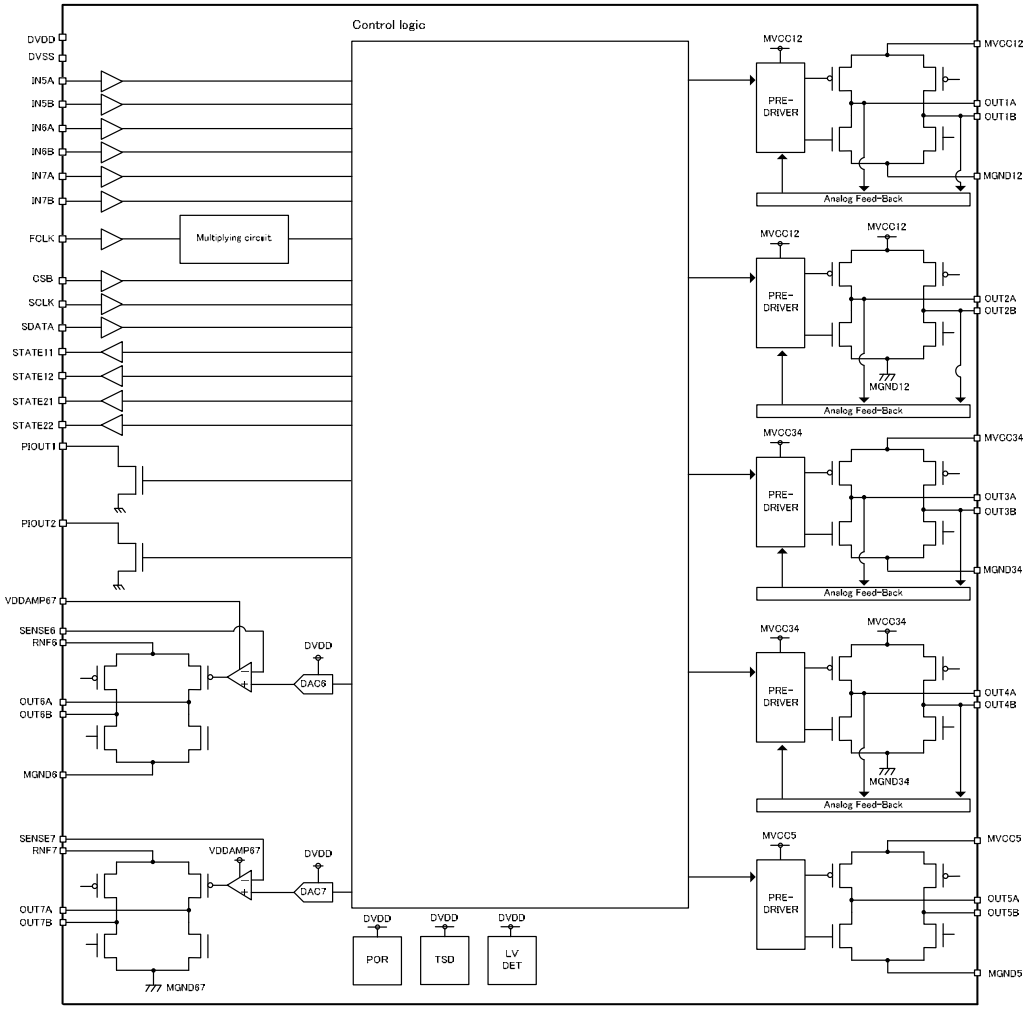
(Note 2) The Ach is defined as 1ch and 2ch driver output, the Bch as 3ch and 4ch driver output,

(Note 3) After resetting (Power ON reset, and CMD_RS), "initial setting" is saved in all registers.

(Note 4) For Mode, different output voltage, Cycle, En, and Rt registers, data that are written before the access to the Pulse register becomes valid, and determined at the rising edge of CSB after the access to the Pulse register. (The Mode, different output voltage, Cycle, En, Rt, and Pulse registers contain Cache registers, but any registers other than those do not contain with such registers.)

(Note 5) For POS, STOP, chop, PWM_Ct, and PWM_duty registers, data are determined at the rising edge of CSB, and for any registers other than those, data are determined at the rising edge of 16th SCLK .

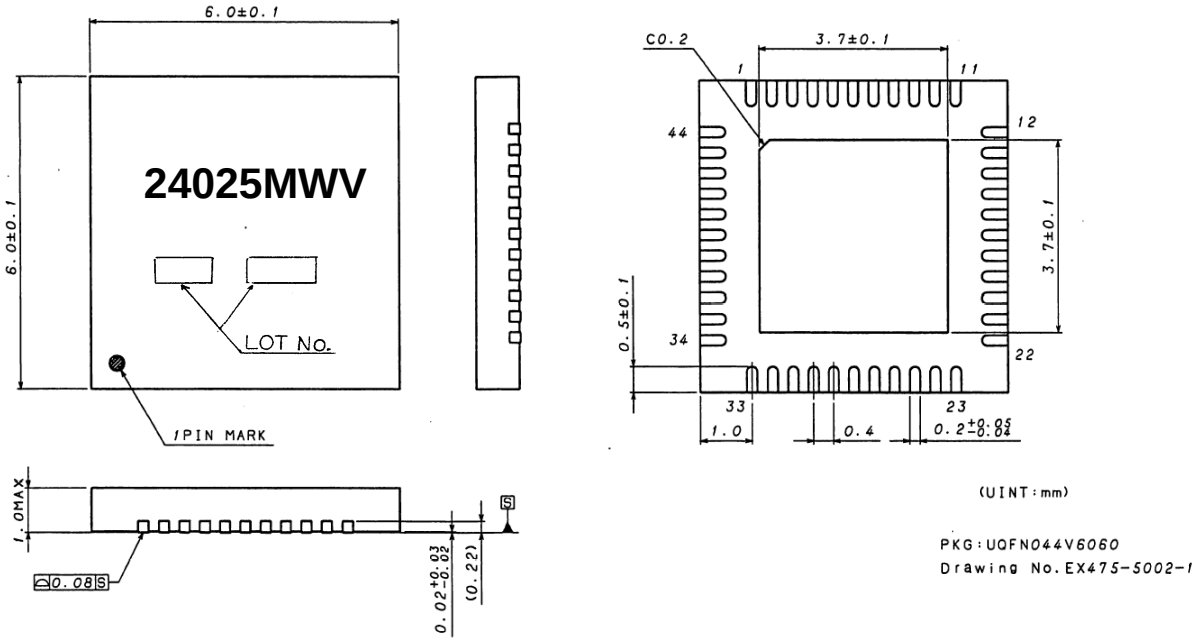
◇Block Diagram



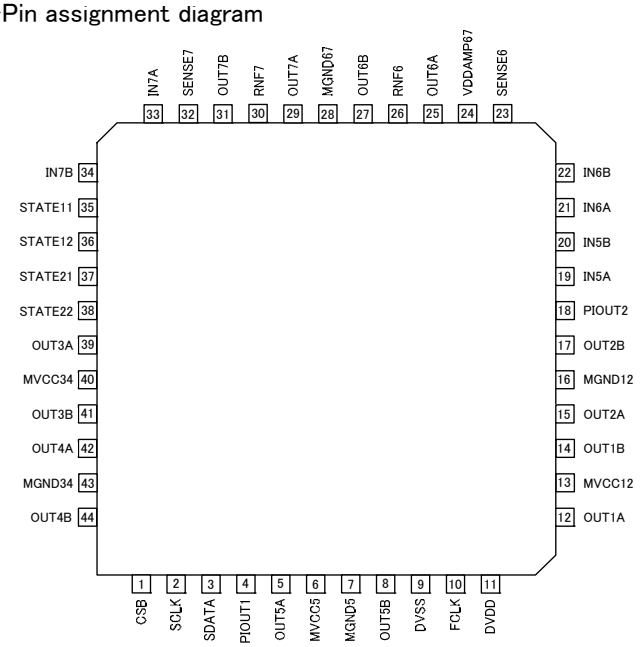
◇Pin functions

No.	Pin name	Power supply	Function	No.	Pin name	Power supply	Function
1	CSB	DVDD	CSB logic input	23	SENSE6	VDDAMP67	Negative input for 6ch current driver
2	SCLK	DVDD	SCLK logic input	24	VDDAMP67	–	Power supply of 6-7channel current driver control
3	SDATA	DVDD	SDATA logic input	25	OUT6A	RNF6	6-channel driver A output
4	PIOUT1	DVDD	PI driving output1	26	RNF6	RNF6	6-channel driver power supply
5	OUT5A	MVCC5	5-channel driver A output	27	OUT6B	RNF6	6-channel driver B output
6	MVCC5	–	5-channel driver power supply	28	MGND67	–	6-7channel driver ground
7	MGND5	–	5-channel driver ground	29	OUT7A	RNF7	7-channel driver A output
8	OUT5B	MVCC5	5-channel driver B output	30	RNF7	RNF7	7-channel driver power supply
9	DVSS	–	Digital ground	31	OUT7B	RNF7	7-channel driver B output
10	FCLK	DVDD	FCLK logic input	32	SENSE7	VDDAMP67	Negative input for 7ch current driver
11	DVDD	–	Digital power supply	33	IN7A	DVDD	IN7A logic input
12	OUT1A	MVCC12	1-channel drive A output	34	IN7B	DVDD	IN7B logic input
13	MVCC12	–	1-2channel driver power supply	35	STATE11	DVDD	STATE11 logic output
14	OUT1B	MVCC12	1-channel drive B output	36	STATE12	DVDD	STATE12 logic output
15	OUT2A	MVCC12	2-channel drive A output	37	STATE21	DVDD	STATE21 logic output
16	MGND12	–	1-2channel driver ground	38	STATE22	DVDD	STATE22 logic output
17	OUT2B	MVCC12	2-channel drive B output	39	OUT3A	MVCC34	3-channel driver A output
18	PIOUT2	DVDD	PI driving output2	40	MVCC34	–	3-4channel driver power supply
19	IN5A	DVDD	IN5A logic input	41	OUT3B	MVCC34	3-channel driver B output
20	IN5B	DVDD	IN5B logic input	42	OUT4A	MVCC34	4-channel driver A output
21	IN6A	DVDD	IN6A logic input	43	MGND34	–	3-4channel driver ground
22	IN6B	DVDD	IN6B logic input	44	OUT4B	MVCC34	4-channel driver B output

◇Outline dimensions/Marking figure



◇Pin assignment diagram



◇Cautions on use

(1) Absolute maximum ratings

If applied voltage, operating temperature range, or other absolute maximum ratings are exceeded, the LSI may be damaged. Do not apply voltages or temperatures that exceed the absolute maximum ratings. If you expect that any voltage or temperature could be exceeding the absolute maximum ratings, take physical safety measures such as fuses to prevent any conditions exceeding the absolute maximum ratings from being applied to the LSI.

(2) GND potential

Maintain the GND pin at the minimum voltage even under any operating conditions.
Actually check to be sure that none of the pins have voltage lower than that of GND pin, including transient phenomena.

(3) Thermal design

With consideration given to the permissible dissipation under actual use conditions, perform thermal design so that adequate margins will be provided.

(4) Short circuit between pins and malfunctions

To mount the LSI on a board, pay utmost attention to the orientation and displacement of the LSI. Faulty mounting to apply a voltage to the LSI may cause damage to the LSI. Furthermore, the LSI may also be damaged if any foreign matters enter between pins, between pin and power supply, or between pin and GND of the LSI.

(5) Operation in strong magnetic field

Make a thorough evaluation on use of the LSI in a strong magnetic field. Not doing so may malfunction the LSI.

Notes

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