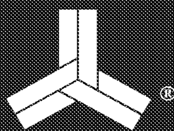
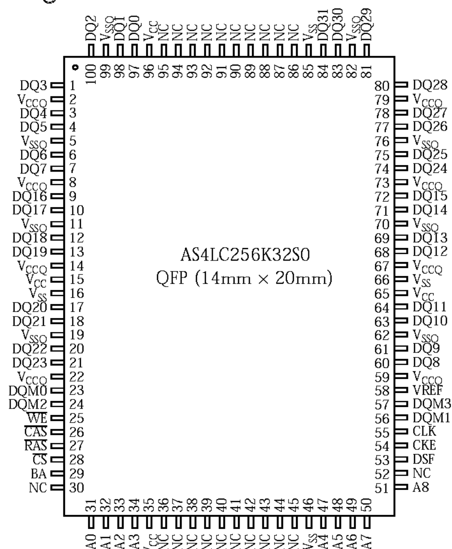


3.3V 256K×32 CMOS synchronous graphic RAM

Features

- Organization
  - 131,072 words × 32 bits × 2 banks
- Fully synchronous
  - All signals referenced to positive edge of clock
- Internal pipeline operation
  - Column address can be changed every clock cycle
- Two internal banks controlled by BA (bank select)
- High speed
  - 150/133/100 MHz
  - 6.5/7/9 ns clock access time
- 1024 refresh cycles, 16 ms refresh interval (Auto or Self)
- Auto precharge and Auto refresh modes
- Two color registers
- Burst read, single write operation
- LVTTL compatible I/O
- 3.3V power supply
- JEDEC standard package, pinout and function
  - 100-pin LQFP and TQFP
- Read/write data masking
- Programmable burst length (1/2/4/8/full page)
- Programmable burst sequence (sequential/interleaved)
- Programmable $\overline{CAS}$ latency (1/2/3)
- Graphics features
  - SMRS cycle
  - Block write (8 columns), write per bit

Pin arrangement



Pin designation

Pin(s)	Description
DQM0 to DQM3	Output disable/write mask
A0 to A8	Address inputs
BA	Bank select input
DQ0 to DQ31	Input/output
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
V_{CC}, V_{CCQ}	Power (3.3V ± 0.3V)
V_{SS}, V_{SSQ}	Ground
CLK	Clock input
CKE	Clock enable
DSF	Special function enable
VREF	SSTL reference voltage input

SGRAM

Selection guide

	Symbol	-150	-133	-100	Unit
Bus frequency	f_{max}	150	133	100	MHz
Maximum clock access time	t_{AC}	6.5	7	9	ns
Minimum address setup time	t_{AS}	2	2.5	2.5	ns
Minimum address hold time	t_{AH}	1.5	1.5	1.5	ns
Minimum row cycle time	t_{RC}	60	67.5	78	ns
Maximum operating current	I_{CC1}	300	275	185	mA
Maximum CMOS standby current, self refresh	I_{CC6}	3	3	3	mA

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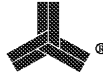


Functional description

The AS4LC256K32S0 is a high performance 8 megabit CMOS Synchronous Graphics Random Access Memory (SGRAM) organized as 131,072 words × 32 bits × 2 banks. Very high bandwidth is achieved using a pipelined architecture where all inputs and outputs are referenced to the rising edge of a common clock. Programmable burst mode can be used to read up to a full page of data without selecting a new column address.

The two internal banks can be alternately accessed (read or write) at the maximum clock frequency for seamless interleaving operations. This provides a significant advantage over asynchronous EDO and fast page mode devices.

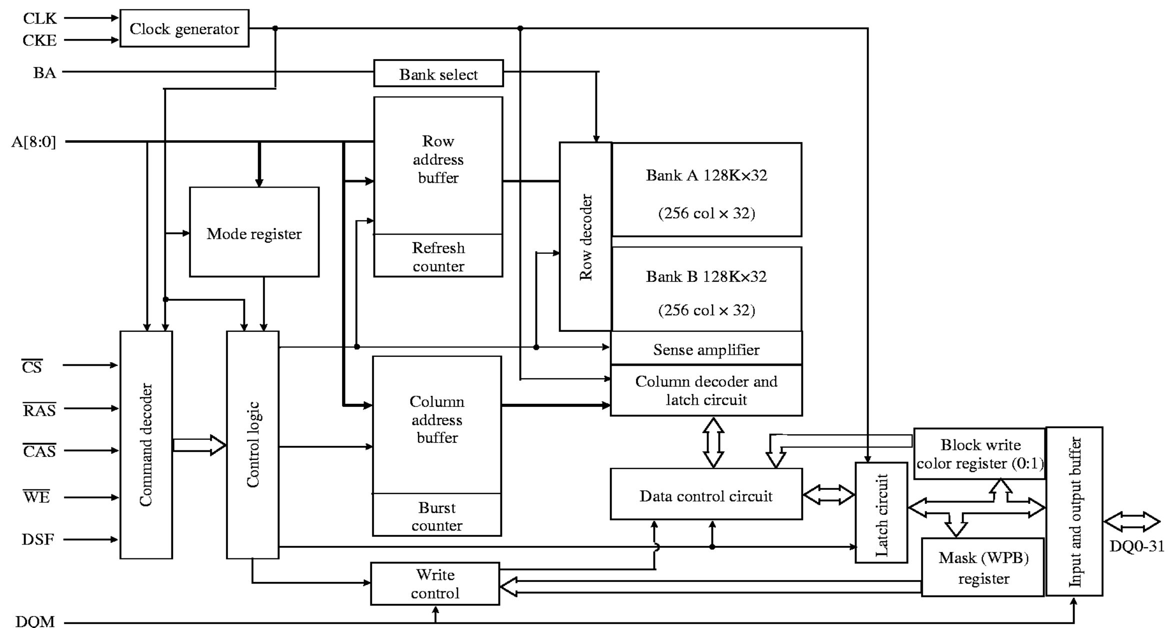
This SGRAM product also features a programmable mode register, allowing users to select read latency as well as burst length and type (sequential or interleaved). Lower latency improves first data access in terms of CLK cycles, while higher latency improves maximum frequency of operation. This feature enables flexible performance optimization for a variety of applications.

DRAM commands and functions are decoded from control inputs. Basic commands are as follows:

- Mode register set
- De-activate bank
- Deactivate all banks
- Select row, activate bank
- Select column, write
- Select column, read
- Deselect, power down
- CBR refresh
- Auto precharge with read/write
- Self refresh
- Block write
- Write per bit
- Special mode register set

The 8 Mb SGRAM device is available in a 100-pin LQFP or 100-pin TQFP. It operates with a power supply of 3.3V ± 0.3V. Multiple power and ground pins are provided for low switching noise and EMI. Inputs and outputs are LVTTL compatible.

Logic block diagram



SGRAM

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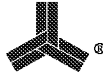

Recommended operating conditions

Parameter	Symbol	Min	Nominal	Max	Unit
Supply voltage	V_{CC}, V_{CCQ}	3.0	3.3	3.6	V
	GND	0.0	0.0	0.0	V
Input voltage	V_{IH}	2.0	–	V_{CC} + 0.3	V
	V_{IL}	-0.5†	–	0.8	V
Output voltage‡	V_{OH}	2.4	–	–	V
	V_{OL}	–	–	0.4	V
Ambient operating temperature	T_A	0		70	℃

† V_{IL} min = -1.5V for pulse widths less than 5 ns.

‡ I_{OH} = -2mA, and I_{OL} = 2mA

Recommended operating conditions apply throughout this document unless otherwise specified.

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Input voltage	V_{in}, V_{out}	-1.0	+4.6	V
Power supply voltage	V_{CC}, V_{CCQ}	-1.0	+4.6	V
Storage temperature (plastic)	T_{STG}	-55	+150	℃
Power dissipation	P_D	–	1	W
Short circuit output current	I_{out}	–	50	mA

Stresses greater than those listed under **Absolute Maximum Ratings** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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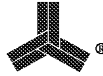

DC electrical characteristics

Parameter	Symbol	Test conditions		-150 Min	-150 Max	-133 Min	-133 Max	-100 Min	-100 Max	Unit	Notes
Input leakage current	I_{IL}	$0V \leq V_{in} \leq V_{CC}$, Pins not under test = 0V		-3	+3	-3	+3	-3	+3	μA	
Output leakage current	I_{OL}	D_{OUT} disabled, $0V \leq V_{out} \leq V_{CCQ}$		-3	+3	-3	+3	-3	+3	μA	
Operating current (one bank active)	I_{CC1}	$t_{RC} \geq$ min, IOL = 0mA, burst length = 1	CL = 3	–	300	–	275	–	185	mA	1
			CL = 2	–	275	–	250	–	175		
Precharge standby current (power down mode)	I_{CC2P}	$CKE \leq V_{IL}(max)$, t_{CK} = 15 ns		–	3	–	3	–	3	mA	
	I_{CC2PS}	CKE & $CLK \leq V_{IL}(max)$, $t_{CK} = \infty$		–	3	–	3	–	3	mA	
Precharge standby current (non power down mode)	I_{CC2N}	$CS \geq V_{IH}(min)$, $CKE \geq V_{IH}(min)$, t_{CC} = 15 ns; input signals changed once during 30 ns		–	45	–	45	–	45	mA	
	I_{CC2NS}	$CLK \leq V_{IL}(max)$, $CKE \geq V_{IH}(min)$, $t_{CK} = \infty$; input signals stable		–	20	–	20	–	20	mA	
Active standby current (power down mode)	I_{CC3P}	$CKE \leq V_{IL}(max)$, t_{CK} = 15 ns		–	3	–	3	–	3	mA	
	I_{CC3PS}	CLK, $CKE \leq V_{IL}(max)$, $t_{CK} = \infty$		–	3	–	3	–	3	mA	
Active standby current (non power down mode, one bank active)	I_{CC3N}	$CKE \geq V_{IH}(min)$, $CS \geq V_{IH}(min)$, t_{CK} = 15 ns; input signals changed once during 30 ns		–	50	–	50	–	50	mA	
	I_{CC3NS}	$CKE \geq V_{IH}(min)$, $CLK \geq V_{IL}(max)$, $t_{CK} = \infty$; input signals stable		–	25	–	25	–	25	mA	
Operating current (burst mode)	I_{CC4}	I_{OL} = 0 mA, Page burst All banks activated $t_{CCD} = t_{CCD}(min)$	CL = 3	–	225	–	200	–	190	mA	1,2
			CL = 2	–	175	–	150	–	140		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}(min)$	CL = 3	–	180	–	150	–	150	mA	3
			CL = 2	–	150	–	130	–	130		
Self refresh current	ICC6	$CKE \leq 0.2$ V		–	3	–	3	–	3	mA	

* CL = CAS latency
1 This parameter depends on output loading and cycle rates. Measured with outputs open, inputs only change one time during t_{CK} (min).
2 Assumed t_{CCD} (min)
3 Refresh period = 16ms

SGRAM

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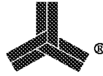

AC parameters common to all waveforms

Symbol	Parameter	CAS latency	-150 Min	-150 Max	-133 Min	-133 Max	-100 Min	-100 Max	Unit	Notes
t_{RRD}	Row active to row active delay		6.5	–	7.5	–	10	–	ns	1
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time		20	–	22.5	–	30	–	ns	1
t_{RP}	Row precharge		20	–	22.5	–	30	–	ns	1
t_{RAS}	Row active		40	120K	45	120K	60	120K	ns	1
t_{RC}	Row cycle time		60	–	67.5	–	90	–	ns	1
t_{CDL}	Last data in to new column address delay		1	–	1	–	1	–	CLK	2
t_{RDL}	Last data in to row precharge		1	–	1	–	1	–	CLK	2
t_{BDL}	Last data in to burst stop		1	–	1	–	1	–	CLK	2
t_{CCD}	Column address to column address delay		1	–	1	–	1	–	CLK	3
t_{CK}	CLK cycle time	3	6.7	–	7.5	–	10	–	ns	4
		2	10	–	12	–	15	1000		4
t_{AC}	CLK to valid output delay	3	–	6.5	–	7.0	–	9.0	ns	4,5
		2	–	7.5	–	10	–	12		4,5
t_{OH}	Output data hold time		3.5	–	3.5	–	3.5	–	ns	
t_{CH}	CLK high pulse width		3.0	–	3.0	–	3.5	–	ns	6
t_{CL}	CLK low pulse width		2.5	–	3.0	–	3.5	–	ns	6
t_S	Input setup time		2.0	–	2.5	–	2.5	–	ns	6
t_H	Input hold time		1.5	–	1.5	–	1.5	–	ns	6
t_{SLZ}	CLK to output in low Z		3	–	3	–	3	–	ns	5
t_{SHZ}	CLK to output in high Z		3.5	6.7	3.5	7.5	3.5	10	ns	

1 Minimum clock cycles = (Minimum time / clock cycle time) rounded up
2 Minimum delay required to complete write.
3 Column address change allowed every cycle.
4 Parameters dependent on CAS latency.
5 If clock rising time > 1ns, (tr/2-0.5)ns should be added to parameter.
6 If (tr and tf) > 1ns, [(tr+tf)/2-1]ns should be added to parameter.

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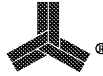

Operating modes

Command		CKE_{n-1}	CKE_n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	DQM	BA	A8	A7–A0	Note
Mode register set		H	X	L	L	L	L	L	X	Op code			1,2
Special mode register set		H	X	L	L	L	L	H	X	Op code			
Auto refresh		H	H	L	L	L	H	X	X	X	X	X	3
Self refresh	Entry	H	L	L	L	L	H	X	X	X	X	X	3
	Exit	L	H	L	H	H	H	X	X	X	X	X	3
				H	X	X	X	X	X	X	X	X	3
Bank activate		H	X	L	L	H	H	L	X	V	row address		—
	w/ WPB							H	X	V			
Read	Auto precharge disable	H	X	L	H	L	H	X	X	V	L	column address	4
	Auto precharge enable										H		4,5
Write	Auto precharge disable	H	X	L	H	L	L	L	X	V	L	column address	4
	Auto precharge enable										H		4,5
Block write	Auto precharge disable	H	X	L	H	L	L	H	X	V	L	column address	—
	Auto precharge enable										H		
Burst stop		H	X	L	H	H	L	X	X	X	X	X	6
Precharge	Selected bank	H	X	L	L	H	L	X	X	V	L	X	
	Both banks									X	H		
Clock suspend or active power down	Entry	H	L	H	X	X	X		X	X	X	X	
				L	V	V	V		X	X	X	X	
	Exit	L	H	X	X	X	X		X	X	X	X	
Precharge power down mode	Entry	H	L	H	X	X	X		X	X	X	X	
				L	H	H	H		X	X	X	X	
	Exit	L	H	H	X	X	X		X	X	X	X	
				L	V	V	V		X	X	X	X	
DQM		H	X	X	X	X	X		V	X	X	X	7
Deselect device		H	X	H	X	X	X	X	X	X	X	X	
No operation		H	X	L	H	H	H	X	X	X	X	X	

1 OP = operation code
A0~A8, BA see above.
2 MRS can be issued only when both banks are precharged. A new command can be issued 2 clock cycles after MRS.
3 Auto refresh functions similarly to CBR DRAM refresh. However, precharge is automatic.
Auto/self refresh can only be issued after both banks are precharged.
4 A8: bank select address. If low during read, write, row active and precharge, bank A is selected.
If high during those states, bank B is selected. Both banks are selected and A8 is ignored if A7 is high during row precharge.
5 A new read/write command cannot be issued during a burst read/write with auto precharge.
It must be issued after the end of the burst. A new row active command can be issued after t_{RP} from the end of the burst.
6 Burst stop command valid at every burst length.
7 DQM sampled at positive edge of CLK. Data-in may be masked at every CLK (Write DQM latency is 0).
Data-out mask is active 2 CLK cycles after issuance. (Read DQM latency is 2).

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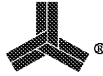

Mode register fields

Register programmed with MRS

Address	BA	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	Write mode		CR	LT mode			BT	burst length		

RFU = 0 during MRS cycle.

Write burst length

BA	A8	Mode
0	0	Normal
1	0	Multiple burst with single write

Burst type

A3	Type
0	Sequential
1	Interleaved

Color register

A7	Registers
0	One color
1	Two color

CAS latency

A6	A5	A4	Latency
0	0	0	Reserved
0	0	1	1
0	1	0	2
0	1	1	3
1	X	X	Reserved

Burst length

A2	A1	A0	BT = 0
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	X	X	Reserved†

†Burst length = full page when A2~A0 = 1.

SGRAM

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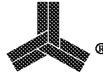

Burst sequence

(burst length = 2)

Initial address A0	Sequential		Interleave	
0	0	1	0	1
1	1	0	1	0

Burst sequence

(burst length = 4)

Initial address A1	A0	Sequential				Interleave			
0	0	0	1	2	3	0	1	2	3
0	1	1	2	3	0	1	0	3	2
1	0	2	3	0	1	2	3	0	1
1	1	3	0	1	2	3	2	1	0

Burst sequence

(burst length = 8)

Initial address A2	A1	A0	Sequential								Interleave							
0	0	0	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1	1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0	2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1	3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1	5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0	6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1	7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0

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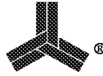

Pin descriptions

Pin	Name	Description
CLK	System clock	All operations synchronized to rising edge of CLK. CLK, driven by the system clock, increments the internal burst counter and controls output registers.
CKE	Clock enable	Controls CLK input. If CKE is high, the next CLK rising edge is valid. If CKE is low, the internal clock is suspended from the next clock cycle and the burst address and output states are frozen. If both banks are idle and CKE goes low, the SGRAM will enter power down mode from the next clock cycle. When in power down mode and CKE is low, no input commands will be acknowledged. To exit power down mode, raise CKE high before the rising edge of CLK.
$\overline{CS}$	Chip select	Enables or disables device operation by masking or enabling all inputs except CLK, CKE, DQM. Input commands are ignored when $\overline{CS}$ = High.
A0~A8	Address	Row and column addresses are multiplexed. Row address: A0~A8 during Active command. Column address: A0~A7 when $\overline{CAS}$ is active; A8 enables/ disables Auto Prechage.
BA	Bank select	Memory cell array is organized in 2 banks. BA selects which internal bank will be active. BA is latched during bank activate, read, write, mode register set, and precharge operations. Asserting BA low selects Bank A; BA high selects Bank B.
$\overline{RAS}$	Row address strobe	Enables row access and precharge operation. When $\overline{RAS}$ is low, row address is latched at the rising edge of CLK.
$\overline{CAS}$	Column address strobe	Enables column access. When $\overline{CAS}$ is low, column address is latched at the rising edge of CLK.
$\overline{WE}$	Write enable	Enables write operation and row precharge operation. When $\overline{WE}$ is low, input data is latched starting from $\overline{CAS}$.
DQM0~3	Output disable/ write mask	Controls I/O buffers. When DQM is high, output buffers are disabled during a read operation and input data is masked during a write operation. DQM latency is 2 clocks for Read and 0 clocks for Write.
DQ0~DQ31	Data input/output	Data inputs/outputs are multiplexed. Input mask for Writer-per-bit; column address mask when block write is active.
DSF	Special function variable	Enables block write, write-per-bit, and/or special mode register load.
V_{DD}/V_{SS}	Power supply/ground	Power and ground for core logic and input buffers.
V_{DDQ}/V_{SSQ}	Data output power/ground	Power and ground for data output buffers.

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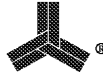

Device operation

Command	Pin settings	Description
Power up		The following sequence is recommended prior to normal operation. 1. Apply power, start clock, and hold all inputs high. 2. After power-up, pause for a minimum of 100µs. Drive CKE high prior to a positive clock edge; all others NOP. 3. Precharge both banks. 4. Perform a minimum of 2 auto refresh cycles to stabilize internal circuitry. 5. Perform Mode Register Set command to initialize mode register.
Mode register set	$\overline{CS}$ = $\overline{RAS}$ = $\overline{CAS}$ = $\overline{WE}$ = low; A0~A8 = opcode	The mode register stores the user selected opcode for the SGRAM operating modes. The $\overline{CAS}$ latency, burst length, burst type, test mode and other vendor specific functions are selected/programmed during the Mode Register Set command cycle. The default setting of the mode register is not defined after power-up. Therefore, it is recommended that the power-up and mode register set cycle be executed prior to normal SGRAM operation. Refer to the Mode Register Set table and timing for details.
Special mode register set		Use this command to load the mask and color registers used in block write and masked write cycles. Control information is applied to address inputs; data to be written to color or mask registers is applied to DQs. If A6 = 1, and all other inputs are 0, color register 0 receives DQ data. If A6 = A7 = Mode Register M7 = 1, color register 1 receives DQ data. If A5 = 1 and all other address inputs are 0, mask register receives DQ data.
Device deselect and no operation (NOP)	$\overline{CS}$ = high	The SGRAM is deselected when $\overline{CS}$ is high. $\overline{CS}$ high disables the command decoder such that $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and address inputs are ignored. Device deselection is also considered a NOP. The SGRAM also performs a NOP when $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ = high. Since the NOP performs no operation, it may be used as a wait state in performing normal SGRAM functions.
Bank activation	$\overline{CS}$ = $\overline{RAS}$ = low; $\overline{CAS}$ = $\overline{WE}$ = high; A0~A8 = row address; BA = bank select	The SGRAM is configured with two internal banks. Use the Bank Activate command to select a row in one of the two idle banks. Initiate a read or write operation after t_{RCD}(min) from the time of bank activation.
Bank activation with WPB		Write-per-bit is activated during a Bank Activation command. All write or block write cycles to the selected bank/row are masked based on the mask register.
Burst read	$\overline{CS}$ = $\overline{CAS}$ = A8 = low; $\overline{RAS}$ = $\overline{WE}$ = high; BA = bank select, A0~A7 = column address	Use the Burst Read command to access a consecutive burst of data from an active row in an active bank. Burst read can be initiated on any column address of an active row. The burst length, sequence and latency are determined by the mode register setting. The first output data appears after the CAS latency from the read command. The output goes into a high impedance state at the end of the burst (BL = 1,2,4,8) unless a new burst read is initiated to form a gapless output data stream. Terminate the burst with a burst stop command, precharge command to the same bank or another burst read/write.
Burst write	$\overline{CS}$ = $\overline{CAS}$ = $\overline{WE}$ = A10 = low; $\overline{RAS}$ = high; A0~A8 = column address	Use the Burst Write command to write data into the SGRAM on consecutive clock cycles to adjacent column addresses. The burst length and addressing mode is determined by the mode register opcode. Input the initial write address in the same clock cycle as the Burst Write command. Terminate the burst with a burst stop command, precharge command to the same bank or another burst read/write. DQM can also be used to mask the input data.

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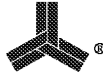

Command	Pin settings	Description
Block write		Use block write to write a single data value to a block of eight consecutive column locations addressed by A7-A3. A Special Mode Register Set command must occur before a block write to assign this data to the color register. Input data on DQs is used to mask specified column/byte combinations within the block.
DQM operation		Use DQM to mask input and output data. It disables the output buffers in a read operation and masks input data in a write operation. The output data is tri-stated 2 clocks after DQM assertion (2 clock latency). Input data is masked on the same clock as DQM assertion (0 clock latency).
Burst stop	$\overline{CS}$ = $\overline{WE}$ = low; $\overline{RAS}$ = $\overline{CAS}$ = high	Use burst stop to terminate burst operation. This command may be used to terminate all legal burst lengths.
Bank precharge	$\overline{CS}$ = A8 = $\overline{RAS}$ = $\overline{WE}$ = low; $\overline{CAS}$ = high; BA = bank select; A0~A7 = don't care	The Bank Precharge command precharges the bank specified by BA. The precharged bank is switched from active to idle state and is ready to be activated again. Assert the precharge command after t_{RAS}(min) of the bank activate command in the specified bank. The precharge operation requires a time of t_{RP}(min) to complete.
Precharge all	$\overline{CS}$ = $\overline{RAS}$ = $\overline{WE}$ = low; $\overline{CAS}$ = A8 = high; BA = bank select; A0~A7 = don't care	The Precharge All command may be used to precharge both banks simultaneously. If A8 is high, BA is a don't care and both banks are simultaneously precharged. If A8 is low, BA specifies which bank is to be precharged. Both banks are switched to the idle state on precharge completion.
Auto precharge	$\overline{CS}$ = $\overline{CAS}$ = $\overline{WE}$ (write) = low; $\overline{RAS}$ = $\overline{WE}$ (read) = A8 = high; BA = bank select; A0~A7 = column address	During auto precharge, the SGRAM adjusts internal timing to satisfy t_{RAS}(min) and t_{RP} for the programmed CAS latency and burst length. Couple the auto precharge with a burst read/write operation by asserting A8 to a high state at the same time the burst read/write commands are issued. At auto precharge completion, the specified bank is switched from active to idle state. Note that no new commands can be issued until the specified bank achieves the idle state.
Clock suspend/ power down mode entry	CKE = low	When CKE is low, the internal clock is frozen or suspended from the next clock cycle and the state of the output and burst address are frozen. If both banks are idle and CKE goes low, the SGRAM enters power down mode at the next clock cycle. When in power down mode, no input commands are acknowledged as long as CKE remains low. To exit power down mode, raise CKE high before the rising edge of CLK.
Clock suspend/ power down mode exit	CKE = high	Resume internal clock operation by asserting CKE high before the rising edge of CLK. Subsequent commands can be issued one clock cycle after the end of the Exit command.

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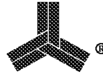

Command	Pin settings	Description
Auto refresh	$\overline{CS}$ = $\overline{RAS}$ = $\overline{CAS}$ = low; $\overline{WE}$ = CKE = high; A0~BA = don't care	SGRAM storage cells must be refreshed every 64ms to maintain data integrity. Use the Auto Refresh command to accomplish the refreshing of all rows in both banks of the SGRAM. The row address is provided by an internal counter which increments automatically. Auto refresh can only be asserted when both banks are idle and the device is not in the power down mode. The time required to complete the auto refresh operation is t_{RC}(min). Use NOPs in the interim until the auto refresh operation is complete. This is the most common refresh mode. It is typically performed once every 15.6us or in a burst of 1024 auto refresh cycles every 64ms. Both banks will be in the idle state after this operation.
Self refresh	$\overline{CS}$ = $\overline{RAS}$ = $\overline{CAS}$ = CKE = low; $\overline{WE}$ = high; A0~BA = don't care	Self refresh is another mode for refreshing SGRAM cells. In this mode, refresh address and timing are provided internally. Self refresh entry is allowed only when both banks are idle. The external clock and all input buffers with the exception of CKE are disabled in this mode. Exit self refresh by restarting the external clock and then asserting CKE high. NOP's must follow for a time of t_{RC}(min) for the SGRAM to reach the idle state where normal operation is allowed. If burst auto refresh is used in normal operation, burst 1024 auto refresh cycles immediately after exiting self refresh.

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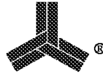
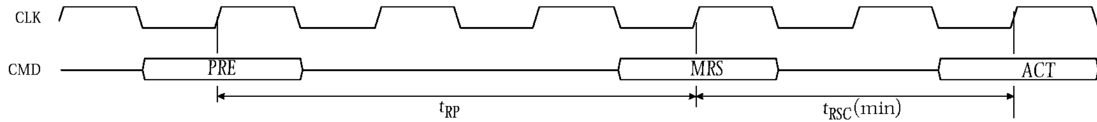


Mode register set command waveform

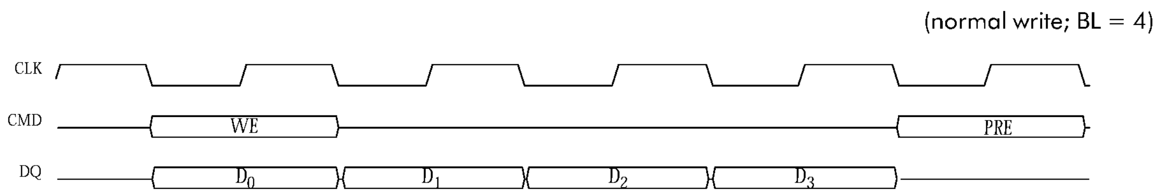


MRS can be issued only when both banks are idle.

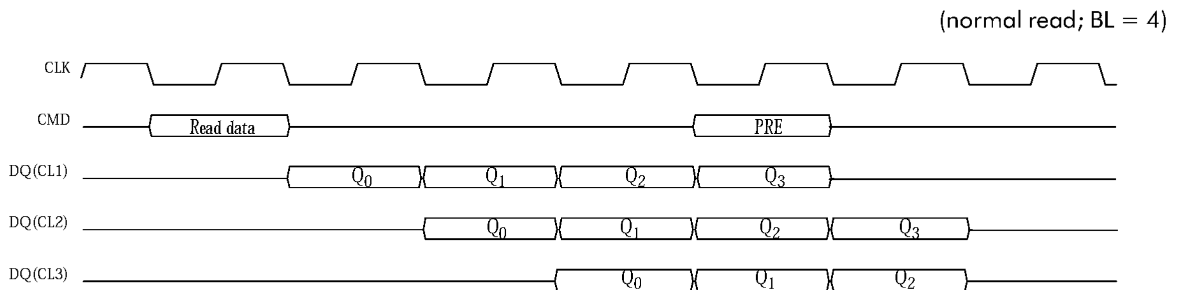
Precharge waveforms

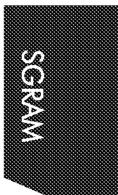
Precharge can be asserted after t_{RAS} (min). The selected bank will enter the idle state after t_{RP}. The earliest assertion of the precharge command without losing any burst data is show below.

(normal write; BL = 4)



(normal read; BL = 4)

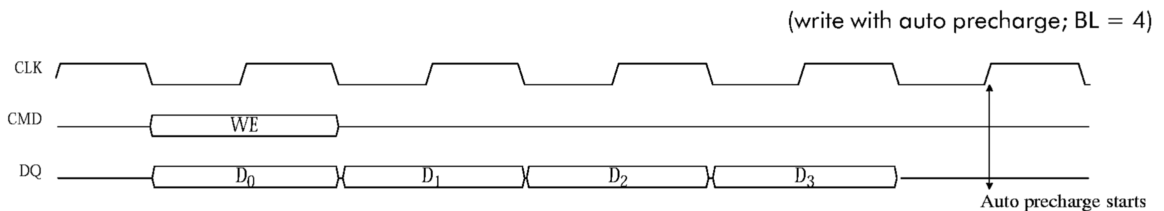




Auto precharge waveforms

A8 controls the selection of auto precharge during the read or write command cycle.

(write with auto precharge; BL = 4)



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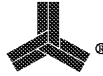
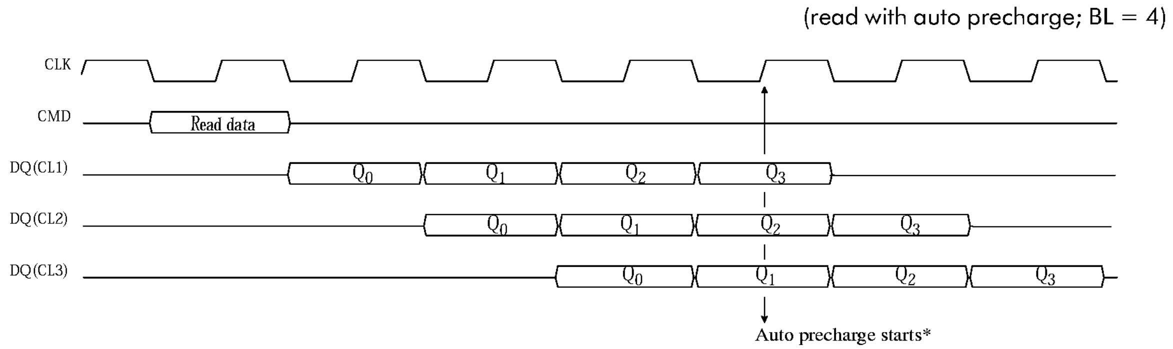


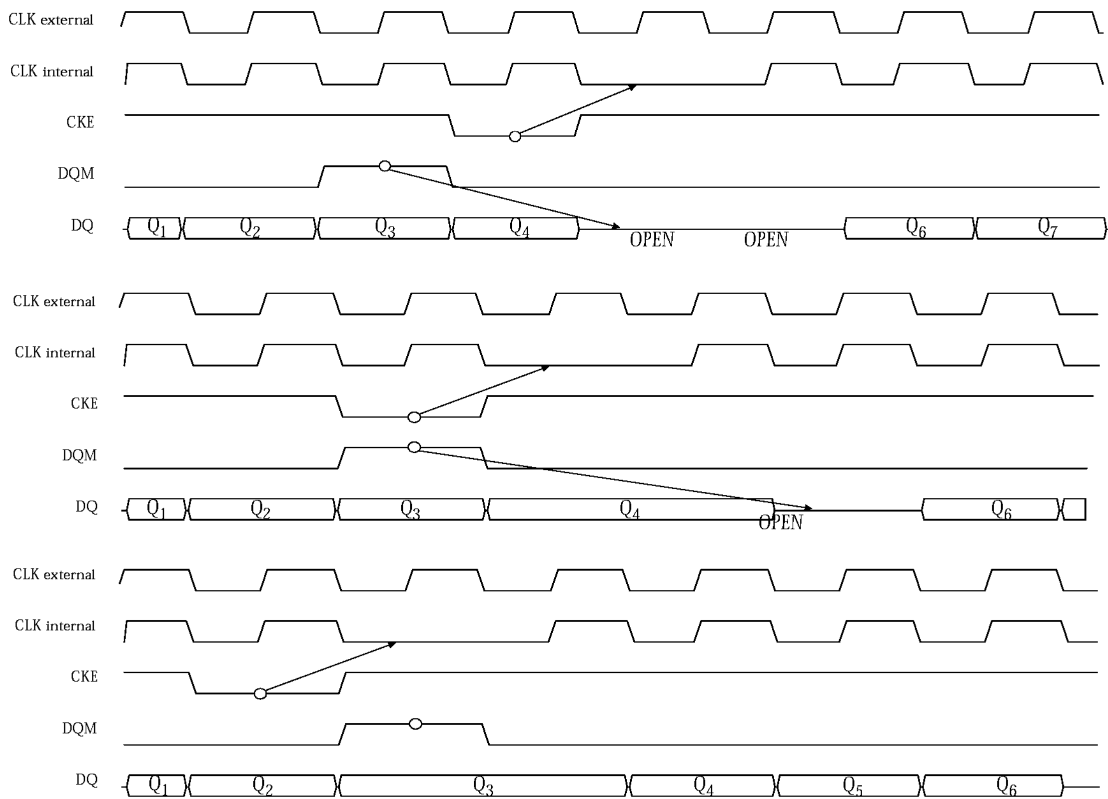
(read with auto precharge; BL = 4)



*The row active command of the precharge bank can be issued after t_{RP} from this point. The new read/write command of another activated bank can be issued from this point. At burst read/write with auto precharge, CAS interrupt of the same/another bank is illegal.

Clock suspension read waveforms

(BL = 8)



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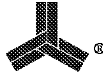
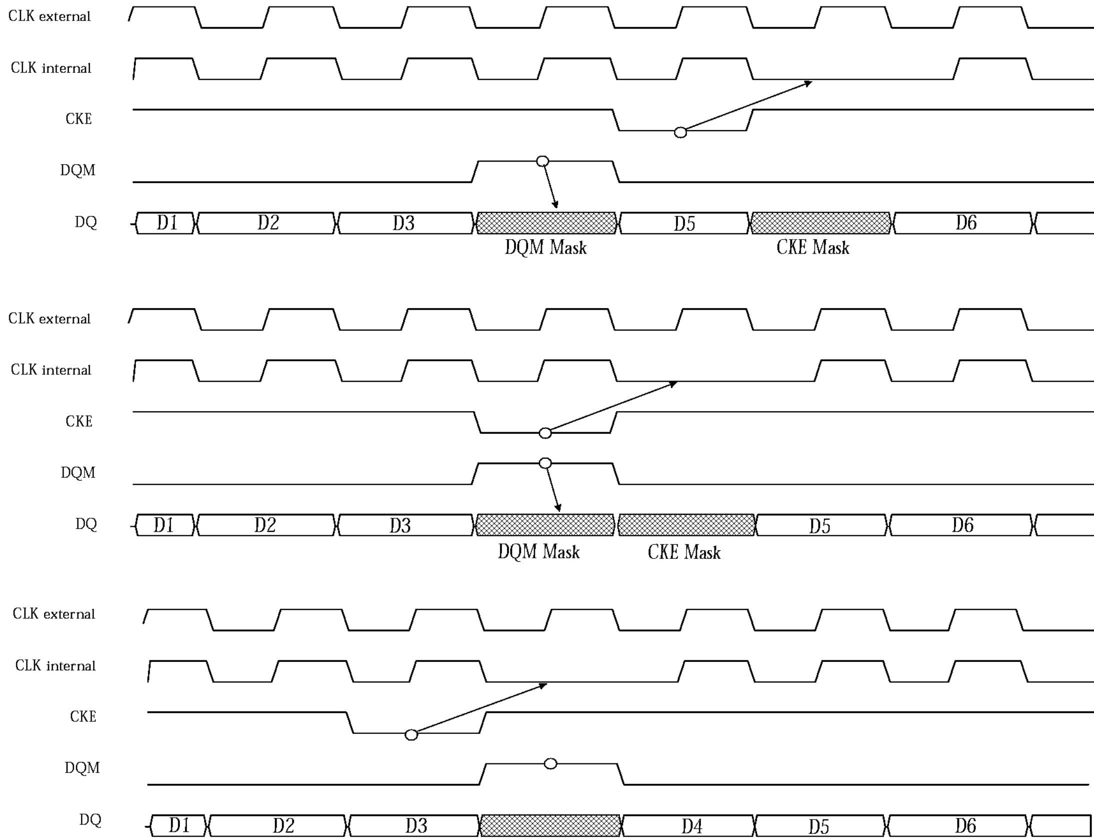
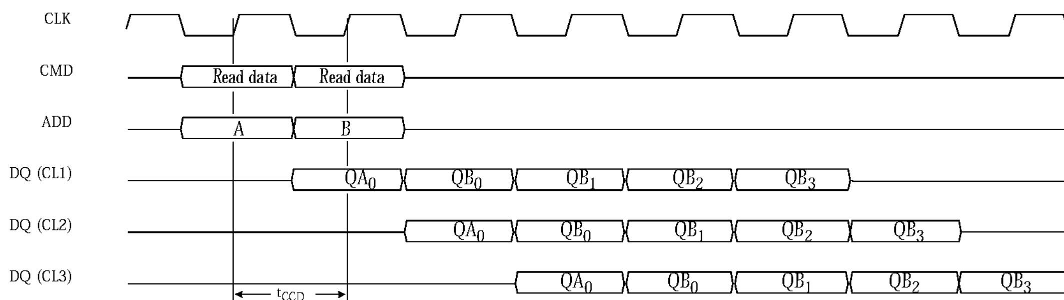


Clock suspension write waveforms



Read/write interrupt timing

read interrupted by read (BL = 4)



t_{CCD} = $\overline{CAS}$ to $\overline{CAS}$ delay (= 1 CLK)

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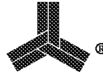
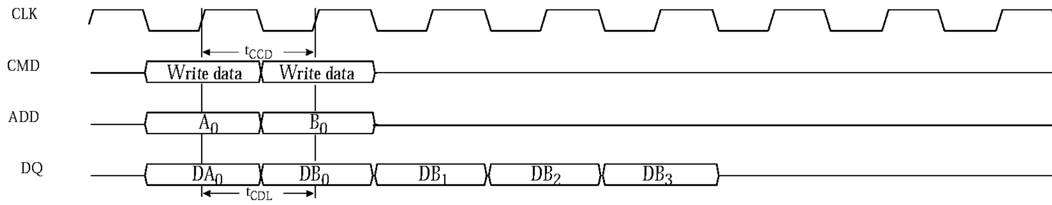


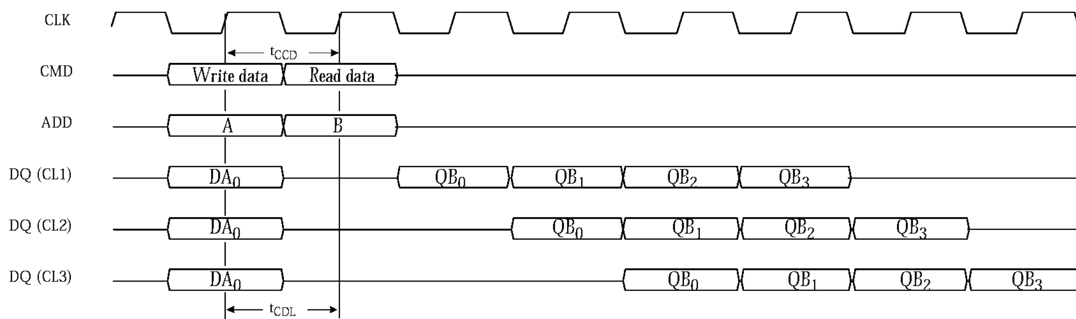
write interrupted by write (BL = 4)



t_{CCD} = $\overline{CAS}$ to $\overline{CAS}$ delay (= 1 CLK)

t_{CDL} = last address in to new column addres delay (= 1 CLK)

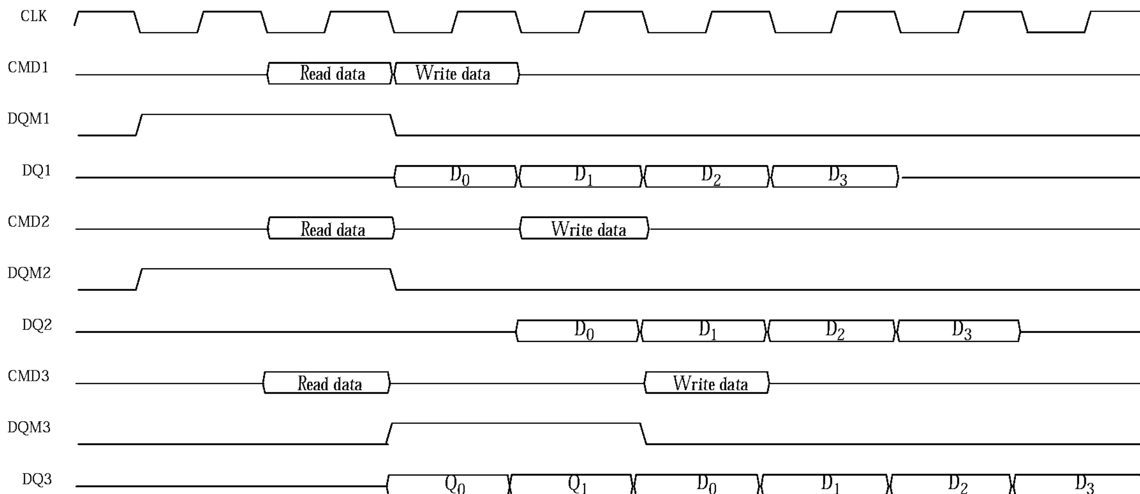
write interrupted by read (BL = 4)



t_{CCD} = $\overline{CAS}$ to $\overline{CAS}$ delay (= 1 CLK)

t_{CDL} = last address in to new column addres delay (= 1 CLK)

read interrupted by write (CL = 1, BL = 4)



To prevent bus contention, maintain a gap between data in and data out.

SGRAM

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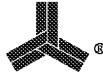
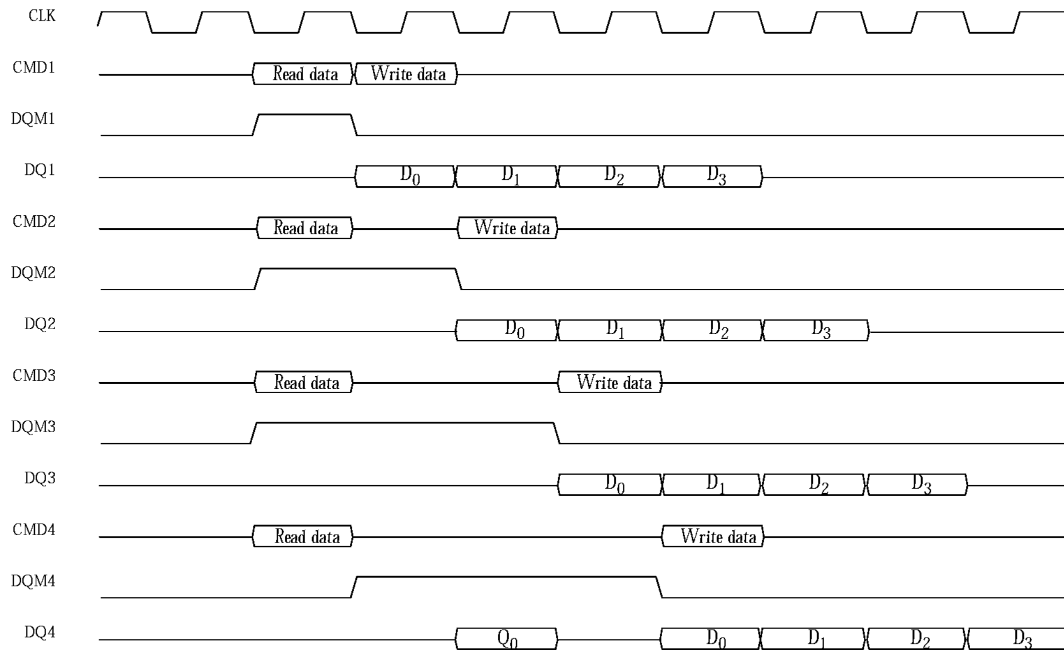
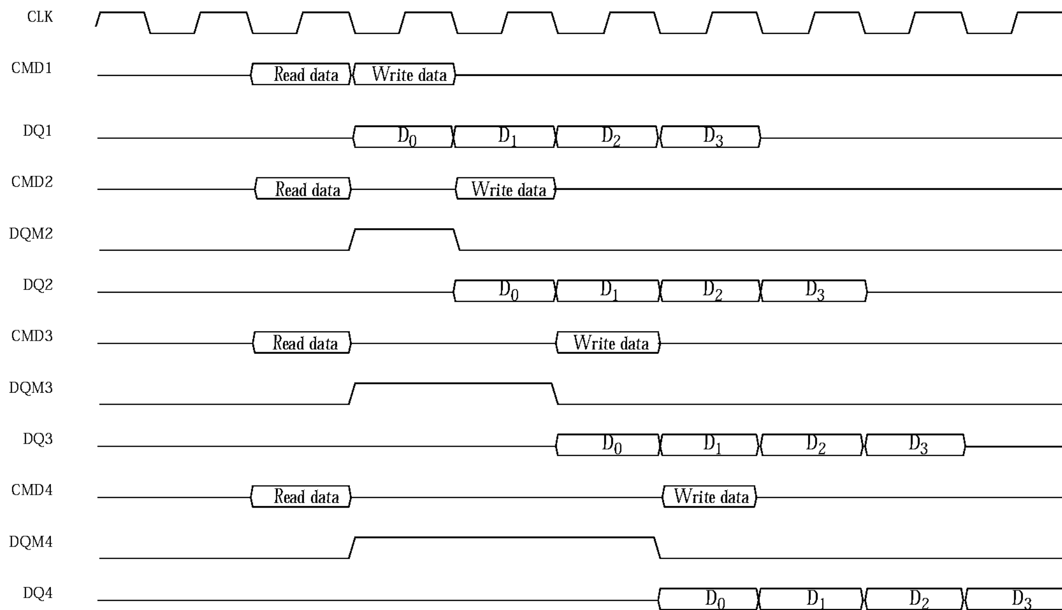


read interrupted by write (CL = 2, BL = 4)



To prevent bus contention, maintain a gap between data in and data out.

read interrupted by write (CL = 3, BL = 4)



To prevent bus contention, maintain a gap between data in and data out.

SGRAM

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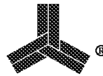
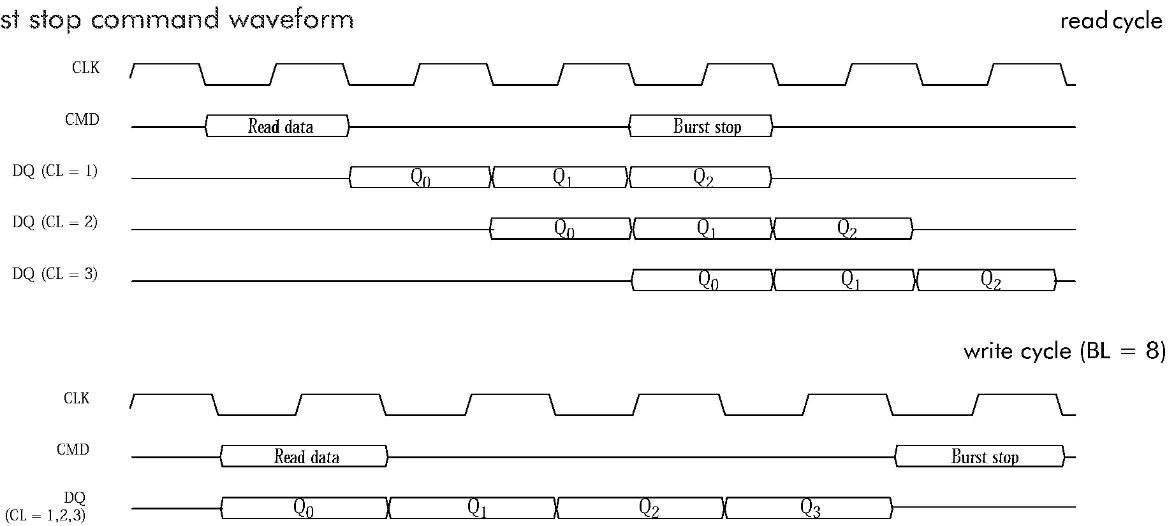


Burst termination

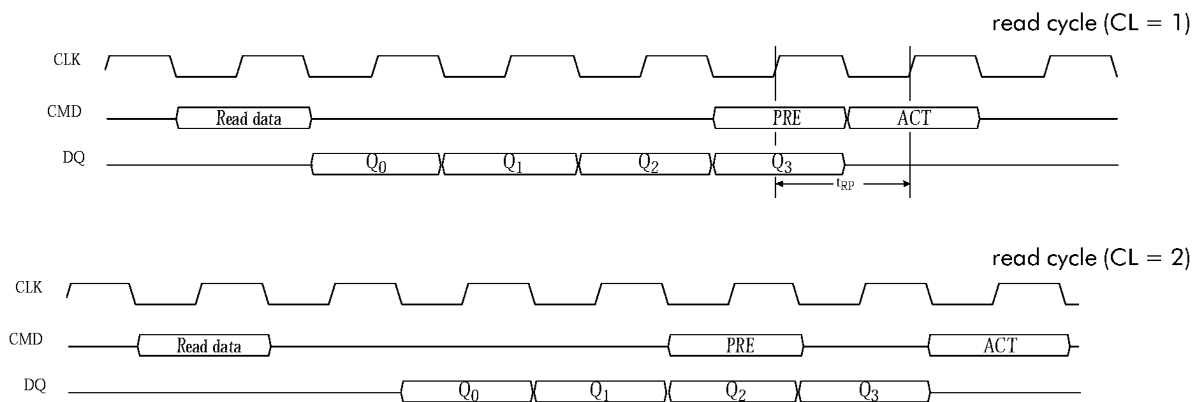
Burst operations may be terminated with a Read, Write, Burst Stop, or Precharge command. When Burst Stop is asserted during the read cycle, burst read data is terminated and the data bus goes to Hi-Z after CAS latency. When Burst Stop is asserted during the write cycle, burst write data is terminated and the databus goes to HI-Z simultaneously.

Burst stop command waveform



Precharge termination

A Precharge command terminates a burst read/write operation during the read cycle. The same bank can be activated after meeting t_{RP}



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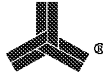
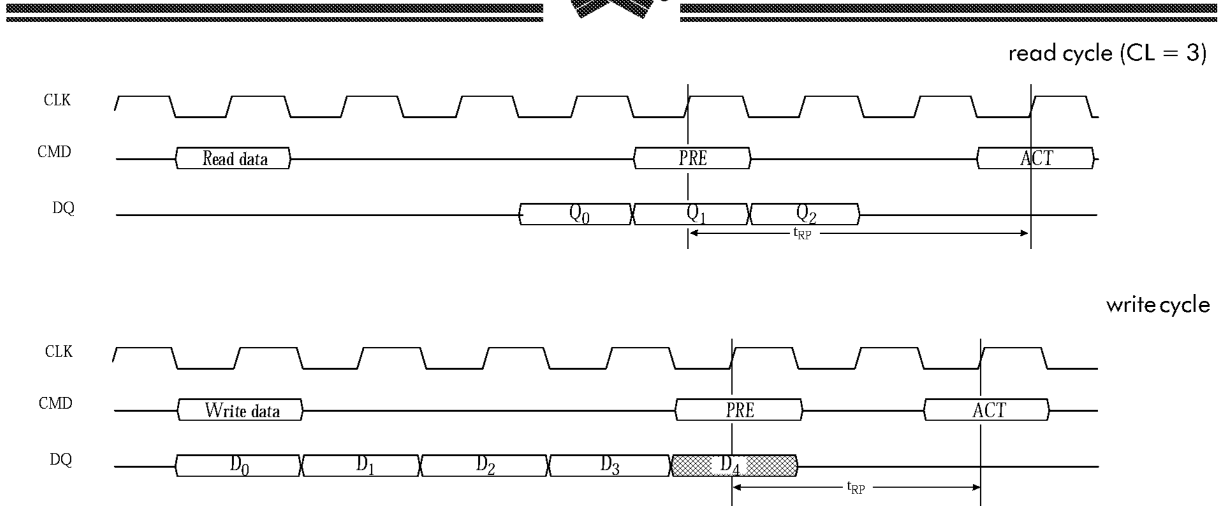
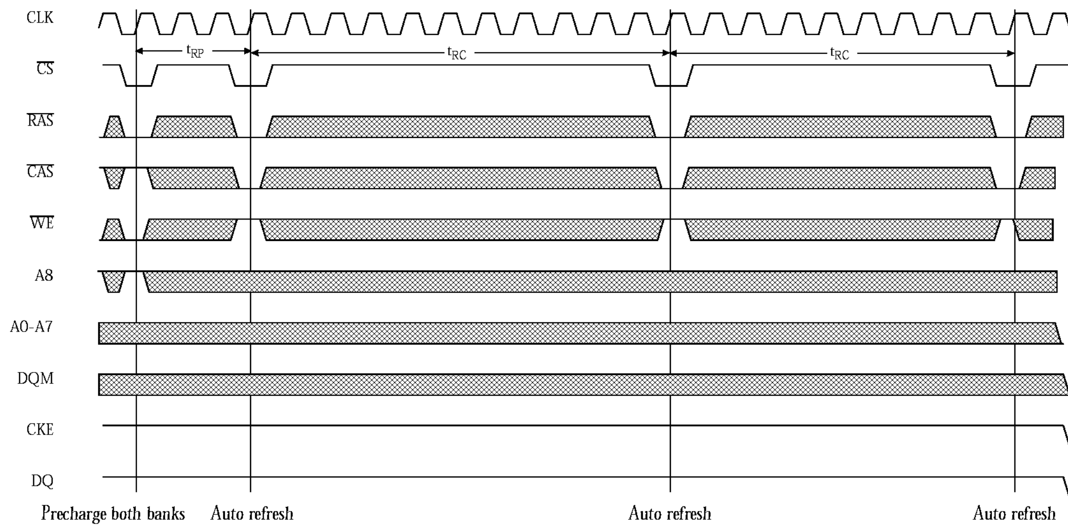




Auto refresh waveform



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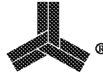
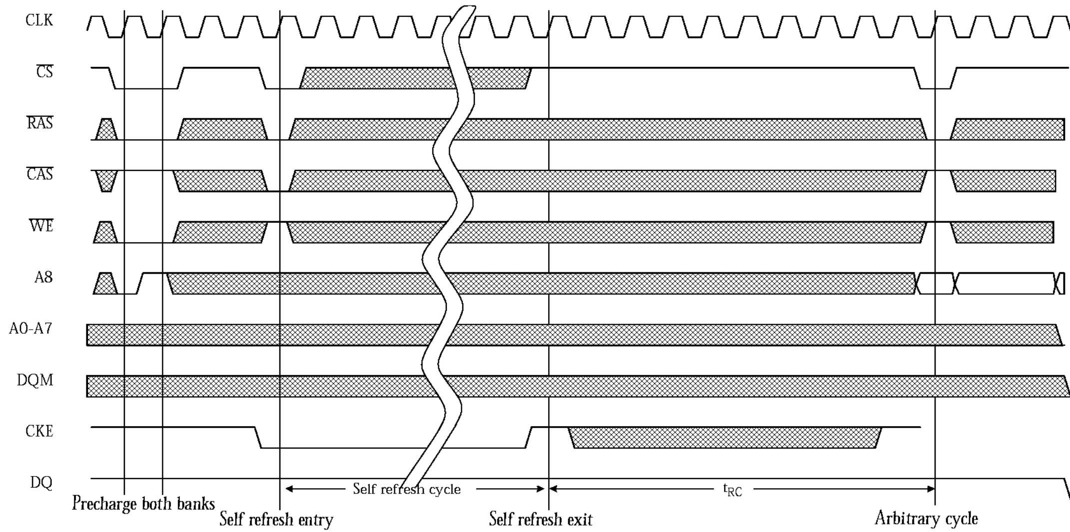
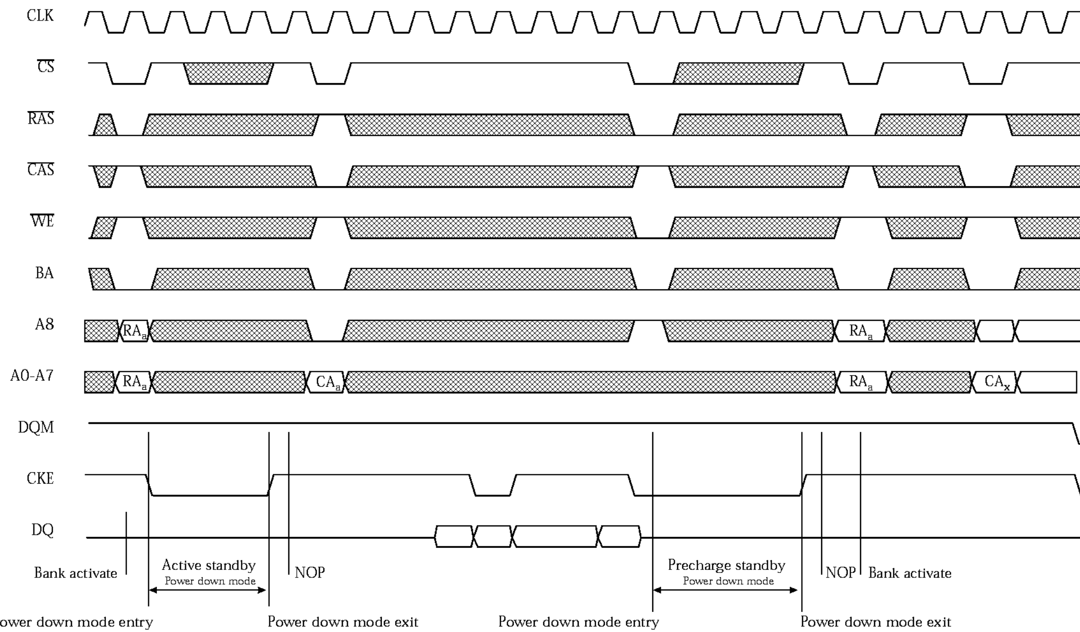


Self refresh waveform



Power down mode waveform

(CL = 3)



Enter power down mode by pulling CKE low.

All input/output buffers (except CKE buffer) are turned off in power down mode.

When CKE goes high, command input must be equal to no operation at next CLK rising edge.

SGRAM

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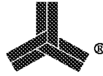
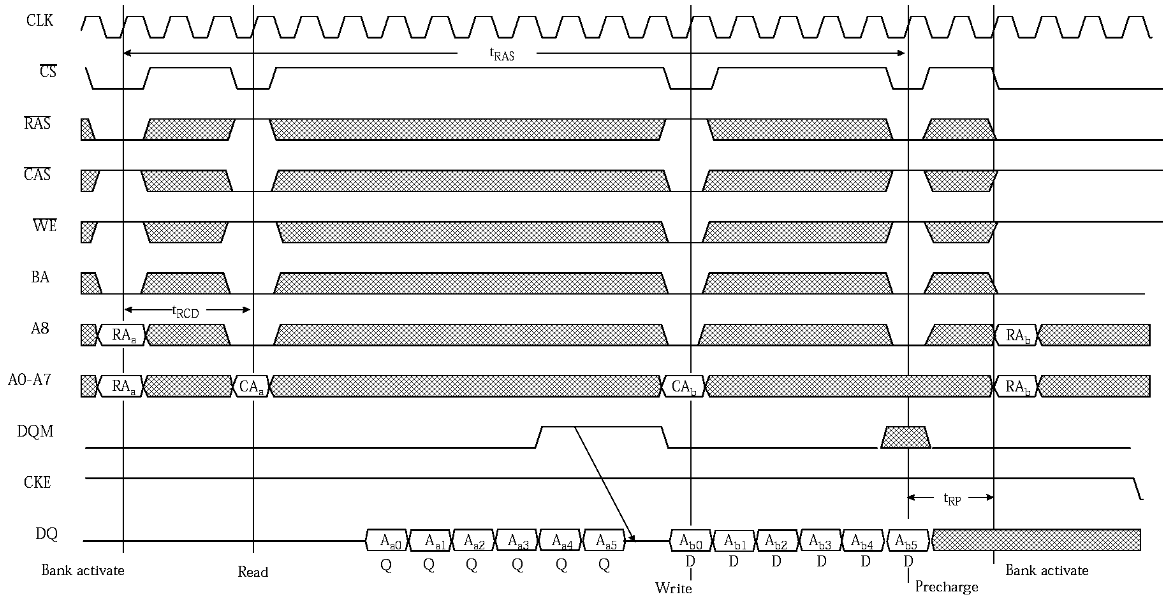


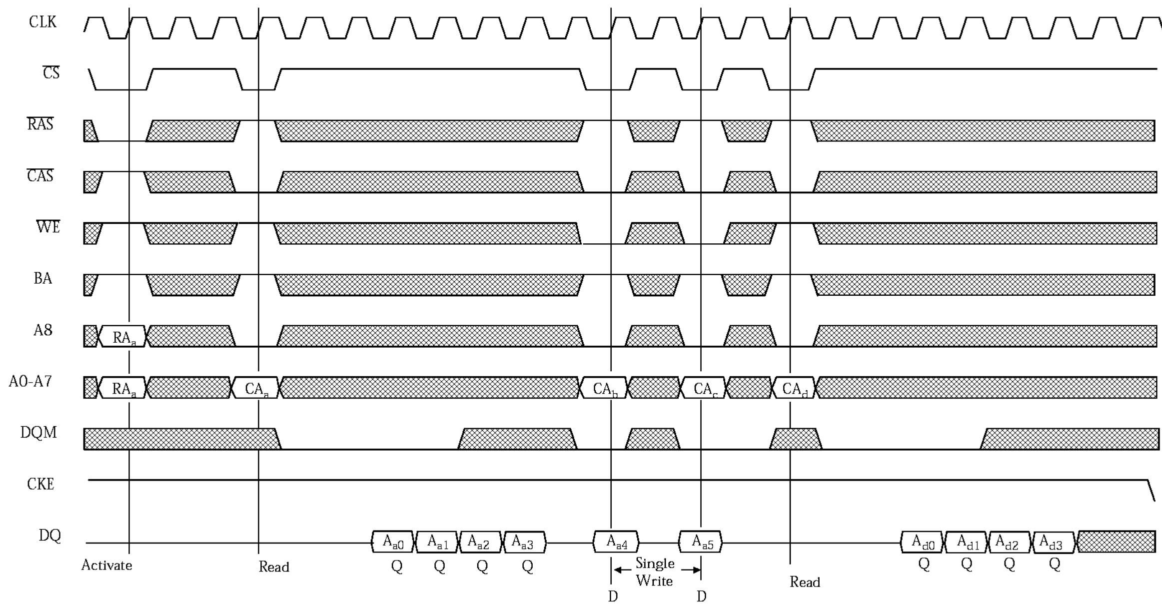
Read/write waveform

(BL = 8, CL = 3)



Burst read/single write waveform

(BL = 4, CL = 3)



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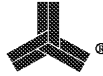
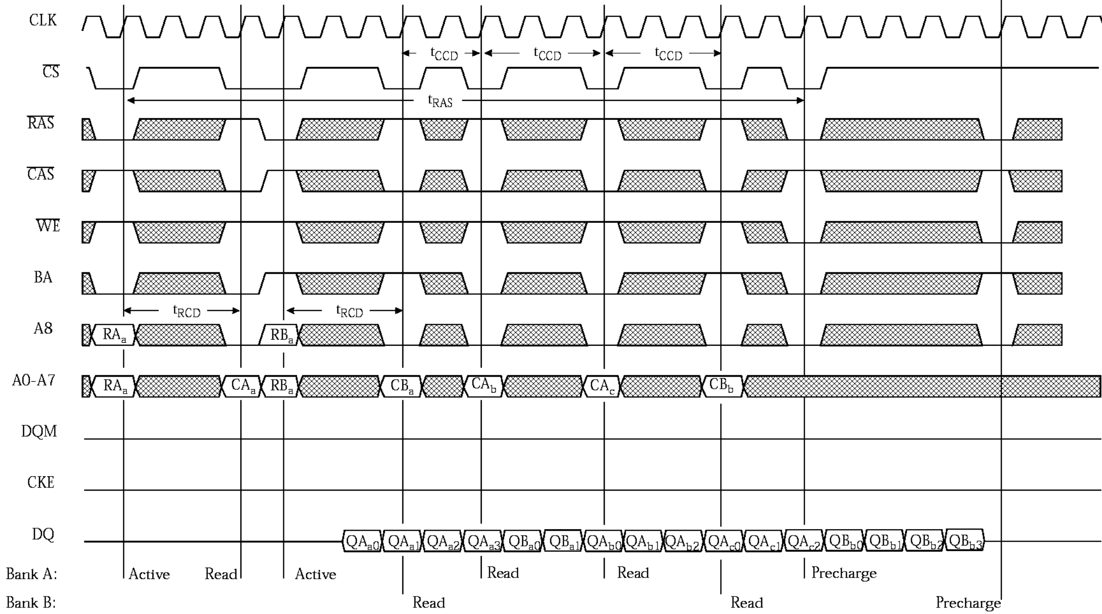


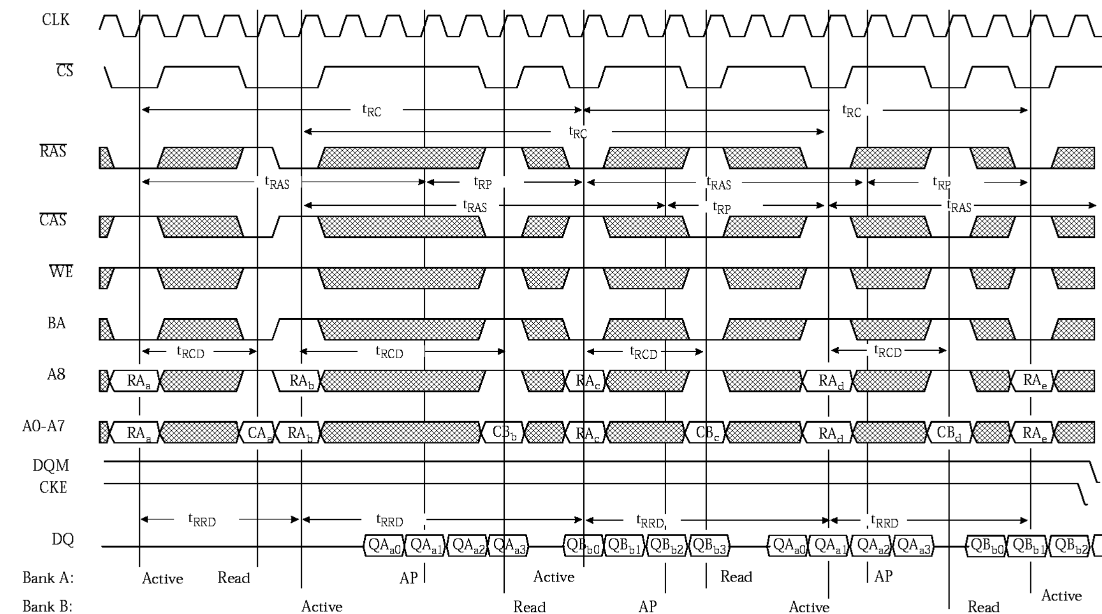
Interleaved bank read waveform

(BL = 4, CL = 3)



Interleaved bank read waveform

(BL = 4, CL = 3, Autoprecharge)



AP = internal precharge begins

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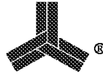
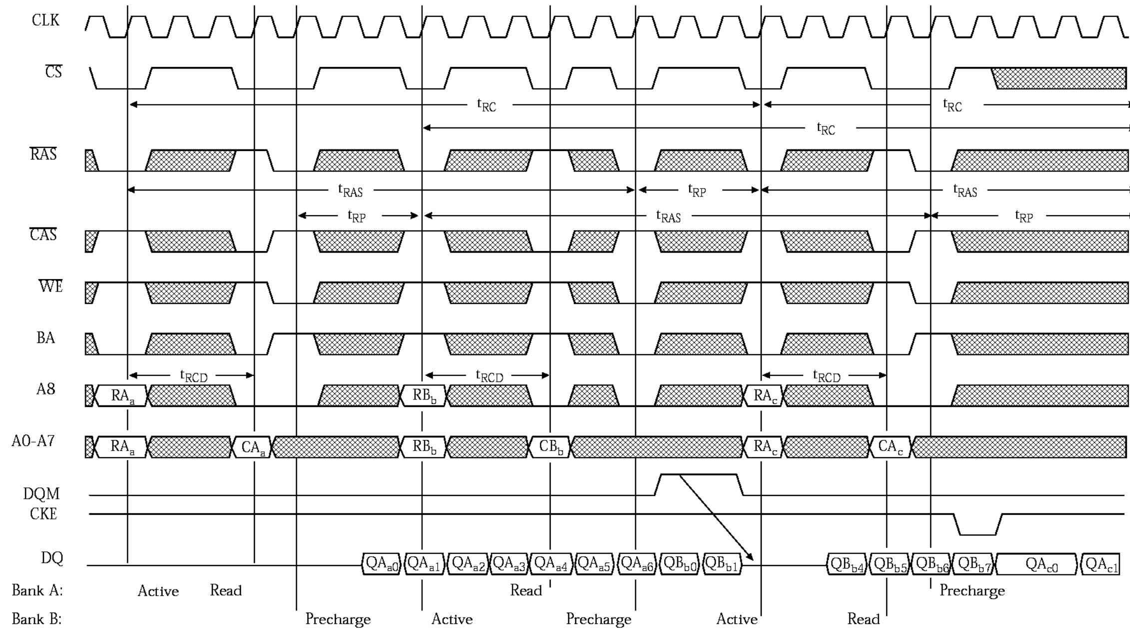


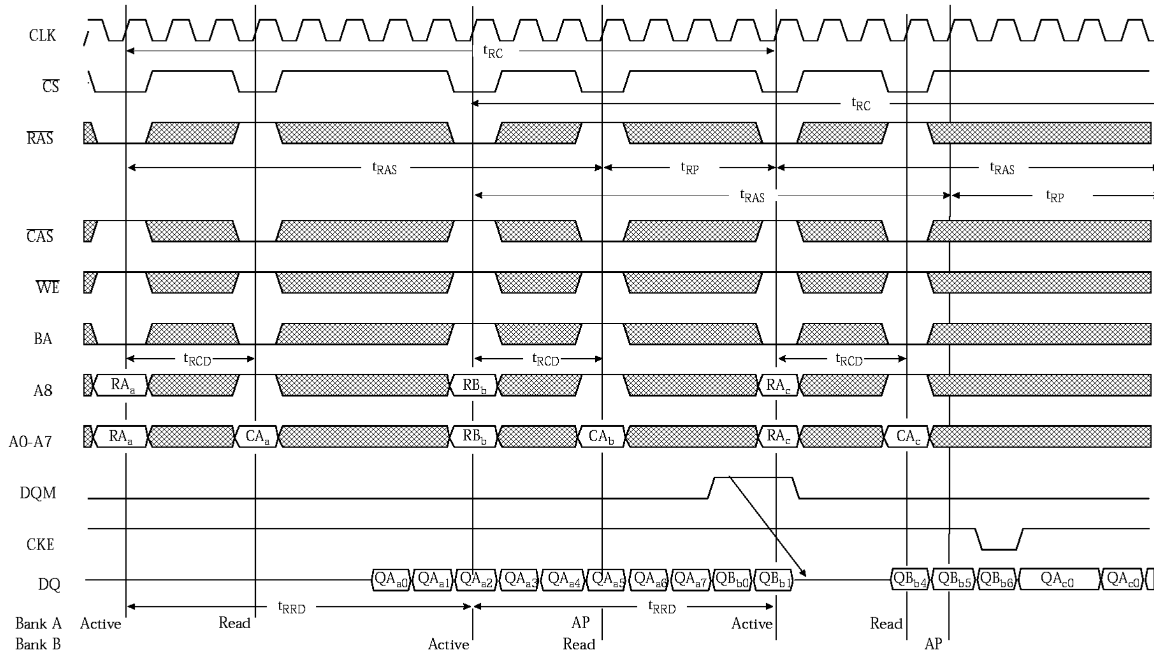
Interleaved bank read waveform

(BL = 8, CL = 3)



Interleaved bank read waveform

(BL = 8, CL = 3, Autoprecharge)



AP = internal precharge begins

SGRAM

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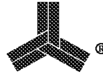
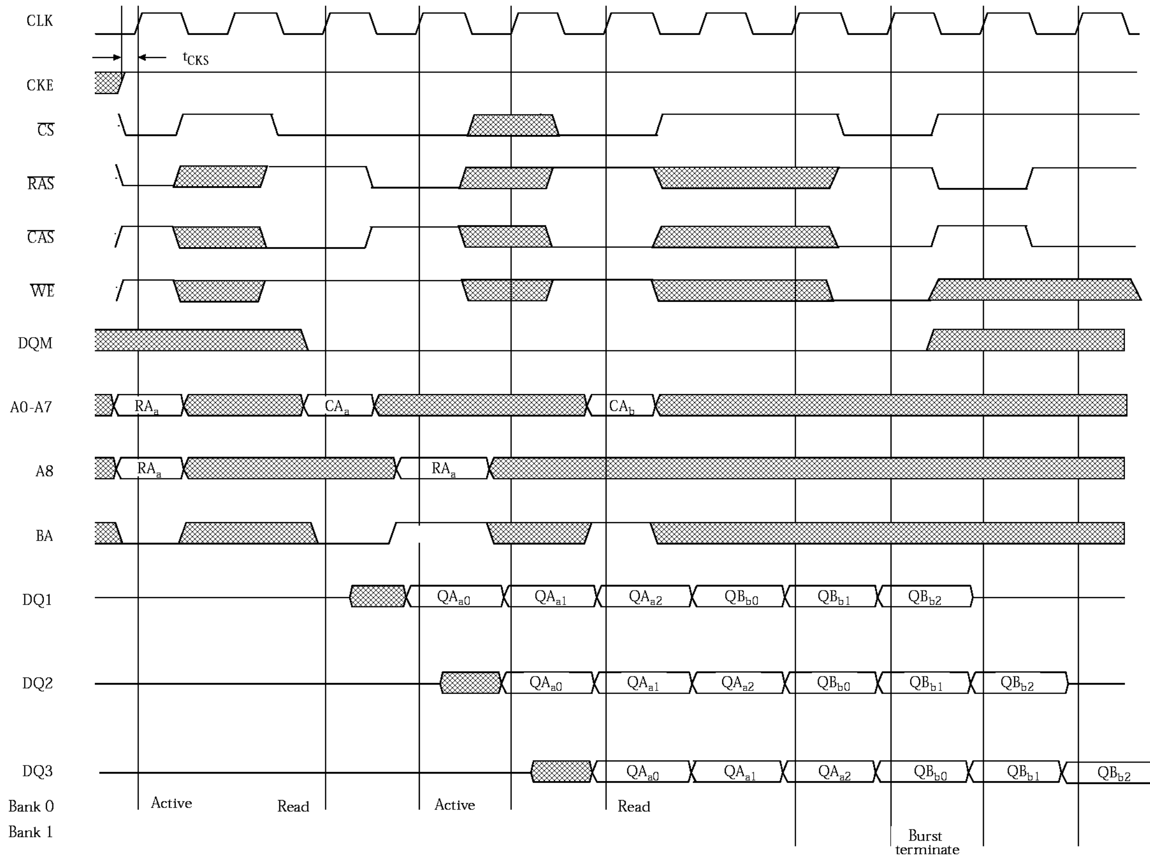


Full page interleaved burst read waveform



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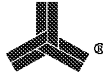
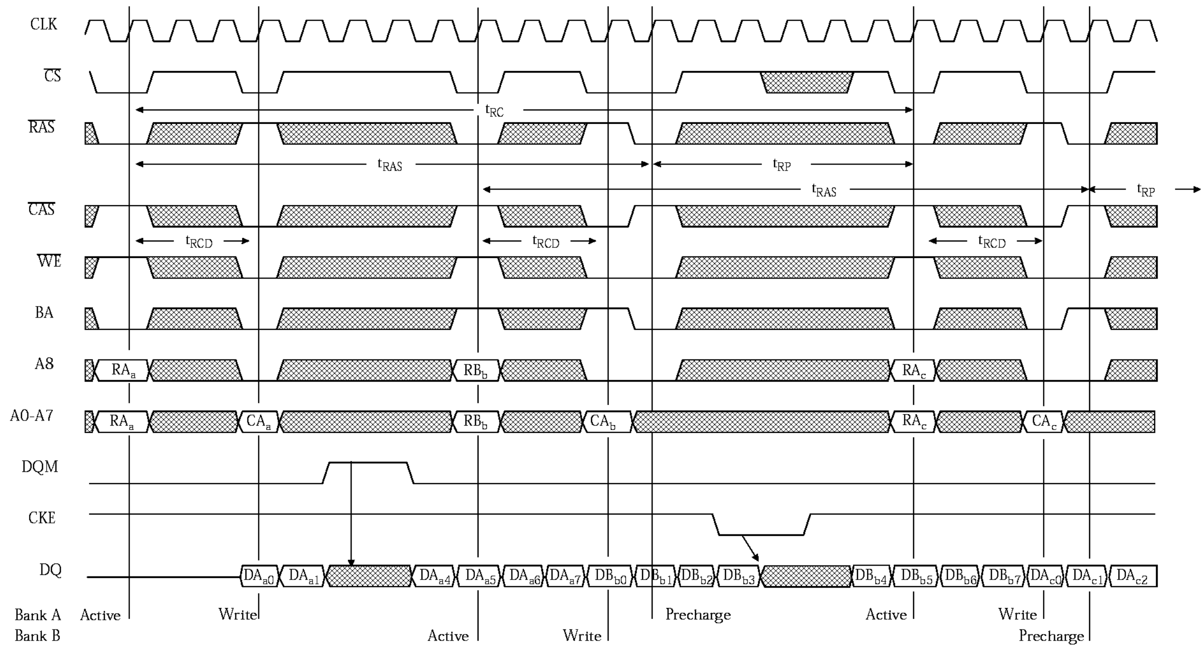
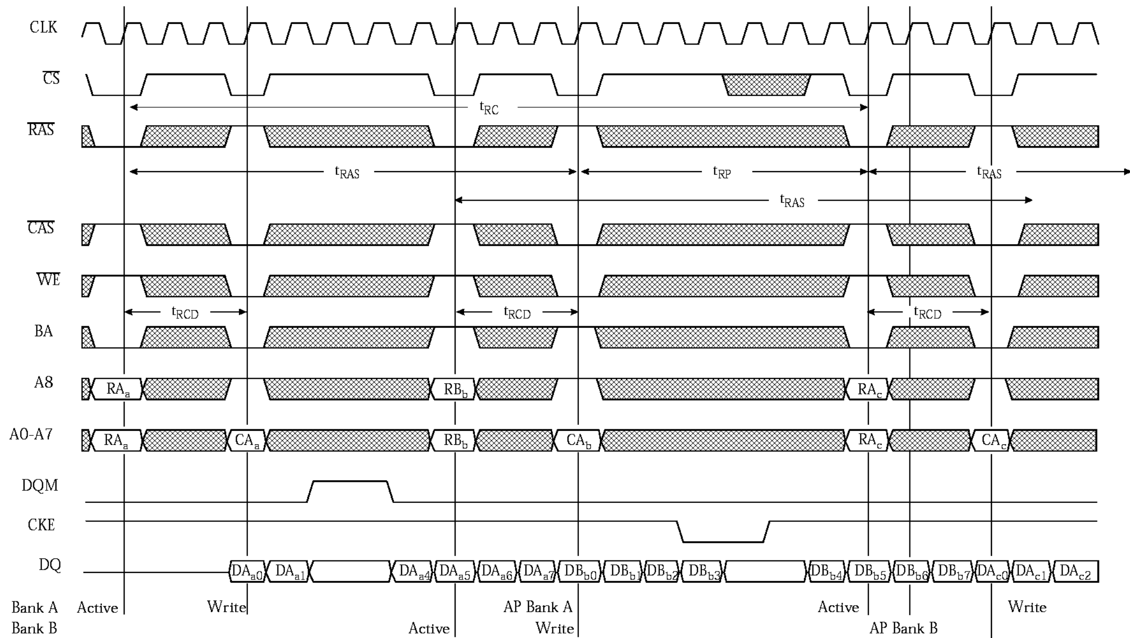


Interleaved bank write waveform (BL = 8)



Interleaved bank write (BL = 8, Autoprecharge)



AP = internal precharge begins

SGRAM

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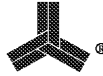
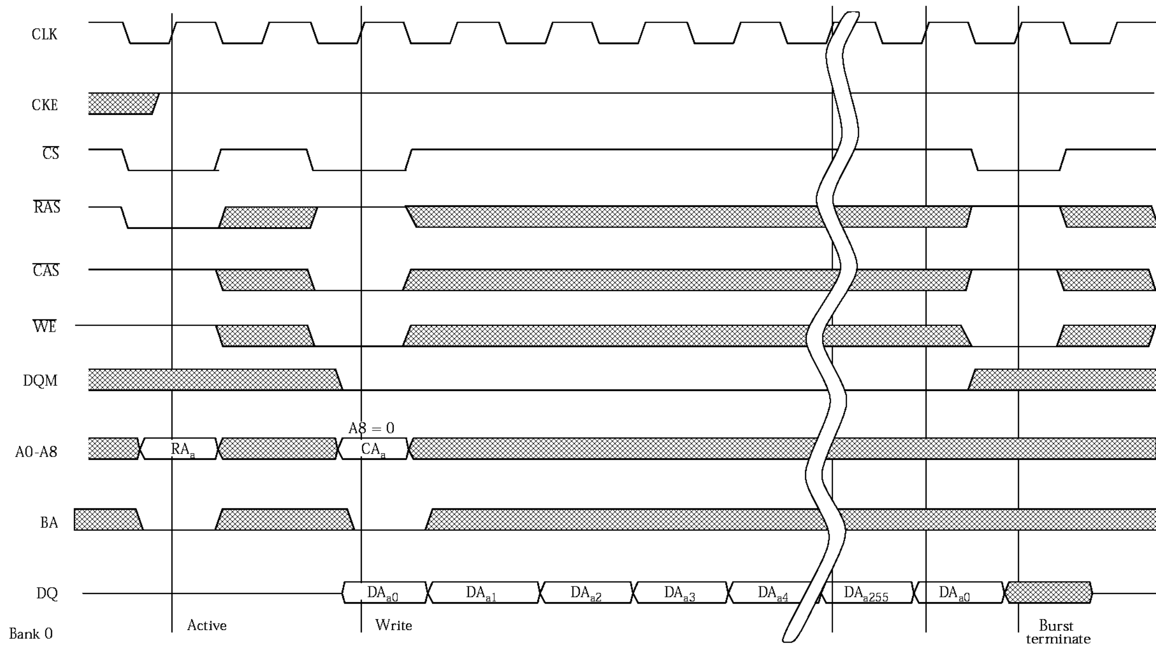


Full page burst write waveform



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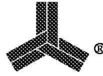
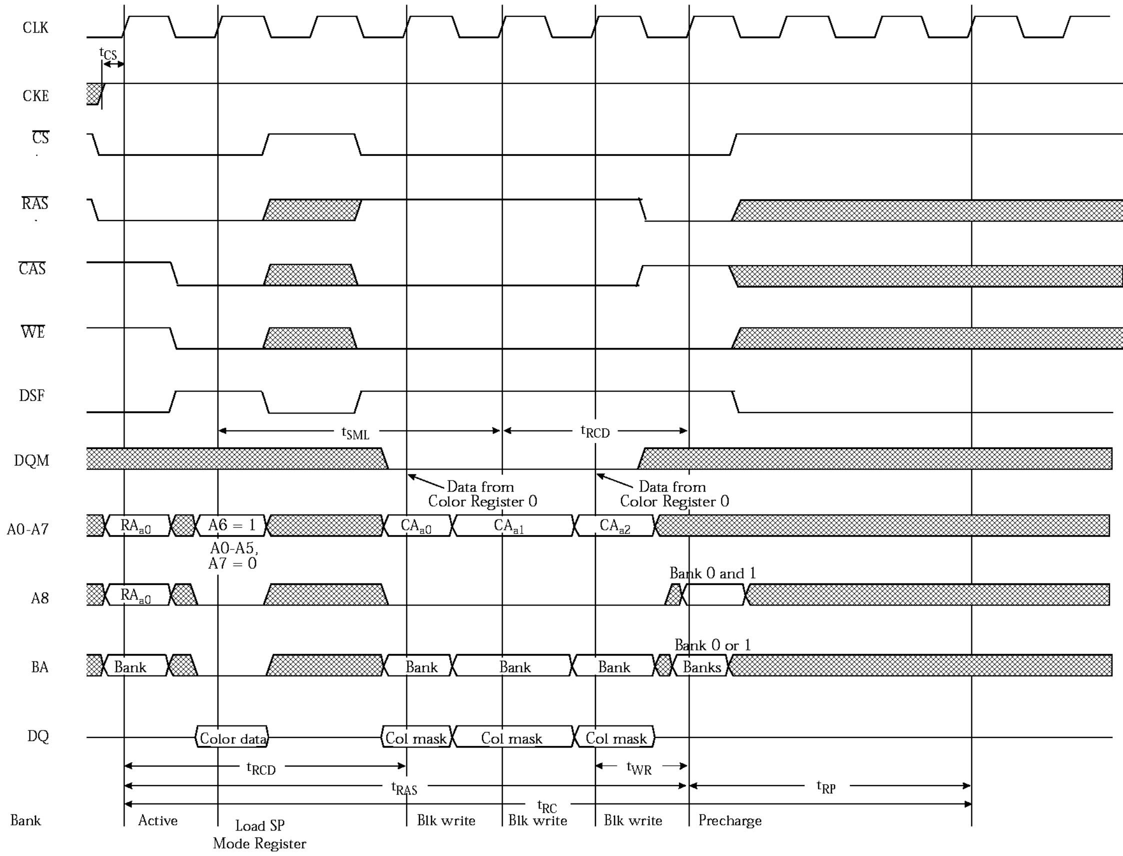


Block write

1 color register



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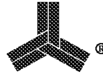
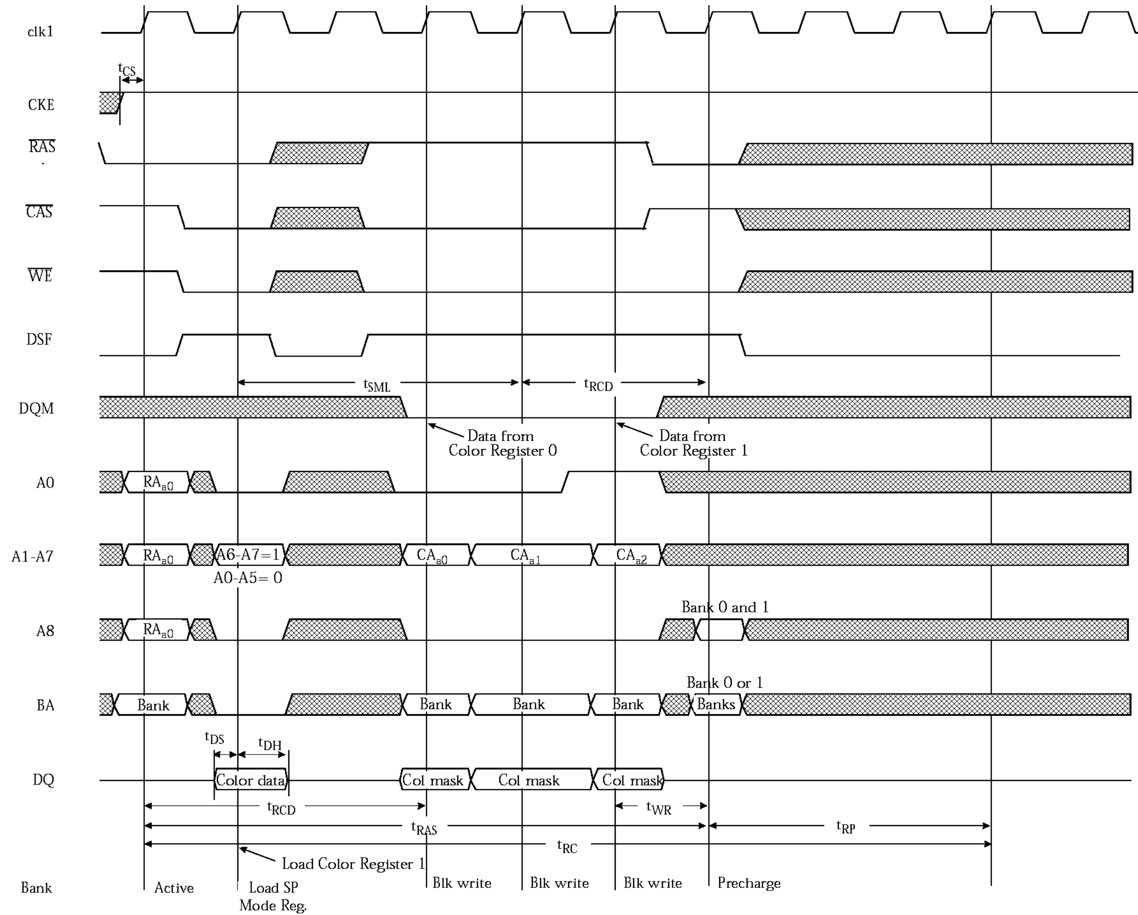


Block write

multiple color register



SGRAM

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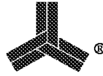
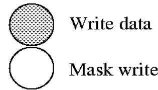
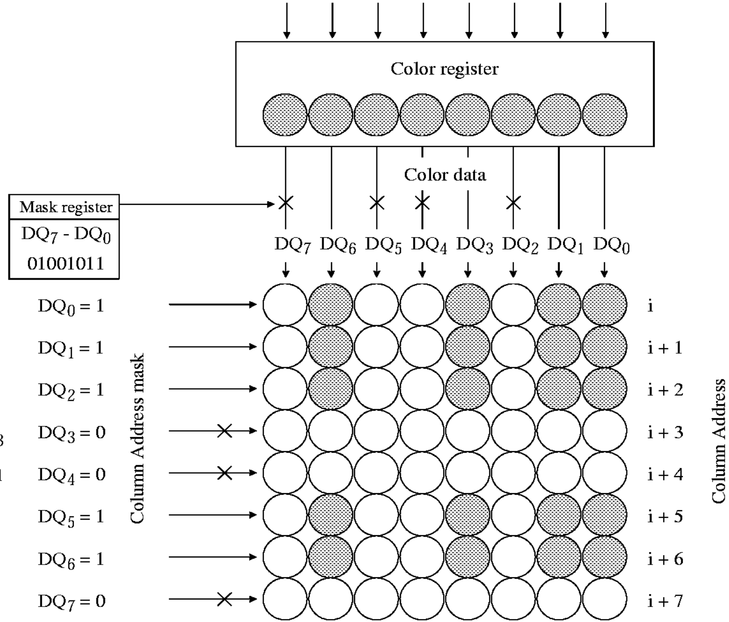


Block write diagram





Column mask

DQ_{0-7}: Column mask for DQ_{0-7}

DQ_{8-15}: Column mask for DQ_{8-15}

DQ_{16-23}: Column mask for DQ_{16-23}

DQ_{24-31}: Column mask for DQ_{24-31}

Write per bit

Mask data = Mask register + DQM

SGRAM

Package dimensions

	(P)QFP		TQFP	
	Min	Max	Min	Max
A1	0.25	0.45	0.05	0.15
A2	2.57	2.87	1.35	1.45
b	0.20	0.40	0.22	0.38
c	0.10	0.20	0.09	0.20
D	13.90	14.10	13.90	14.10
E	19.90	20.10	19.90	20.10
e	0.65 nominal		0.65 nominal	
Hd	17.00	17.40	15.90	16.10
He	23.00	23.40	21.90	22.10
L	0.65	0.95	0.45	0.75
L1	1.60 nominal		1.00 nominal	
α	0°	10°	0°	7°

Dimensions in millimeters

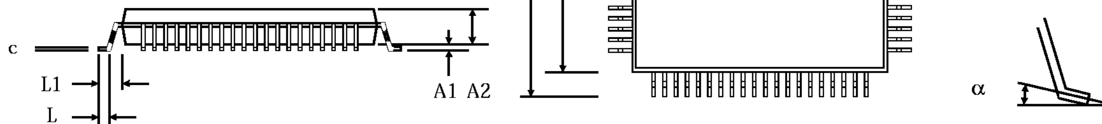
Hd

D

b

e

He E



α

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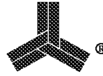

AC test conditions

- Input reference levels of V_{IH} = 2.4V and V_{IL} = 0.8V
- Output reference levels = 1.4V
- Input rise and fall times: 1 ns

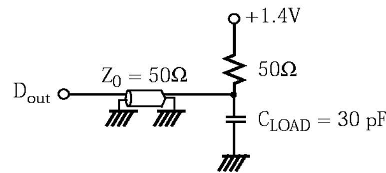

Figure A: Equivalent output load

Capacitance

f = 1 MHz, T_a = 25°C, V_{CC} = 3.3V

Parameter	Symbol	Signals	Max	Unit
Input capacitance	C_{IN1}	A0 to BA	5	pF
	C_{IN2}	DQM, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CLK, CKE, DSF	5	pF
I/O capacitance	$C_{I/O}$	DQ0 to DQ31	5	pF

Part numbering system

AS4	LC	XXXS0	-XX	XX	C
DRAM prefix	LC = 3.3V CMOS	Device number for synchronous DRAM	1/frequency	Package (device dependent): Q = LQFP TQ = TQFP	Commercial temperature range, 0 ℃ to 70 ℃

Ordering codes

Package/Frequency	150 MHz	133 MHz	100 MHz
Plastic PQFP, 100-pin, 14mm × 20mm	AS4LC256K32S0-150QC	AS4LC256K32S0-133QC	AS4LC256K32S0-100QC
Plastic TQFP, 100-pin, 14mm × 20mm	AS4LC256K32S0-150TQC	AS4LC256K32S0-133TQC	AS4LC256K32S0-100TQC

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