AmPALC29MA16

24-Pin E^2-Based CMOS Programmable Array Logic
ADVANCE INFORMATION

Distinctive Characteristics

- High-performance semi-custom logic replacement; Electrically Erasable (E^2) technology allows reprogrammability
- 16 bidirectional user-programmable I/O logic macrocells for Combinatorial/Registered/Latched operation
- Output Enable controlled by a pin or product terms
- Variable product term distribution for increased design flexibility
- Programmable clock selection with common pin clock/latch enable (LE) or individual product term clock/LE with LOW/HIGH clock/LE polarity
- Register/Latch PRELOAD permits full logical verification
- Available in high-speed (t_{PD} = 35 ns, f_{MAX} = 20 MHz) and standard-speed (t_{PD} = 45 ns, f_{MAX} = 15.0 MHz) versions
- 100% post-programming functional yield (PPFY), fast programming and excellent reliability assured through proven E^2PROM technology
- Full-function AC and DC testing at the factory
- 24-pin 300-mil DIP and 28-pin chip carrier packages

General Description

The AmPALC29MA16 is a high-speed, E^2-based CMOS Programmable Array Logic device designed for general logic replacement in TTL or CMOS digital systems. It offers high-speed, low-power consumption, high programming yield, fast programming and excellent reliability. Programmable logic devices (PLDs) combine the flexibility of custom logic with the off-the-shelf availability of standard products, providing major advantages over other semicustom solutions such as gate arrays and standard cells, including reduced development time and low up-front development cost.

The AmPALC29MA16 uses the familiar sum-of-products (AND-OR) structure, allowing users to customize logic functions by programming the device for specific applications. It provides up to twenty-nine array inputs and sixteen outputs. It incorporates AMD's unique input/output logic macrocell which provides flexible input/output structure and polarity, flexible feedback selection, multiple Output Enable choices, and a programmable clocking scheme. The macrocells can be individually programmed as "Combinatorial", "Registered", or "Latched" with active-HIGH or active-LOW polarity. The flexibility of the logic macrocells permits the system designer to tailor the device to particular application requirements.

Increased logic power has been built into the AmPALC29MA16 by providing a variable number of logical product terms per output. Eight outputs have four product terms each, four outputs have eight product terms each, and the other four outputs have twelve product terms each. This variable product-term distribution allows complex functions to be implemented in a single PAL device. Each output can be dynamically controlled by a common Output Enable pin or an individual Output Enable product terms. Each output can also be permanently enabled or disabled.

System operation has been enhanced by the addition of common asynchronous-PRESET and RESET product terms and a power-up RESET feature. The AmPALC29MA16 also incorporates PRELOAD and Observability functions which permit full logical verification of the design.

The AmPALC29MA16 is offered in the space-saving 300-Mil DIP package as well as chip carrier surface-mount packages.

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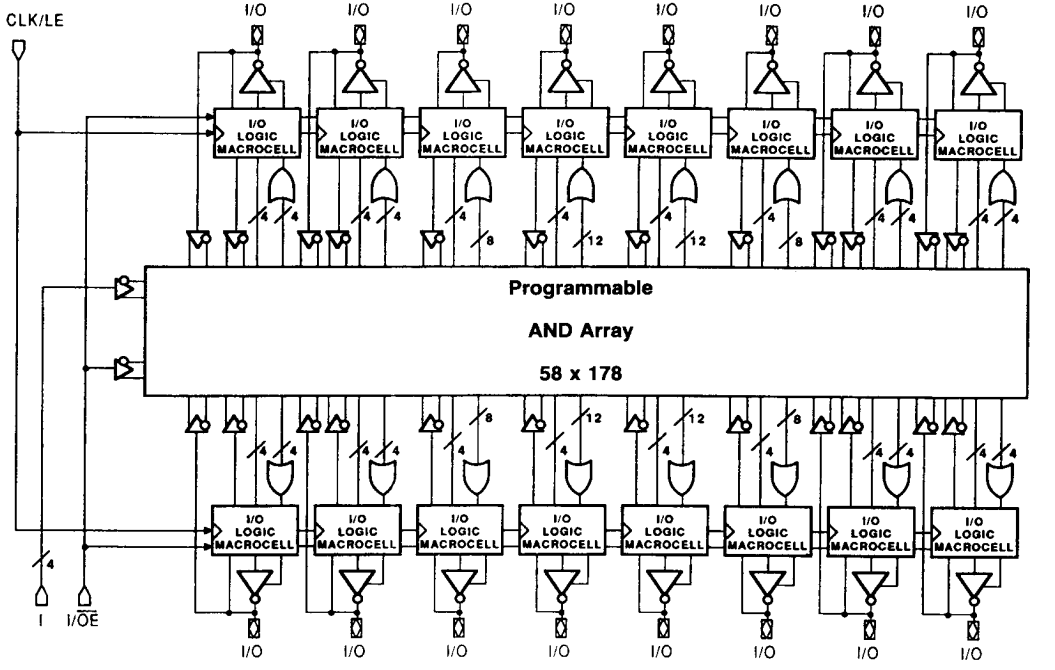
JANUARY 1988

Block Diagram



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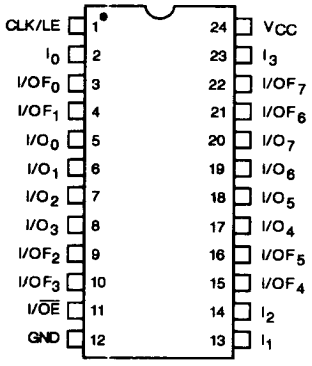
Connection Diagrams

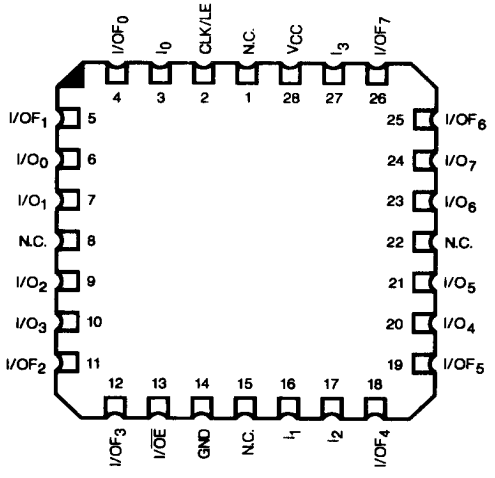
Top View

DIPs



CD010272

LCC*



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*Also available in PLCC. Pinouts identical to LCC.

Note: Pin 1 is marked for orientation.

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Pin Description

The following describes the functionality of all the pins on the 24-pin DIP. The 28-pin chip carrier has the same functionality with NO CONNECTS on pins 1,8,15,22.

CLK/LE (PIN 1):
Used as dedicated clock/latch enable pin for all registers/latches on the device if so selected. (See I/O Logic Macrocell Configurations.) This pin is a clock pin for macrocells configured as registers and a latch enable pin for macrocells configured as latches.

I/$\overline{OE}$ PIN (PIN 11):
Used as a dedicated input pin to the AND array or as the Output Enable control pin (Active LOW) for all macrocells with pin-controlled Output Enable selected.

I_0-I_3 (PINS 2,13,14,23):
Dedicated input pins.

I/OF_0-I/OF_7 (PINS 3,4,9,10,15,16,21,22):
Eight bidirectional I/O pins with two independent feedback paths to the AND array. The first feedback path is a dedicated I/O pin feedback to the AND array for combinatorial input. The second feedback path consists of direct register/latch feedback to the array (see Figure 1).

I/O_0-I/O_7 (PINS 5,6,7,8,17,18,19,20):
Eight bidirectional I/O pins with user-programmable register/latch or I/O pin feedback to the AND array (see Figure 1).

V_{CC} (PIN 24):
Supply Voltage

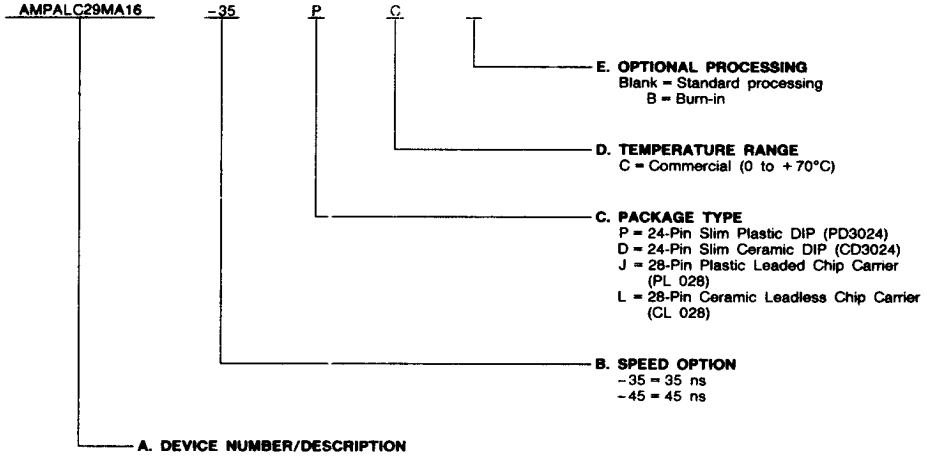
GND (PIN 12):
Circuit Ground

Ordering Information

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

A. Device Number
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AmPALC29MA16-35, -45	PC, DC, DCB, JC, LC, LCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

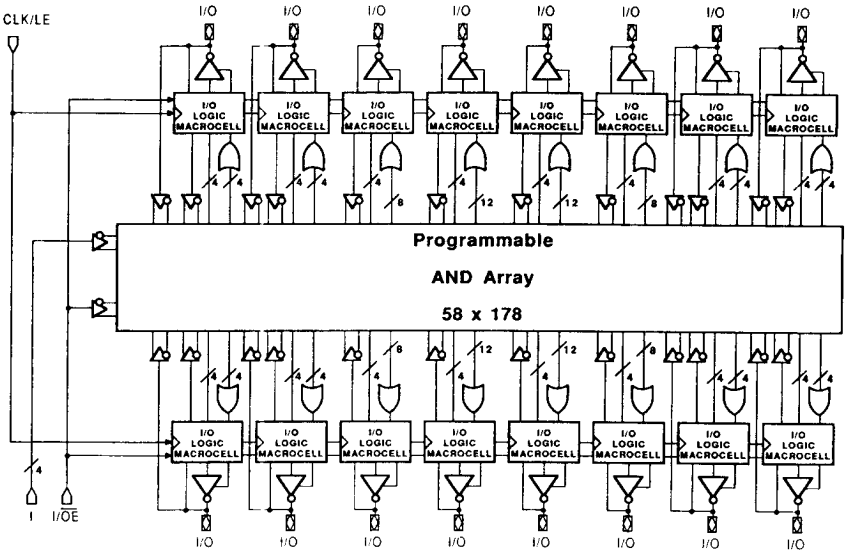
Functional Description

Inputs

The AmPALC29MA16 has 29 inputs to drive each product term (up to 58 inputs with both TRUE and complement versions available to the AND array) as shown in the block diagram below. Of these 29 inputs, 4 are dedicated inputs. 16 are from 8 I/O logic macrocells with 2 feedbacks, 8 are from other I/O logic macrocells with single feedback and 1 is for I/$\overline{OE}$ input.

Initially the AND-array gates are disconnected from all the inputs. This condition represents a logical TRUE to the AND array. By selectively programming the E^2cells, the AND array may be connected to either the TRUE input or the complement input. When both the TRUE and complement inputs are connected, a logical FALSE results at the output of the AND gate.

Block Diagram



Product Terms

The degree of programmability and complexity of a PAL device is determined by the number of connections that form the programmable-AND and OR gates. Each programmable-AND gate is called a product term. The AmPALC29MA16 has 178 product terms. 112 of these product terms provide logic capability and others are architectural product terms. Among the control product terms, 1 is for Observability, and 1 is for PRELOAD. The Output Enable of each macrocell can be programmed to be controlled by a common Output Enable pin or an individual product term. It may be also permanently enabled or permanently disabled. In addition, independent product terms for each marcocell control PRESET, RESET and CLK/LE.

Each product term on the AmPALC29MA16 consists of a 58-input AND gate. The outputs of these AND gates are connected to a fixed-OR plane. Product terms are allocated to OR gates in a variable distribution across the device ranging from 4-to-12 wide, with an average of 7 logical product terms per output. Increased number of product terms per output allows more complex functions to be implemented in a single PAL device. This flexibility aids in implementing functions such as counters, exclusive-OR functions, or complex state machines, where different states require different numbers of product terms.

Individual asynchronous-PRESET and RESET product terms are connected to all Registered/Latched inputs/outputs.

When the asynchronous-PRESET product term is asserted (HIGH) all the registers/latches will immediately be loaded with a HIGH, independent of the clock. When the asynchronous-RESET product term is asserted (HIGH) all the registers/latches will be immediately loaded with a LOW, independent of the clock. The actual output state will depend on the macrocell polarity selection. The latches must be in latched mode (not transparent mode) for the RESET/PRESET, PRELOAD, and power-up RESET modes to be meaningful.

Input/Output Logic Macrocells

The I/O logic macrocell allows the user the flexibility of defining the architecture of each input or output on an individual basis. It also provides the capability of using the associated pin either as an input or an output.

The AmPALC29MA16 has 16 macrocells, one for each I/O pin. Each I/O macrocell can be programmed for combinatorial, registered or latched operation (see Figure 1). Combinatorial output is desired when the PAL device is used to replace combinatorial glue logic. Registers are used in synchronous logic applications while latches are used in asynchronous applications where speed is critical. The output polarity for each macrocell in each of the three modes of operation is user-selectable, allowing complete flexibility of the macrocell configuration.

Eight of the macrocells (I/OF_0-I/OF_7) have two independent feedback paths to the AND array (see Figure 1). The first is a dedicated I/O pin feedback to the AND array for combinatorial input. The second path consists of a direct register/latch feedback to the array. If the pin is used as a dedicated input using the first feedback path, the register/latch feedback path is still available to the AND array. This path provides the capability of using the register/latch as a buried state register/latch. The other eight macrocells have a single feedback path to the AND array. This feedback is user-selectable as either an I/O pin or a register/latch feedback.

Each macrocell can provide true input/output capability. The user can select each macrocell register/latch to be driven by either the output generated by the AND-OR array or the I/O pin. When the I/O pin is selected as the input, the feedback path provides the register/latch input to the array. When used as an input, each macrocell is also user-programmable for registered, latched, or combinatorial input.

The AmPALC29MA16 has one dedicated CLK/LE pin and an individual CLK/LE product term. All macrocells have a programmable select to choose between these two as the clock or the latch enable signal. These signals are clock signals for macrocells configured as registers and latch enable signal for macrocells configured as latches. The polarity of these CLK/LE signals is also individually programmable. Thus different registers can be driven by multiple clocks and clock phases.

The Output-Enable mode of each of the macrocells can be selected by the user. The I/O pin can be configured as an output pin (permanently enabled) or as an input pin (permanently disabled). It can also be configured as a dynamic I/O controlled by the Output Enable pin or by product term.

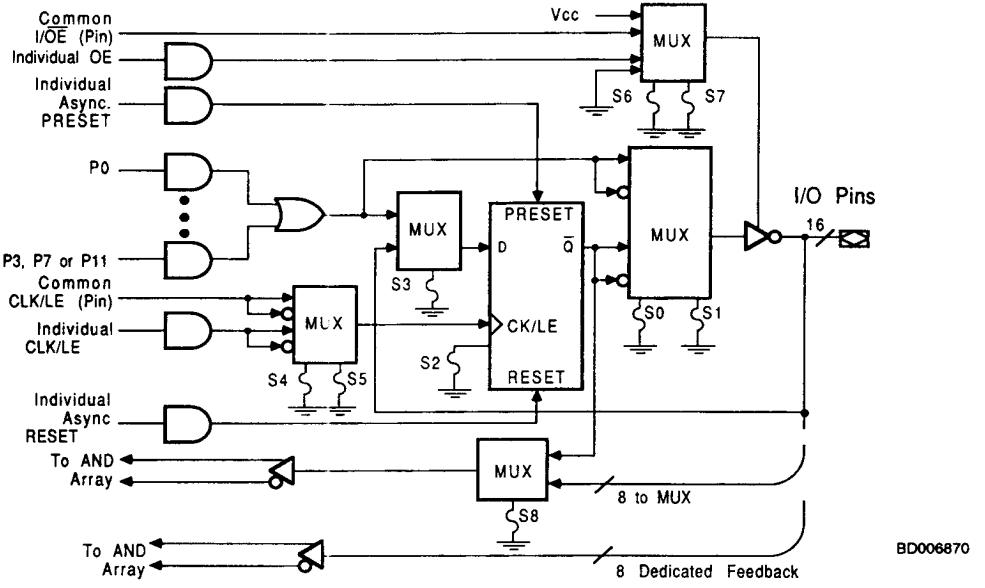


Figure 1. AmPALC29MA16 I/O Macrocell

I/O Logic Macrocell Configuration

AMD's unique I/O macrocell offers major benefits through its versatile, programmable input/output cell structure, multiple clock choices, flexible Output Enable and feedback selection. Eight I/O macrocells with single feedback contain nine E^2cells, while the other eight macrocells contain eight E^2cells for programming the input/output functions (see Table 1, Figure 2).

E^2cell S1 controls whether the macrocell will be combinatorial or registered/latched. S0 controls the output polarity (active-HIGH or active-LOW). S2 determines whether the input/output is a register or a latch. S3 allows the use of the macrocell as an input register/latch or as an output register/latch. It selects the direction of the data path through the register/latch. If connected to the usual AND-OR array output, the register/latch is an output connected to the I/O pin. If connected to the I/O pin, the register/latch becomes an input register/latch to the AND array using the feedback data path.

Programmable E^2cells S4 and S5 allow the user to select one of the four CLK/LE signals for each macrocell. S6 and S7 are used to control Output Enable as pin controlled, product term controlled, permanently enabled or permanently disabled. S8 is a feedback multiplexer for the macrocells with a single feedback path only.

In the virgin erased state (charged, disconnected), an architectural cell is said to have a value of "1" ; In the programmed state (discharged, connected), an architectural cell is said to have a value of "0".

Table 1. AmPALC29MA16 I/O Logic Macrocell Architecture Selections

S3	I/O Cell
1	Output Cell
0	Input Cell

S2	Storage Element
1	Register
0	Latch

S1	Output Type
1	Combinatorial
0	Register/Latch

S0	Output Polarity
1	Active LOW
0	Active HIGH

S8	Feedback*
1	Register/Latch
0	I/O

*Applies to macrocells with single feedback only.

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Table 1. AmPALC29MA16 I/O Logic Macrocell Clock Polarity & Output Enable Selections
(Cont'd.)

S4	S5	Clock Edge/Latch Enable Level
1	1	CLK/LE pin positive-going edge, active-HIGH LE
1	0	CLK/LE pin negative-going edge, active-LOW LE
0	1	CLK/LE PT positive-going edge, active-HIGH LE
0	0	CLK/LE PT negative-going edge, active-LOW LE

S6	S7	Output Buffer Control
1	1	Pin-Controlled 3-State Enable
1	0	PT-Controlled 3-State Enable
0	1	Permanently Enabled (Output only)
0	0	Permanently Disabled (Input only)

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1 = Erased State (Charged or disconnected)
0 = Programmed State (Discharged or connectec)

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Some Possible Configurations of the Input/Output Logic Macrocell

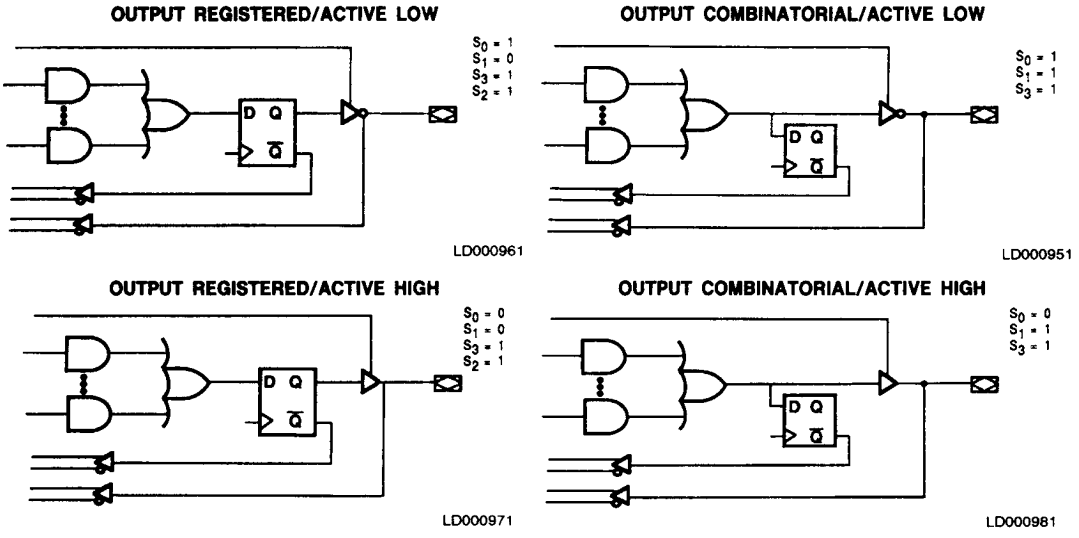

Figure 2a. Dual Feedback Macrocells

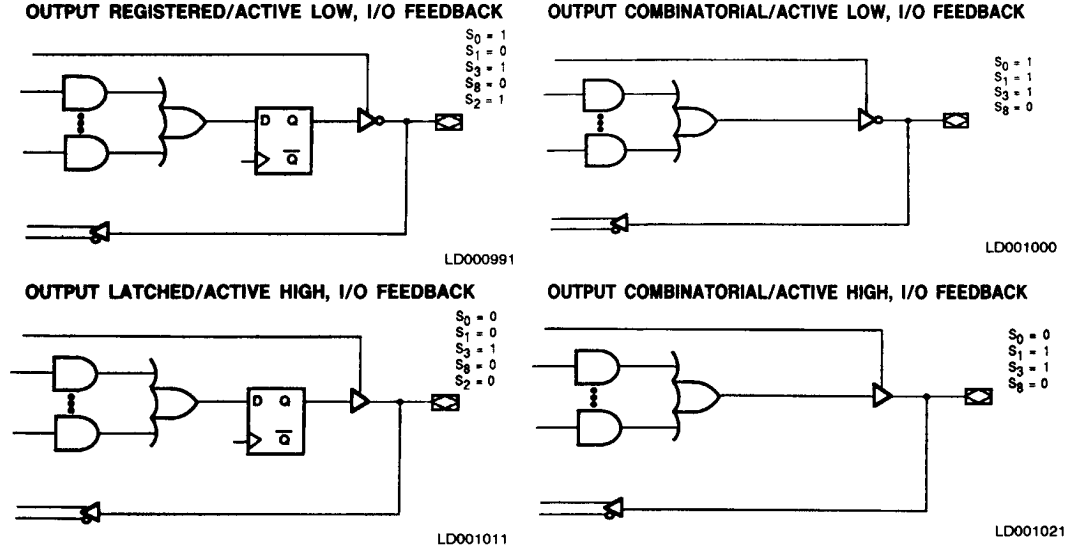

Figure 2b. Single Feedback Macrocells

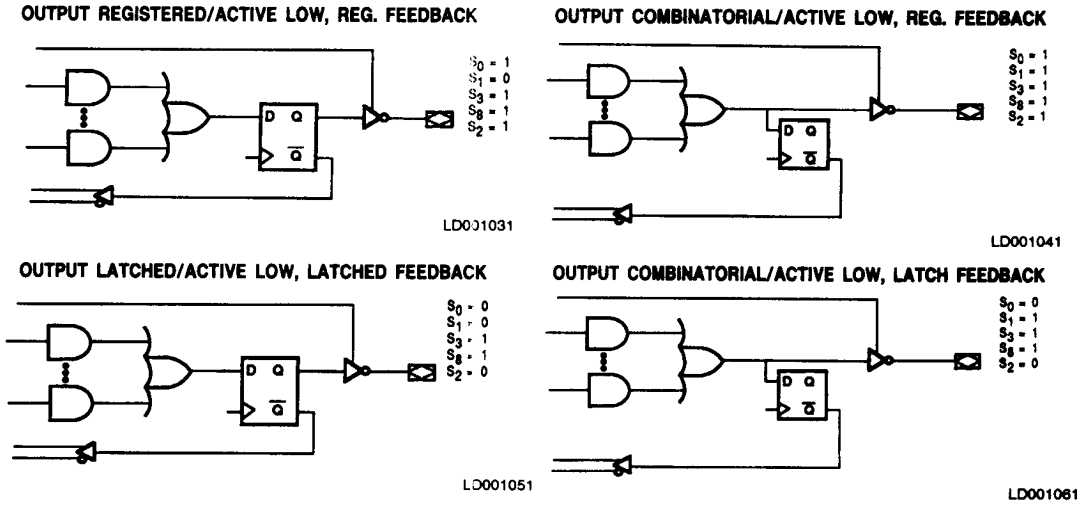

Figure 2b. Single Feedback Macrocells (Cont'd.)

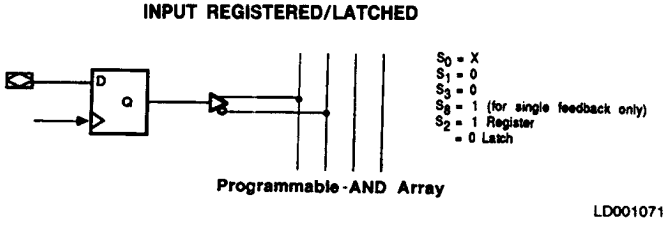

Figure 2c. All Macrocells

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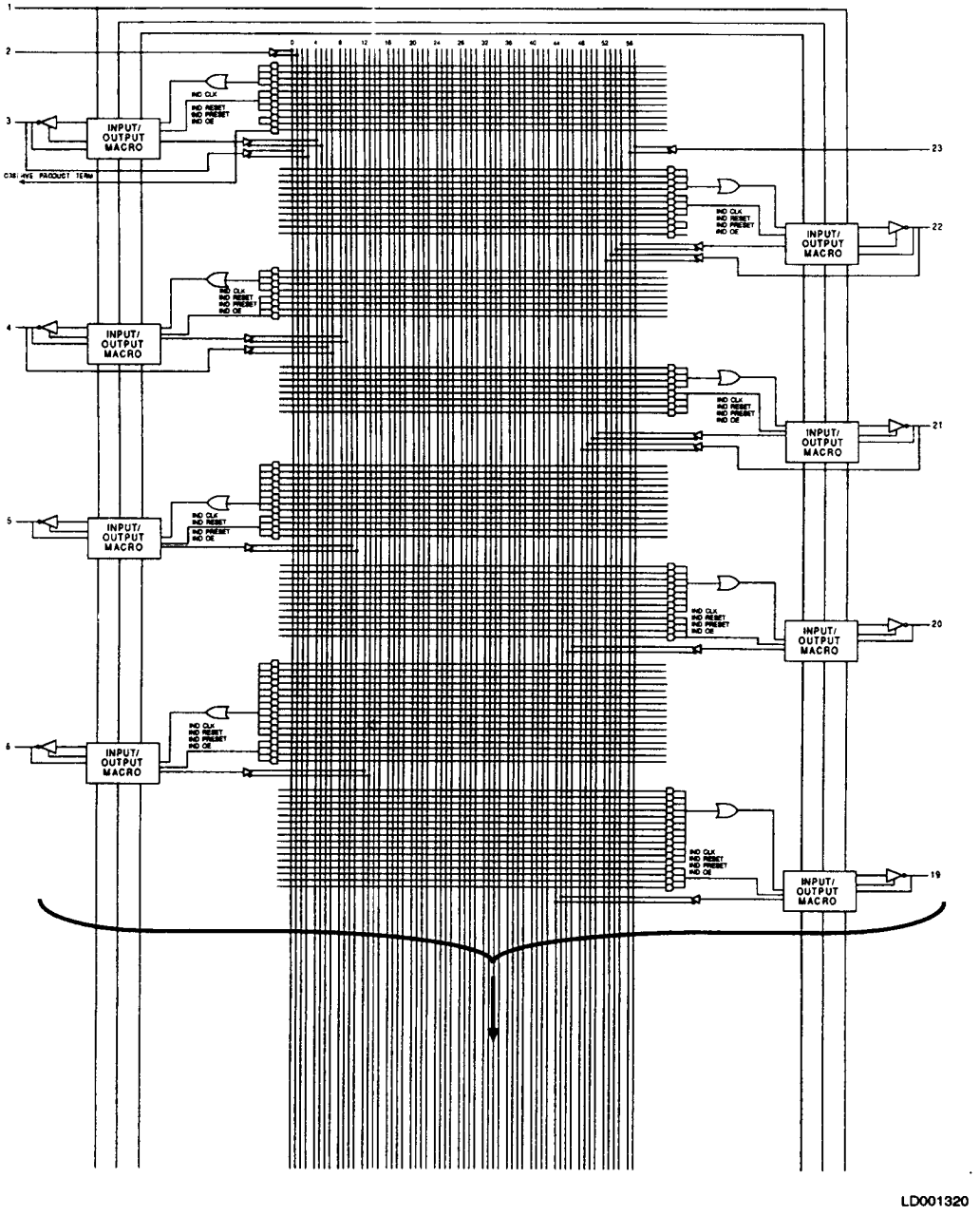

Figure 3. AmPALC29MA16 Logic Diagram

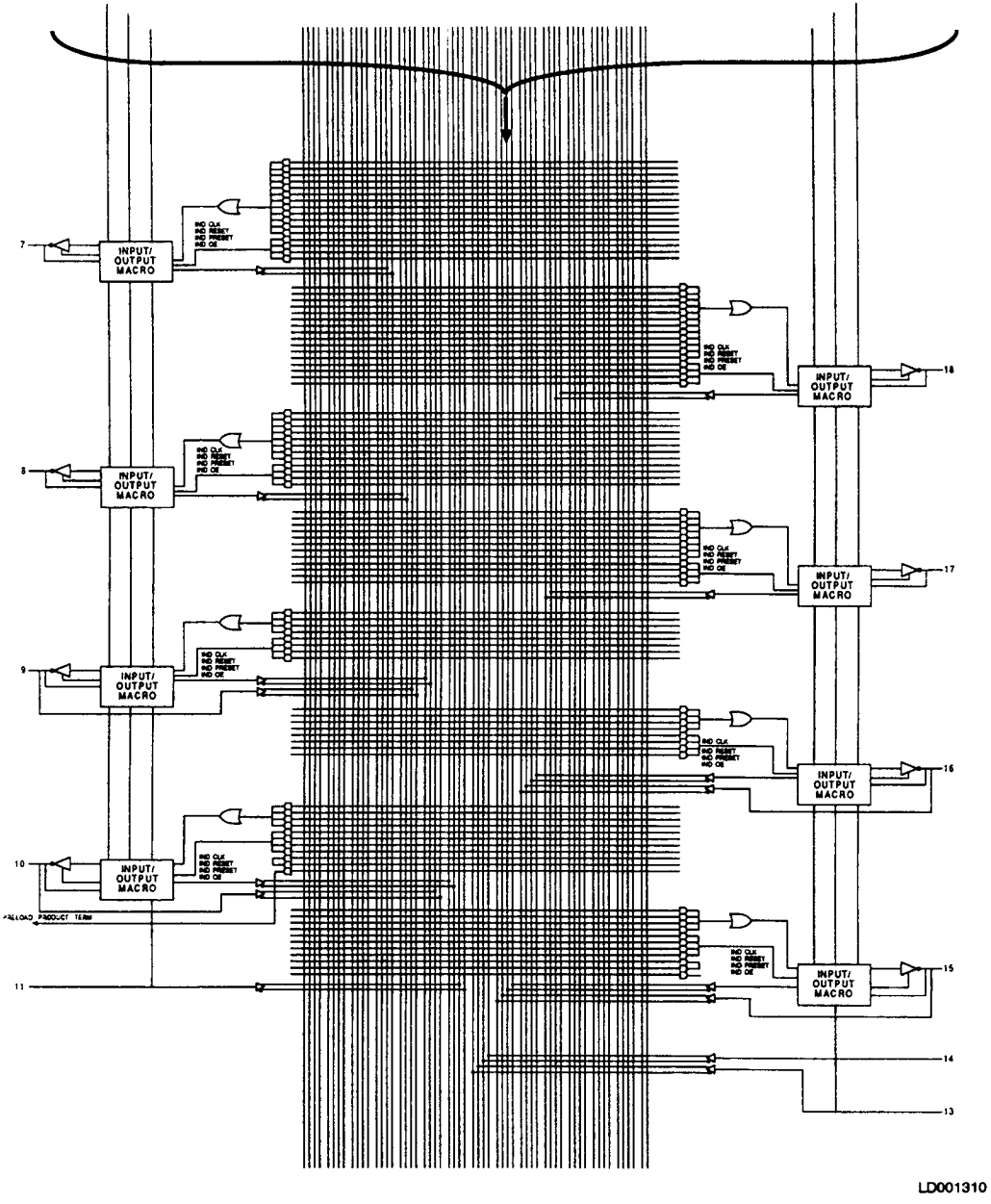

Figure 3. AmPALC29MA16 Logic Diagram (Cont'd.)

Designed in Testability and Debugging

PRELOAD

To simplify testing, the AmPALC29MA16 is designed with PRELOAD circuitry that provides an easy method for testing logical functionality. Both product-term controlled and supervoltage-enabled PRELOAD modes are available. This offers even more test capability than previously implemented in AMD's PAL devices. The TTL-level PRELOAD product term can be useful during debugging, where supervoltages may not be available.

PRELOAD allows any arbitrary state value to be loaded into the registers/latches of the device. A typical functional-test sequence would be to verify all possible state transitions for the device being tested. This requires the ability to set the state registers into an arbitrary "present state" value and to set the devices inputs into any arbitrary "present input" value. Once this is done, the state machine is clocked into a new state, or "next state", which can be checked to validate the transition from the "present state". In this way any transition can be checked.

Since PRELOAD can provide the capability to go directly to any desired arbitrary state, test sequences may be greatly shortened. Also, all possible states can be tested, thus greatly reducing test time and development costs and guaranteeing proper in-system operation.

Observability

The output register/latch observability product term, when asserted, suppresses the combinatorial output data from appearing on the I/O pin and allows the observation of the contents of the register/latch on the output pin for each of the logic macrocells. This unique feature allows for easy debugging and tracing of the buried state machines. In addition, a capability of supervoltage observability is also provided.

Power-Up Reset

All the device registers/latches have been designed to reset during device power-up. Following the power-up, all registers/latches will be cleared (Q = 0), setting the outputs to a state determined by the output select multiplexer. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization.

Security Cell

A security cell is provided on each device to prevent unauthorized copying of the user's proprietary logic design. Once programmed, the security cell disables the programming, verification, PRELOAD, and the observability modes. The only way to erase the protection cell is by charging the entire array and architecture cells, in which case no proprietary design can be copied. (This cell should be programmed only after the rest of the device has been completely programmed and verified.)

Programmers/Development Systems

(refer to Programmer Reference Guide, page 3-81)

Absolute Maximum Ratings

Storage Temperature ..... −65 to +150°C
Ambient Temperature under bias ..... −55 to +125°C
Supply Voltage with
Respect to Ground ..... −0.5 V to +7.0 V
DC Output Voltage ..... −0.5 V to V_{CC} + 0.5 V
DC Input Voltage
(Except Pin I/$\overline{OE}$) ..... −0.5 V to V_{CC} + 0.5 V
DC Input Voltage (Pin I/$\overline{OE}$) ..... −0.6 V to +7 V
DC Input Current ..... −1 mA to +1 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Operating Ranges

Commercial (C) Devices
Temperature (T_A) ..... 0°C to +70°C
Supply Voltage (V_{CC}) ..... +4.50 to +5.50 V

Military (M) Devices*

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Consult Factory for Military Specifications

DC Characteristics over operating range unless otherwise specified

HCT Devices**

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL} I_{OH} = −2 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 6 mA		0.5	V
			I_{OL} = 4 mA		0.33	
			I_{OL} = 20 μA		0.1	
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for all Inputs		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for all Inputs			0.8	V
I_I	Input Leakage Current	V_{IN} = 0 to 5.5 V, V_{CC} = Max.			10	μA
I_O	Output Leakage Current	V_{IN} = 0 to 5.5 V, V_{CC} = Max.			10	μA
I_{CCOP}	Operating Current Supply	f = f_{MAX}, Outputs Open (I_O = 0)			120	mA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_O = 0 V		−30	−90	mA

Capacitance

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Units
C_{IN}	Input Capacitance	V_{CC} = 5.00 V., T_A = 25°C V_{IN} = 0 V @ f = 1 MHz	5	pF
C_{OUT}	Output Capacitance		8	

Note: These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

** Consult Factory for DC specifications for HC Devices.

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Switching Characteristics

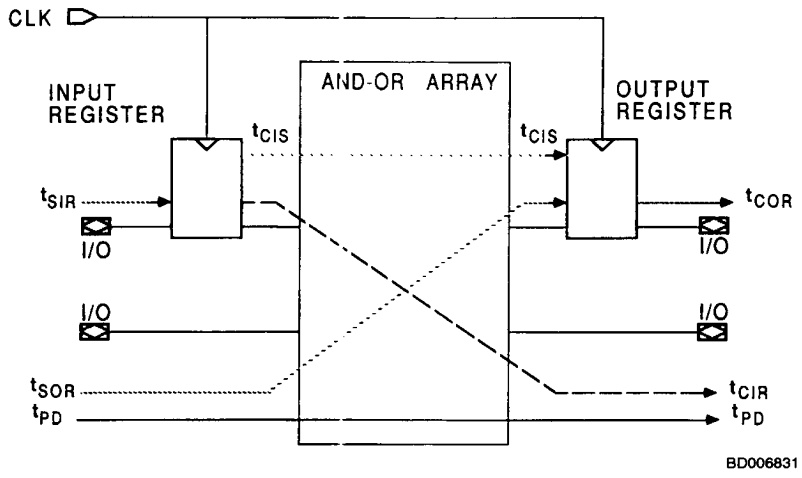
over operating range unless otherwise specified; all values are determined under the loading of one TTL gate and a capacitance of 50 pF

Parameter Number	Parameter Symbol	Parameter Description	-35		-45		Units
			Min.	Max.	Min.	Max.	
REGISTERED OPERATION (Numbers 1 through 20)							
1	t_{PD}	Input or I/O Pin to Combinatorial Output		35		45	ns
Output Register – Pin Clock							
2	t_{SOR}	Input or I/O Pin to Output Register Setup	27		34		ns
3	t_{COR}	Output Register Clock to Output		23		32	ns
4	t_{HOR}	Data Hold Time for Output Register	0		0		ns
Output Register – Product Term Clock							
5	t_{SORP}	I/O Pin or Input to Output Register Setup	20		24		ns
6	t_{CORP}	Output Register Clock to Output		45		56	ns
7	t_{HORP}	Data Hold Time for Output Register	15		20		ns
Input Register – Pin Clock							
8	t_{SIR}	I/O Pin to Input Register Setup	6		8		ns
9	t_{CIR}	Register Feedback Clock to Combinatorial Output		45		58	ns
10	t_{HIR}	Data Hold Time for Input Register	3		4		ns
Clock and Frequency							
11	t_{CIS}	Register Feedback (Pin Driven Clock) to Output Register/Latch (Pin Driven) Setup	35		45		ns
12	t_{CISPP}	Register Feedback (PT Driven Clock) to Output Register/Latch (PT Driven) Setup	45		60		ns
13	f_{MAX}	Maximum Frequency (Pin Driven) $1/(t_{SOR} + t_{COR})$		20		15	MHz
14	f_{MAXI}	Maximum Internal Frequency (Pin Driven) $1/t_{CIS}$		28.5		22.5	MHz
15	f_{MAXP}	Maximum Frequency (PT Driven) $1/(t_{SORP} + t_{CORP})$		15.5		12.5	MHz
16	f_{MAXIPP}	Maximum Internal Frequency (PT Driven) $1/t_{CISPP}$		22.5		16.5	MHz
17	t_{CWH}	Pin Clock Width HIGH	12		15		ns
18	t_{CWL}	Pin Clock Width LOW	12		15		ns
19	t_{CWHP}	PT Clock Width HIGH	15		20		ns
20	t_{CWLP}	PT Clock Width LOW	15		20		ns

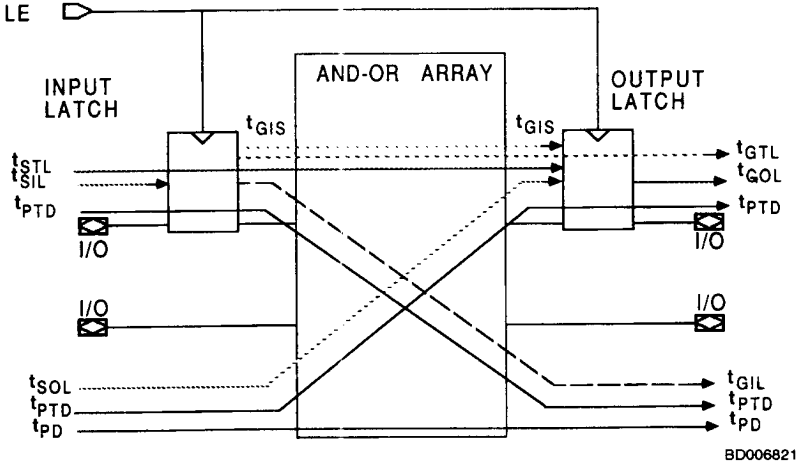
Parameter Number	Parameter Symbol	Parameter Description	-35		-45		Units
			Min.	Max.	Min.	Max.	
LATCHED OPERATION (Numbers 21 through 39)							
21	t_{PD}	Input or I/O Pin to Combinatorial Output		35		45	ns
22	t_{PTD}	Input or I/O Pin to Output via Transparent Latch		45		55	ns
Output Latch – Pin LE							
23	t_{SOL}	Input or I/O Pin to Output Latch Setup	27		34		ns
24	t_{GOL}	Latch Enable to Transparent Mode Output		23		32	ns
25	t_{HOL}	Data Hold Time for Output Latch	0		0		ns
26	t_{STL}	Input or I/O Pin to Output Latch Setup via Transparent Input Latch	35		45		ns
Output Latch – PT LE							
27	t_{SOLP}	Input or I/O Pin to Output Latch Setup	20		24		ns
28	t_{GOLP}	Latch Enable to Transparent Mode Output		45		56	ns
29	t_{HOLP}	Data Hold Time for Output Latch	15		20		ns
30	t_{STLP}	Input or I/O Pin to Output Latch Setup via Transparent Input Latch	30		35		ns
Input Latch – Pin LE							
31	t_{SIL}	I/O Pin to Input Latch Setup	6		8		ns
32	t_{GIL}	Latch Feedback, Latch Enable Transparent Mode to Combinatorial Output		45		58	ns
33	t_{HIL}	Data Hold Time for Input Latch	3		4		ns
Latch Enable							
34	t_{GIS}	Latch Feedback (Pin Driven) to Output Register/Latch (Pin Driven) Setup	35		45		ns
35	t_{GISPP}	Latch Feedback (PT Driven) to Output Register/Latch (PT Driven) Setup	45		60		ns
36	t_{GWH}	Pin Enable Width HIGH	12		15		ns
37	t_{GWL}	Pin Enable Width LOW	12		15		ns
38	t_{GWHP}	PT Enable Width HIGH	15		20		ns
39	t_{GWLP}	PT Enable Width LOW	15		20		ns

Parameter Number	Parameter Symbol	Parameter Description	-35		-45		Units
			Min.	Max.	Min.	Max.	
RESET/PRESET & OUTPUT ENABLE (Numbers 40 through 49)							
40	t_{APO}	Input or I/O Pin to Output Register/Latch RESET/ PRESET		40		55	ns
41	t_{AW}	Async. RESET/PRESET Pulse Width	35		45		ns
42	t_{ARO}	Async. RESET/PRESET to Output Register/Latch Recovery	30		40		ns
43	t_{ARI}	Async. RESET/PRESET to Input Register/Latch Recovery	20		30		
44	t_{ARPO}	Async. RESET/PRESET to Output Register/Latch Recovery PT Clock/LE	20		25		ns
45	t_{ARPI}	Async. RESET/PRESET to Input Register/Latch Recovery PT Clock/LE	15		20		ns
46	t_{PZX}	I/$\overline{OE}$ Pin to Output Enable		30		40	ns
47	t_{PXZ} *	I/$\overline{OE}$ Pin to Output Disable		30		40	ns
48	t_{EA}	Input or I/O to Output Enable via PT		35		45	ns
49	t_{ER} *	Input or I/O to Output Disable via PT		35		45	ns

* Output disable times do not include test load RC time constants.

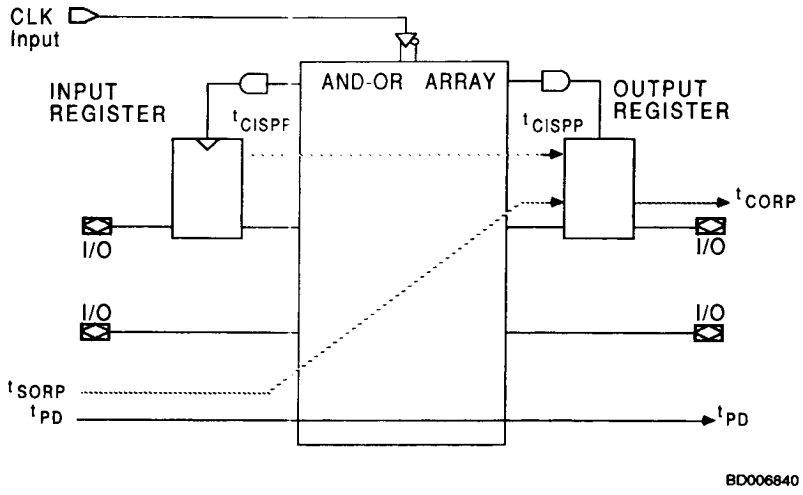


Input/Output Register Specs (Pin CLK Reference)

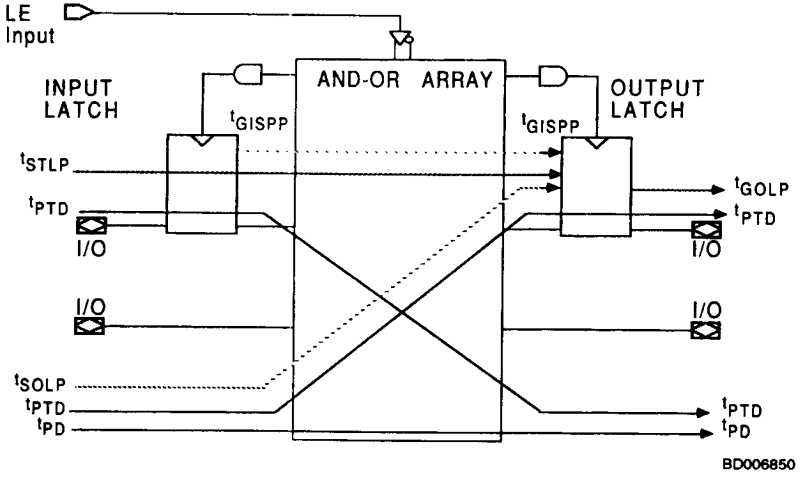


Input/Output Latch Specs (Pin LE Reference)

5

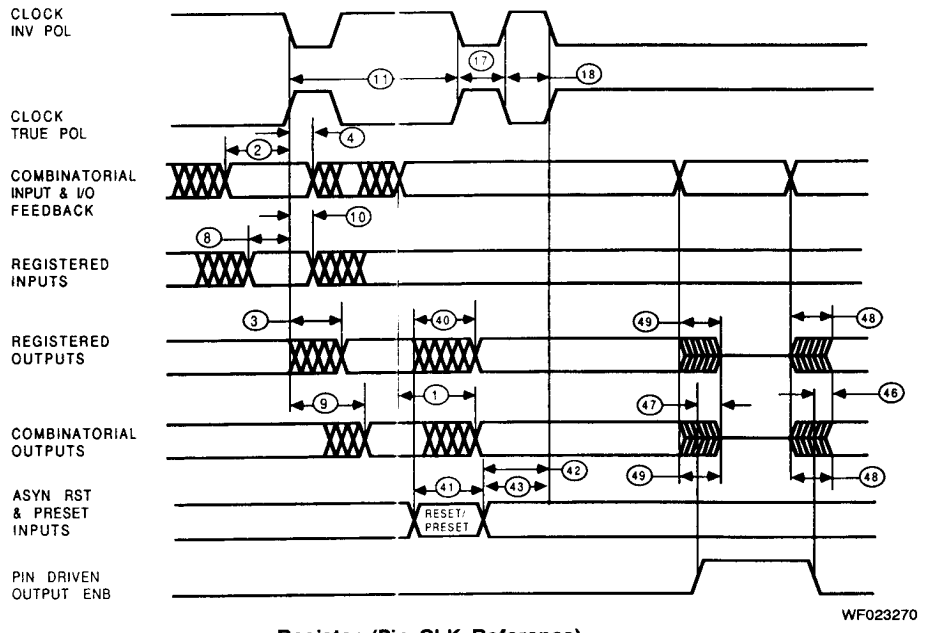


Input/Output Register Specs (PT CLK Reference)

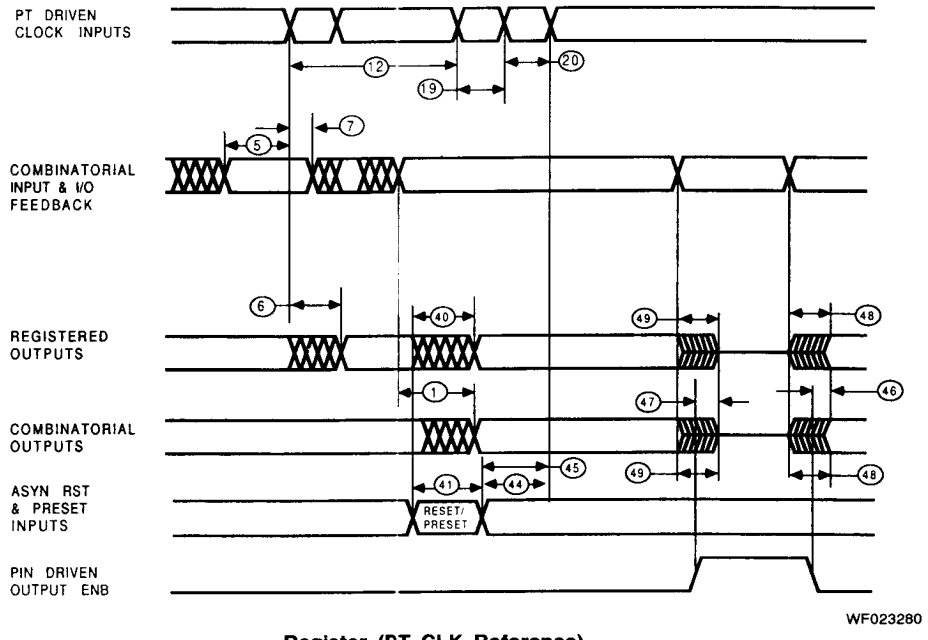


Input/Output Latch Specs (PT LE Reference)

Switching Waveforms

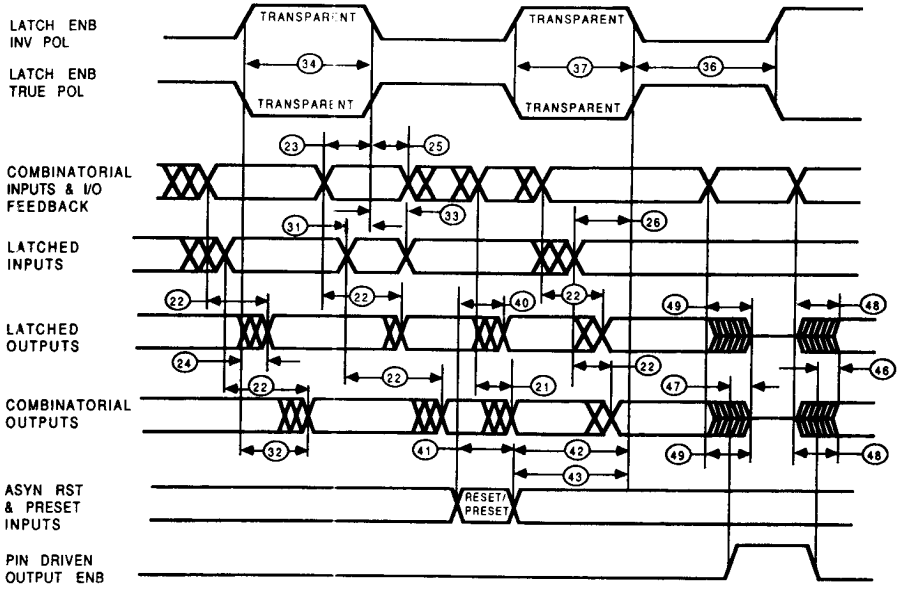


Register (Pin CLK Reference)



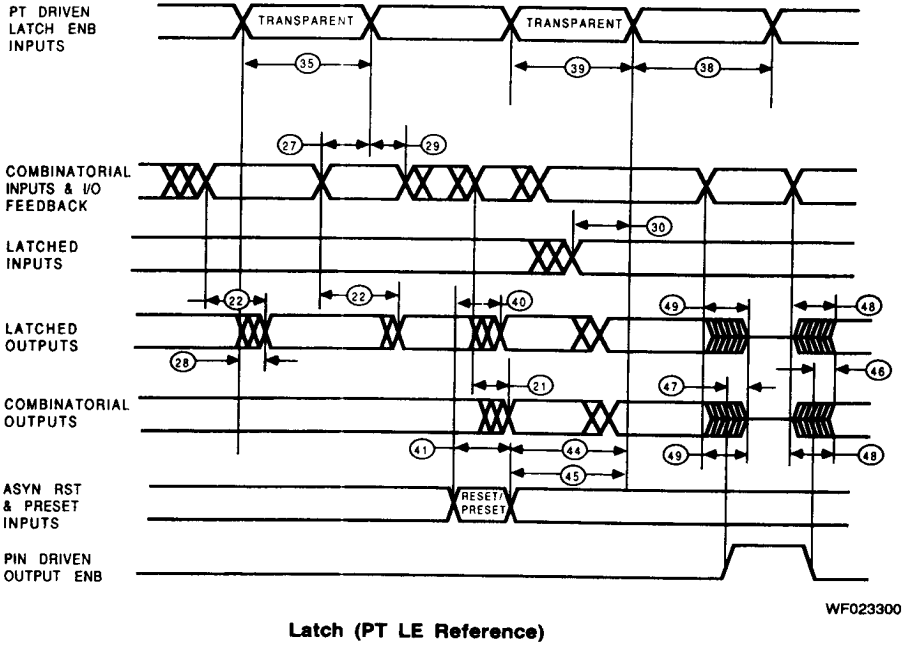
Register (PT CLK Reference)

Switching Waveforms (Cont'd.)



WF023290

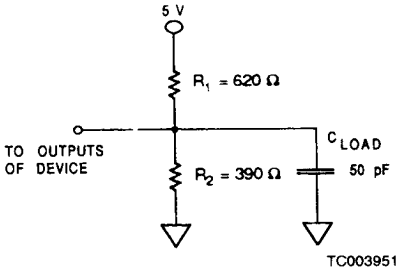
Latch (Pin LE Reference)



WF023300

Latch (PT LE Reference)

Switching Test Circuit



Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
——— / ———	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010

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