

AKN62321E Series

AKN62331E Series

131072-Word × 8-Bit CMOS Mask Programmable ROM

AKN62321E, AKN62331E Series is a 1-Mbit CMOS mask-programmable ROM organized as 131072-word x 8-bit. It can be operated with a battery because of low power consumption. The large capacity of 1M bits is optimum for a kanji character generator.

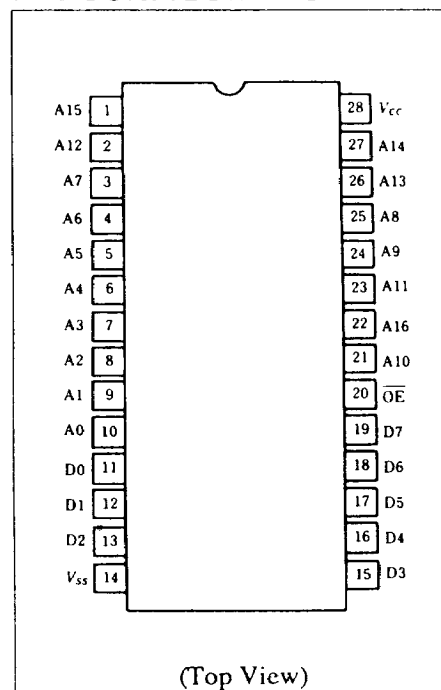
Features

- Single 5 V
- Wired OR is permitted for the output in three states
- TTL compatible
- Address access time: 120/200 ns (max)
- OE access time: 60/100ns (max)
- Low power: 100 mW (typ)
- Byte-Wide Data Organization

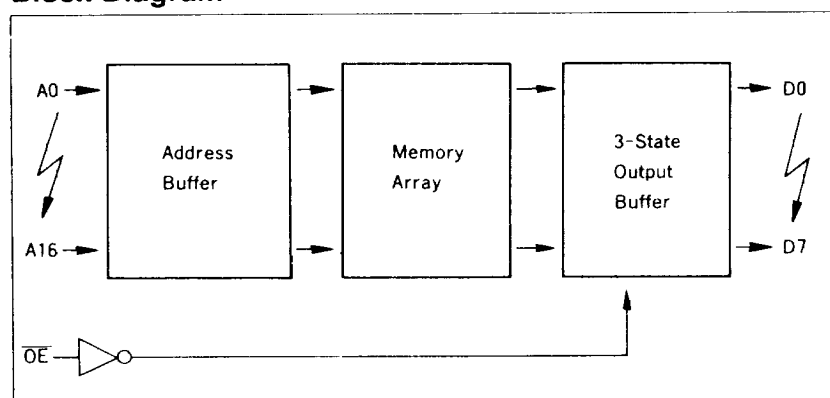
Ordering Information

Type No.	Address Access Time	Package
AKN62321EP	200 ns	600 mil 28-pin plastic DIP
AKN62331EP	120 ns	
AKN62321EF	200 ns	28-pin plastic SOP
AKN62331EF	120 ns	

PIN CONFIGURATION



Block Diagram



Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage*1	V _{CC}	-0.3 to +7.0	V
Terminal voltage*1	V _T	-0.3 to V _{CC} + 0.3	V
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	-55 to +125	°C
Bias temperature	T _{bias}	-20 to +85	°C

Note: *1. With respect to V_{SS}.

Recommended Operating Conditions (V_{SS} = 0 V, T_a = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage	V _{CC}	4.5	5.0	5.5	V
Input voltage	V _{HI}	2.2	—	V _{CC} + 0.3	V
	V _{LI}	-0.3	—	0.8	V

DC Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, T_a = 0 to +70°C)

Item	Symbol	Min	Max	Unit	Test Conditions
Power supply current	I _{CC}	—	50	mA	V _{CC} = 5.5 V, I _{OUT} = 0 mA, t _{RC} = Min
Input leak current	I _{LI}	—	10	μA	V _{IN} = 0 to V _{CC}
Output leak current	I _{LO}	—	10	μA	$\overline{\text{OE}}$ = 2.2 V, V _{OUT} = 0 to V _{CC}
Output voltage	V _{OH}	2.4	—	V	I _{OH} = -205 μA
	V _{OL}	—	0.4	V	I _{OL} = 3.2 mA

Capacitance (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, T_a = 25°C, V_{in} = 0 V, f = 1 MHz)

Item	Symbol	Min	Max	Unit
Input capacitance*1	C _{in}	—	10	pF
Output capacitance*1	C _{out}	—	15	pF

Note: *1. This parameter is sampled and not 100% tested.

AC Operating Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, T_a = 0 to +70°C)

Test Conditions

Input pulse level: 0.8 to 2.4 V

Output load:

1 TTL gate + C_L = 100 pF
(including jig capacitance)

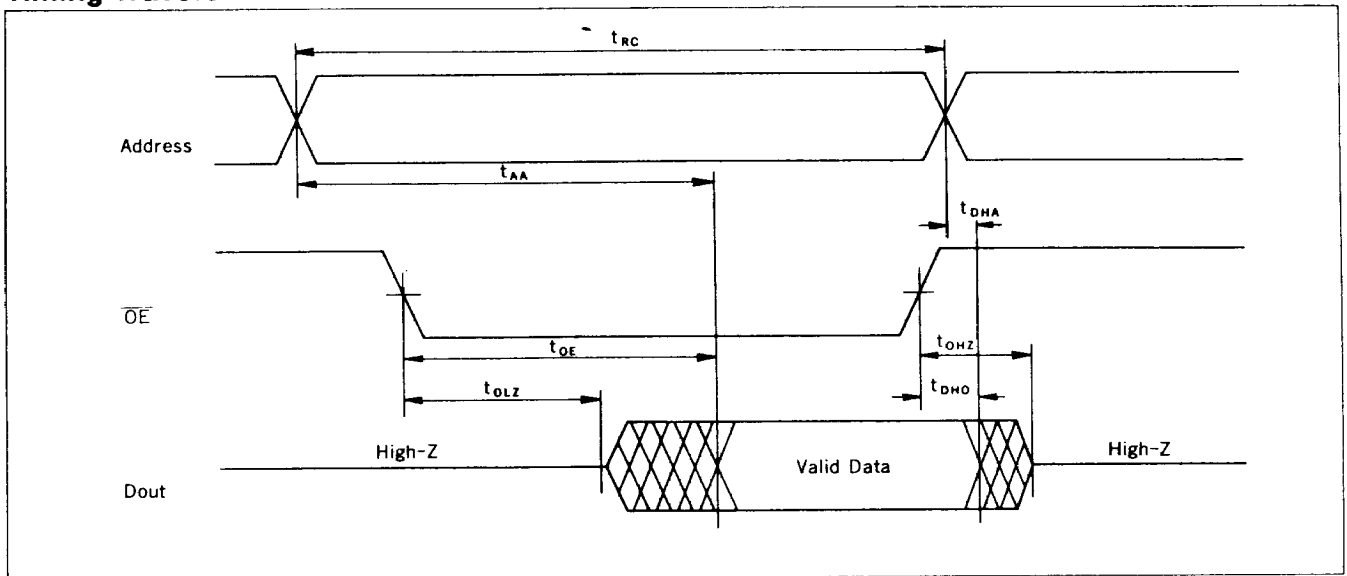
I/O timing reference level: 1.5 V

Input rise/fall time: 10 ns

Item	Symbol	AKN62331E		AKN62321E		Unit
		Min	Max	Min	Max	
Cycle time	t _{RC}	120	—	200	—	ns
Address access time	t _{AA}	—	120	—	200	ns
$\overline{\text{OE}}$ access time	t _{OE}	—	60	—	100	ns
Output Hold Time from Address Change	t _{DHA}	0	—	0	—	ns
Output Hold Time from $\overline{\text{OE}}$	t _{DHO}	0	—	0	—	ns
$\overline{\text{OE}}$ to Output in High Z	t _{OHZ} *1	—	60	—	100	ns
$\overline{\text{OE}}$ to Output in Low Z	t _{OLZ}	5	—	10	—	ns

Note: *1 t_{OHZ} define the time at which the output goes to the high impedance state and is not referenced to output voltage levels.

Timing Waveform



- Notes:
1. t_{DHA} , t_{DHO} ; Determined by whichever is faster.
 2. t_{AA} , t_{OE} ; Determined by whichever is slower.