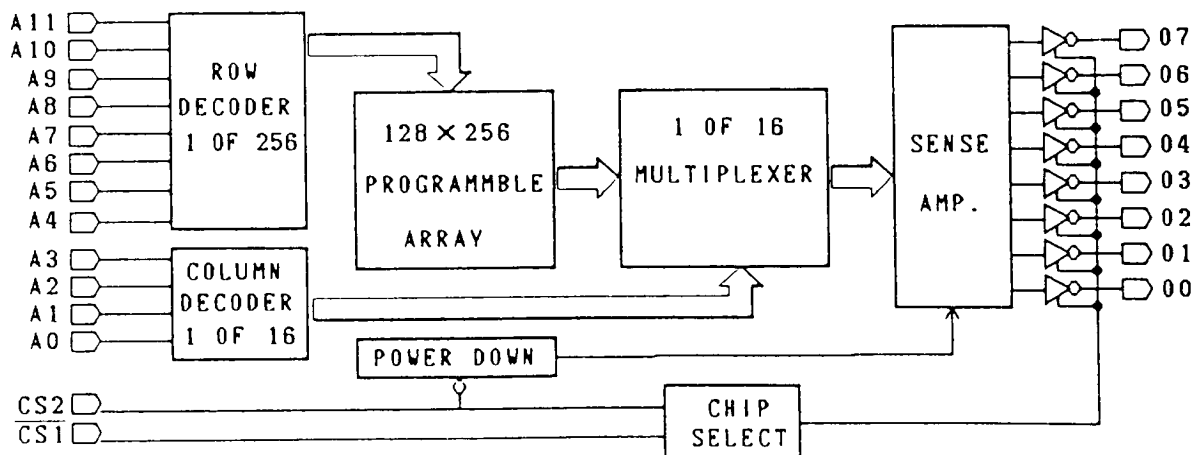


AK27CX321 / 322

32Kbit CMOS High-Speed UV-Erasable PROM

Features

- ☐ 4096word $\times$ 8bit
- ☐ Advanced CMOS EPROM Technology
- ☐ High Performance
 - AK27CX321/322-35 $\cdot \cdot$ $t_{AA} = 35\text{ns max.}$
 - AK27CX321/322-40 $\cdot \cdot$ $t_{AA} = 40\text{ns max.}$
 - AK27CX321/322-45 $\cdot \cdot$ $t_{AA} = 45\text{ns max.}$
- ☐ Low Power Consumption
 - $I_{CC} = 40\text{mA max.}$ - Active
 - $I_{SB} = 500\mu\text{A typ.}$ - Standby Mode
- ☐ TTL-Compatible I/O
- ☐ Reprogrammability
 - Adds convenience, reduces costs
 - Windowed package for UV erasure
 - Allows 100% factory testing
- ☐ Bipolar PROM replacement
 - Pin-compatible with Bipolar PROMs
 - Higher speed
 - Lower power consumption
 - 300-mil(AK27CX322) and 600-mil(AK27CX321) packages

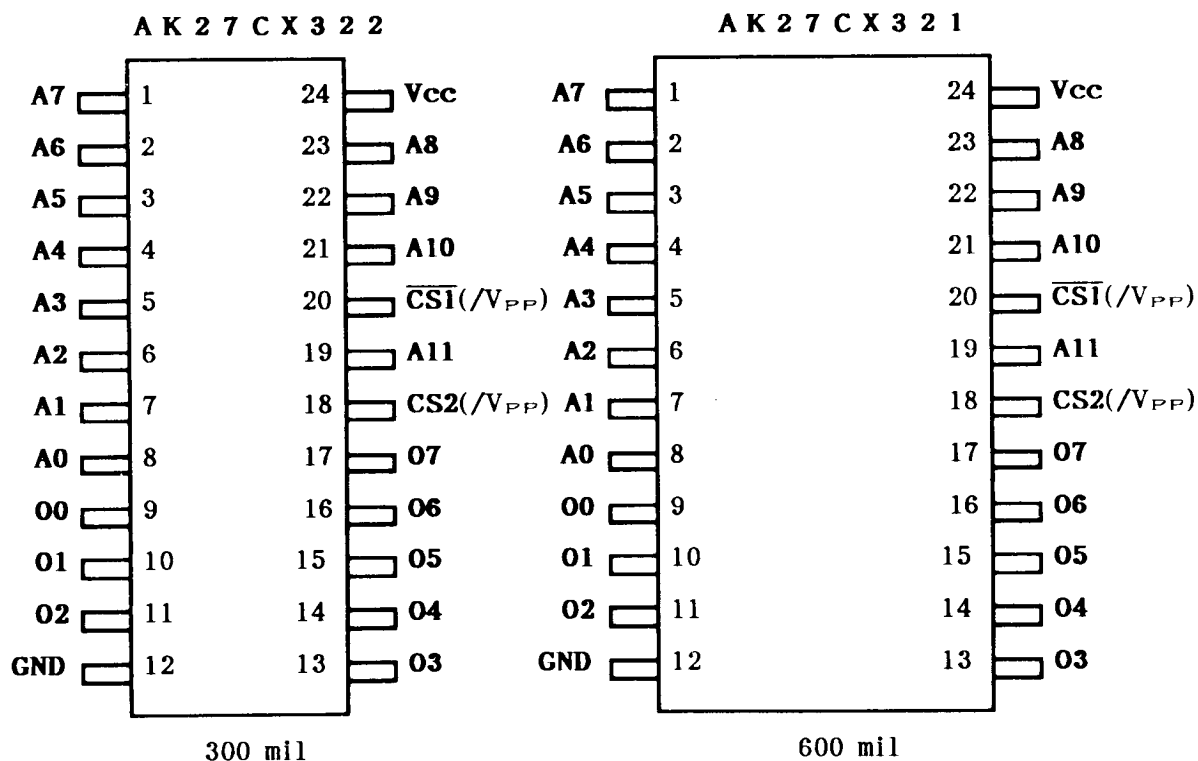


Block Diagrams

General Description

The AKM AK27CX321 and AK27CX322 are $4096 \times 8\text{bit}$, CMOS, high-speed, UV-erasable PROMs that provide a low-power, reprogrammable alternative to bipolar fuse-link PROMs. Available in both 600mil(AK27CX321) and 300mil(AK27CX322) packages, these devices are pin/socket-compatible with many popular bipolar PROMs. The AK27CX321/322 is designed in an advanced CMOS EPROM technology and utilize differential memory cell techniques to provide access times comparable to high-speed bipolar PROMs (as fast as 35ns), with a significant improvement in power consumption. A special, user-programmable, low-power standby mode reduces power consumption even further when the device is deselected. The reprogrammability of the AK27CX321/322 not only adds convenience and reduces development and field retrofit costs, but enhances factory testability, allowing for 100% field programmability and function.

■ Pin Diagrams



A0-A11 = Address Input

O0-O7 = Data Output

CS1 = Chip Select 1 (/V_{PP} Programming Voltage)

CS2 = Chip Select 2 (/V_{PP} Power-down set Voltage)

GND = Ground

Vcc = Power Supply(+5V)

Standby Low-Power Mode

The low-power standby mode is a user-selectable option that can be set using programming equipment that supports the AK27CX321/322. If this mode is set, the AK27CX321/322 will power-down to typically 500 μ A supply current while CS2 is asserted low. The delay from CS2 low to power-down is approximately 45ns. Note that chip-select-to-data-out timing for CS2 will change if the standby mode is selected (refer to the specification for t_{CS2} under A.C. Electrical Characteristics). For information on selecting the standby option, please contact your programmer manufacturer or AKM.

Erase Characteristics

The AK27CX321/322 is erased by exposure to ultraviolet light. For complete erasure, the recommended minimum integrated dose (UV intensity $\times$ exposure time) is 15 Watt-second/cm² of ultraviolet light with a wavelength of 2537 . For an ultraviolet lamp with a 12mW/cm² power rating, the exposure time would be approximately 20 minutes. The AK27CX321/322 should be placed within one inch of the lamp during erasure. Exposing the CMOS EPROM to high-intensity UV-light for extended periods may affect device reliability.

Programming the AK27CX321/322

The AK27CX321/322 employs a dual-transistor differential memory cell design. Initially, and after erasure, all bits of the AK27CX321/322 are in an undefined state. Thus, verifying a blank device will yield erroneous results. The desired state of each bit must be programmed into the device to ensure proper operation.

Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage

Symbol	Parameter	Conditions	Rating	Unit
V _{CC}	Supply Voltage	Relative to GND	-0.6 ~ +7.0	V
V _{IO}	Voltage Applied to Any Pin	Relative to GND	-0.6 ~ V _{CC} +0.6	V
T _A	Ambient Temp., Power Applied		-10 ~ +85	°C
T _{ST}	Storage Temperature		-65 ~ +125	°C
T _{LT}	Lead Temperature	Soldering 10 seconds	+260	°C

Read Operation

Operation Ranges

Symbol	Parameter	Conditions	min.	max.	Unit
V_{CC}	Supply Voltage		4.75	5.25	V
T_A	Ambient Temperature		0	70	°C

D.C. Electrical Characteristics

Over the operating range

Symbol	Parameter	Conditions	min.	max.	Unit
V_{IH}	Input HIGH Level		2.0		V
V_{IL}	Input LOW Level			0.8	V
V_{OH}	Output HIGH Voltage* ¹	$V_{CC}=\text{min.}, I_{OH}=-4.0\text{mA}$	2.4		V
V_{OL}	Output LOW Voltage	$V_{CC}=\text{min.}, I_{OL}=12\text{mA}$		0.45	V
I_L	Input Leakage Current	$V_{CC}=\text{max.}, \text{GND} \leq V_I \leq V_{CC}$		10	μA
I_{OS}	Output Short Circuit Current* ²	$V_{CC}=\text{max.}, V_O=\text{GND}$ $\overline{CS1}=V_{IL} \text{ and } CS2=V_{IH}$	-15	-90	mA
I_{OZ}	Output Leakage Current	$V_{CC}=\text{max.}, V_O=V_{CC} \text{ or } \text{GND}$ $\overline{CS1}=V_{IH} \text{ or } CS2=V_{IL}$		10	μA
I_{CC}	Power Supply Current	All Inputs=(GND or $V_{CC}) \pm 0.3\text{V}$		40	mA
I_{SB}	Standby Current* ³	$CS2=V_{IL}, \text{Other Inputs}=(\text{GND or } V_{CC}) \pm 0.3\text{V}$	0.1	5	mA
V_{IC}	Input Clamp Voltage	$V_{CC}=\text{min.}, I_{IN}=-10\text{mA}$		-1.2	V

Notes :

1. The AK27CX321/322 provide true CMOS output interface levels. The specifications shown are for TTL interface.
2. No more than one output should be shorted at a time. Duration of short circuit should not be more than one second.
3. Applicable only if standby mode is programmed.

Capacitance

These measurements are periodically sample tested

Symbol	Parameter	Conditions	min.	max.	Unit
C_{IN}	Input Capacitance	$T_A=25^{\circ}C$ $V_{CC}=5.0V$ @ $f=1MHz$		6	pF
C_{OUT}	Output Capacitance			12	pF
C_{CS1}	$\overline{CS1}$ Pin Capacitance			15	pF
C_{CS2}	CS2 Pin Capacitance			6	pF

A.C. Electrical Characteristics

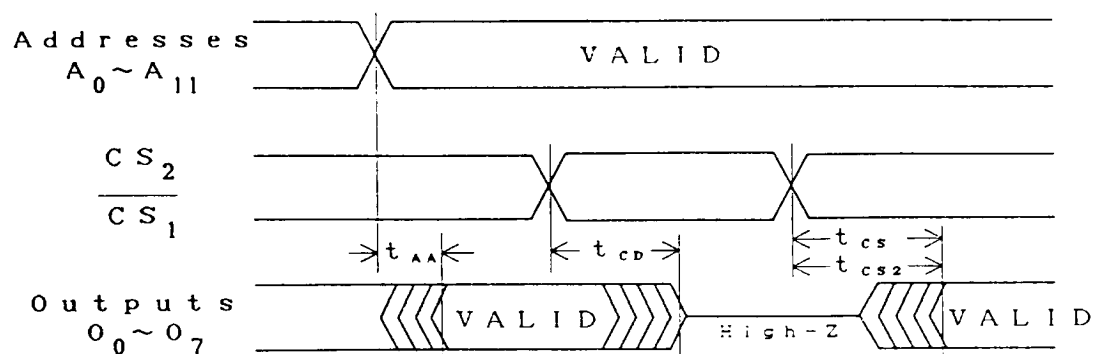
 Over the Operating Range⁴

Symbol	Parameter	27CX321-35 27CX322-35		27CX321-40 27CX322-40		27CX321-45 27CX322-45		Unit
		min.	max.	min.	max.	min.	max.	
t_{AA}	Access Time From Address To Output		35		40		45	ns
t_{CS}	Access Time From Chip Select 1 or 2 to Output ^{*5}		20		25		25	ns
t_{CS2}	Chip Select 2 to Output In Standby Mode ^{*3, *5}		30		30		35	ns
t_{GD}	Chip Select 1 and 2 Disable to High-Z ^{*5, *6}		20		20		25	ns

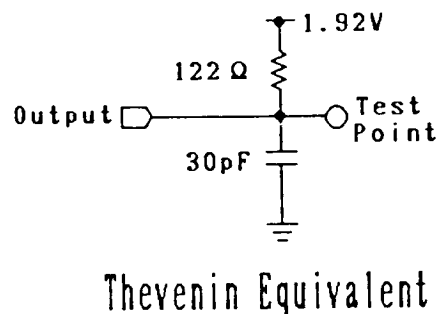
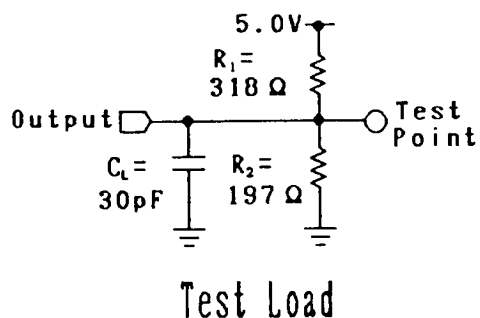
Note :

4. Test conditions assume: signal transition times of 5ns or less from the 10% and 90% points; timing reference levels of 1.5V(unless otherwise specified); and test loads shown.

Switching Waveforms



Test Loads



Note :

5. t_{CS} , t_{CS2} , and t_{CD} are measured at the midpoint between output ($O_0 \sim O_7$) steady-state high-Z level and V_{OH} or V_{OL} .
6. C_L includes scope and jig capacitance. t_{CD} is tested with $C_L = 5 \text{ pF}$.

Program operation

Operation Ranges

Symbol	Parameter	Conditions	min.	max.	Unit
T_A	Ambient Temperature		20	30	°C

D.C. Electrical Characteristics

$T_a = 25^\circ\text{C}$

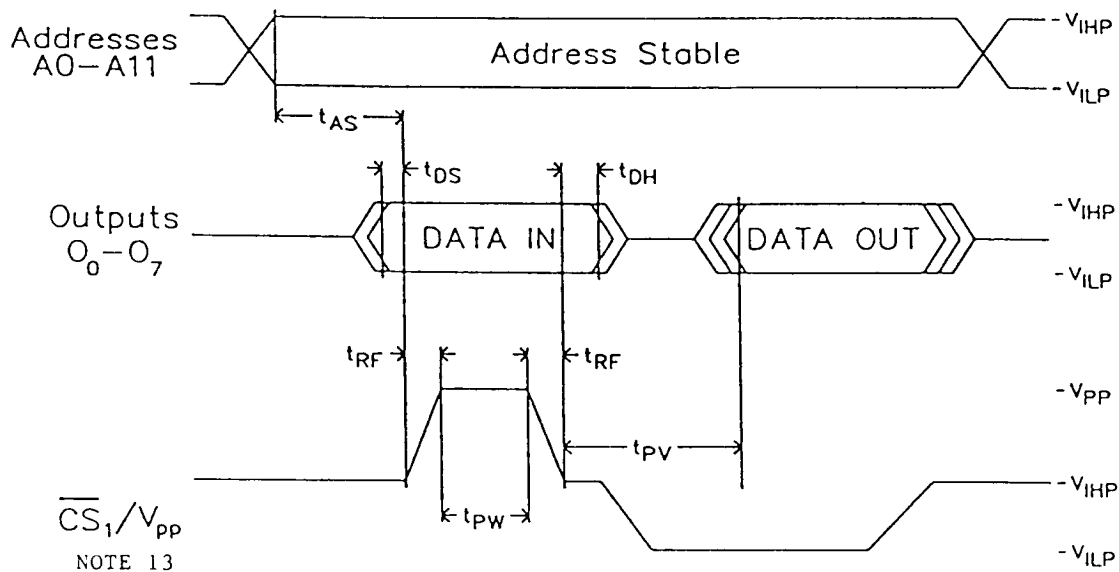
Symbol	Parameter	min.	typ.	max.	Unit
V_{ccp}	Vcc during programming	5.75	6	6.25	V
V_{IHP}	Input HIGH Level during programming	2.4		6.25	V
V_{ILP}	Input LOW Level during programming	0		0.45	V
V_{pp}	Programming Voltage	12.2	12.5	12.8	V
I_{pp}	V_{pp} Supply Current		20	50	mA

A.C. Electrical Characteristics

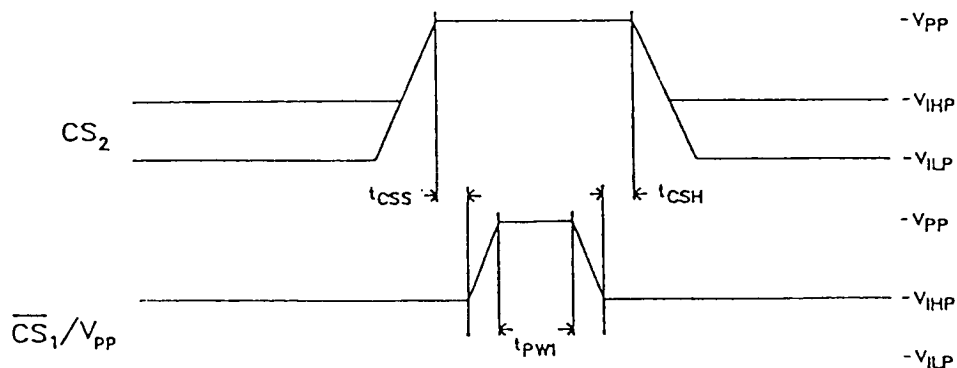
$T_a = 25^\circ\text{C}$

Symbol	Parameter	min.	typ.	max.	Unit
t_{AS}	Address set-up to V_{pp} pulse	0			ns
t_{DS}	Data set-up to V_{pp} pulse	0			ns
t_{PW}	V_{pp} program pulse width *7			50	μs
t_{PWI}	VPP pulse width for (set) power-down mode			100	ms
t_{RF}	V_{pp} rise and fall ramp time *8	1			ns/V
t_{DH}	Data hold time	10			ns
t_{PV}	V_{pp} pulse to verify delay *9		2	5	μs
t_{CSS}	Chip select 2 set-up to V_{PP}	10			ns
t_{CSH}	Chip select 2 hold after V_{PP}	10			ns

Switching Waveforms (PROGRAMMING) <Vccp=6V>



Switching Waveforms (SET POWER-DOWN) <Vccp=6V>



Note :

- *7: It is recommended to use $50\mu s$ for the V_{PP} Program pulse width in the interlative section to ensure maximum device performance.
- *8: In using the recommended rise and fall ramp times, any overshoot due to system and/or tester noise must not exceed the maximum V_{CCP} voltage.
- *9: This timing parameter is the device internal delay. After the $\overline{CS}_1/V_{PP}$ pin has been ramped down from the V_{PP} to the V_{ILP} voltage (to do a data read for data verification), the outputs will have a t_{PV} delay before they are valid .

Programming Flow

