ANALOG DEVICES

Low Cost 16-Bit Digital-to-Analog Converter

AD1145

FEATURES
16-Bit Resolution
Low Nonlinearity
  Differential: ±3/4LSB max
  Integral: ±1LSB max
Relative Accuracy: ±0.003% max
Fast Full-Scale Settling: 6μs to ±1/2LSB
High Stability
  Monotonic to 16 Bits: +15°C to +35°C
  Offset TC: ±0.1ppm/°C max
  Gain TC: ±0.1ppm/°C max
Double Buffered Digital Input
Parallel and Serial Data Input
Single +5V Supply Operation
Low Power Consumption: 2.5mW
Small Size: 44-Pad Plastic LLCC
Low Cost

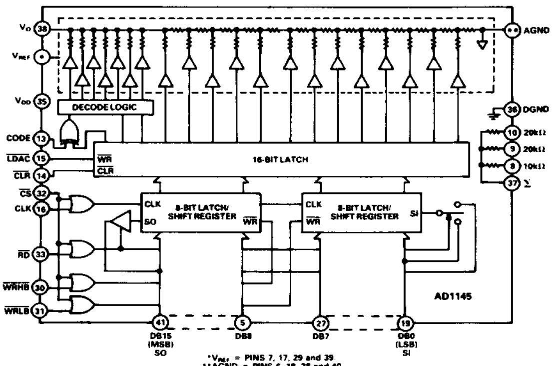
APPLICATIONS
Automatic Test Equipment
Scientific Instrumentation
Machine Control
Digital Audio
Robotics

GENERAL DESCRIPTION

The AD1145 is a double-buffered, 16-bit resolution DAC with ±3/4LSB maximum differential and ±1LSB maximum integral nonlinearity. Size comparable to the smallest monolithic DACs and high reliability are owed to its proprietary two-chip construction. A custom CMOS integrated circuit and laser-trimmed, thin-film resistor network provide 16-bit accuracy, excellent temperature stability and low power consumption.

The AD1145 offers an unparalleled combination of low cost, high accuracy, small size and convenient design-in features. The AD1145 directly interfaces with 8- and 16-bit microprocessors or can be used in stand-alone applications. Digital input coding is binary for unipolar output and offset binary or twos complement for bipolar output. Data can be written to the DAC in either a parallel or a serial mode. Serial data readback is available for error checking.

AD1145 FUNCTIONAL BLOCK DIAGRAM



*V_{REF} = PINS 7, 17, 29 and 39
**AGND = PINS 6, 18, 28 and 40

A clear line allows resetting the DAC output to zero volts on command. Power-up automatically resets the DAC output to zero volts following a power failure as required in machine control applications. All outputs may be simultaneously updated in a multiple DAC system.

Internal application resistors allow a wide variety of pin programmable output voltage ranges (+5V, +10V, −5V, −10V, ±5V and ±10V). The AD1145 may be operated off of a single +5V reference/supply, consuming only 2.5mW of power.

A 5 volt full-scale output step settles to within ±1/2LSB in just 6 microseconds. Wideband noise (100kHz) is only 50 microvolts peak-to-peak.

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SPECIFICATIONS (typical @ +25°C, rated supplies unless otherwise specified)

Model	AD1145A/AG	AD1145B/BG
RESOLUTION	16 Bits	*
ACCURACY		
Differential Nonlinearity, max	±1LSB (= ±0.0015%)	±3/4LSB (= ±0.001%)
Integral Nonlinearity, max[1]	±1LSB (= ±0.0015%)	*
Relative Accuracy, max	±0.003%	*
Initial Errors		
Offset Error	±1/4LSB	*
Gain Error		
w/o Int. Application Resistors	±1/4LSB	*
w/Int. Application Resistors	±0.1%	*
STABILITY VS. TEMPERATURE		
Monotonicity, Guaranteed (Range °C)		
16 Bits	@ +25	+15 to +35
15 Bits	0 to +70	−40 to +85
14 Bits	−40 to +100	−40 to +100
Offset, max	±0.1ppm/°C	*
Gain, max	±0.1ppm/°C	*
STABILITY LONG TERM		
Differential Nonlinearity	±0.1ppm/1000 hours	*
Offset	±0.1ppm/1000 hours	*
Gain	±0.1ppm/1000 hours	*
DYNAMIC PERFORMANCE		
5V Full-Scale Settling Time (to ±1/2LSB)	6μs	*
LSB Settling Time	3μs	*
Glitch Energy (Major Carry @ BW = 20MHz)	800mV × 2μs	*
Total Harmonic Distortion	−98dB	*
ANALOG OUTPUT		
Nominal Voltage Output Range	+5V	*
Voltage Ranges (w/External Amplifier)[2]	−5V, −10V, +5V, +10V, ±5V, ±10V	*
Noise (BW = 0.1-10Hz)	5μV pk-pk	*
Noise (BW = 100kHz)	50μV pk-pk	*
Source Capacitance	18pF	*
Output Impedance	5kΩ	*
POWER SUPPLY REQUIREMENTS (V_{DD})		
w/CMOS Digital Inputs (V_{IN} = V_{DD} or GND)	+5V dc @ 10μA	*
w/TTL Digital Inputs (V_{IN} = 2.4V or 0.5V)	+5V dc @ 3mA	*
Range for Multiplying[3]	$V_{REF} - 0.3 \leq V_{DD} \leq V_{REF} + 0.6V$	*
Total Power @ +5V (Including Reference)		
w/CMOS Digital Inputs	2.5mW	*
w/TTL Digital Inputs	17.5mW	*
POWER SUPPLY SENSITIVITY		
Differential Nonlinearity	0.2ppm/%	*
Offset	10μV/V	*
Gain	10μV/V	*
EXTERNAL REFERENCE INPUT		
Nominal	+5V @ 500μA	*
Range[3]	+3.0V dc to +6.0V dc	*
Input Resistance	10kΩ	*
DIGITAL INPUTS		
V_{IL}	0.8V max @ 10μA max	*
V_{IH}	2.0V min @ 10μA max	*
Parallel & Serial (with Serial Readback)		
Unipolar Code	Binary	*
Bipolar Codes	Offset Binary, Twos Complement	*
TEMPERATURE RANGE		
Rated Performance	−40°C to +100°C	*
Storage	−55°C to +125°C	*
PACKAGE		
Surface Mount Device (AD1145A, B)	44-Pad Plastic Leadless Chip Carrier	*
Leaded Device (AD1145AG, BG)	44-Pin Grid Array	*

NOTES
[1] *Best Straight Line* linearity by manipulation of the gain and/or offset to equalize maximum positive and negative deviations.
[2] For custom voltage ranges use external resistors as shown in Figure 2d and 2e.
[3] V_{DD} must track V_{REF} within +0.6 and −0.3 volts. V_{DD} and V_{REF} can be tied together if the reference voltage is well buffered.
*Specifications same as AD1145A/AG.
Specifications subject to change without notice.

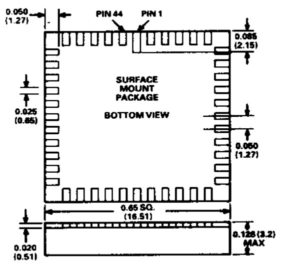
CAUTION: OBSERVE PROPER PLUG-IN POLARITY AND DO NOT PLUG INTO "LIVE" SOCKET – THE CONVERTER MAY BE DAMAGED.

ESDS CLASSIFICATION: MIL-STD-883, METHOD 3015, CATEGORY B

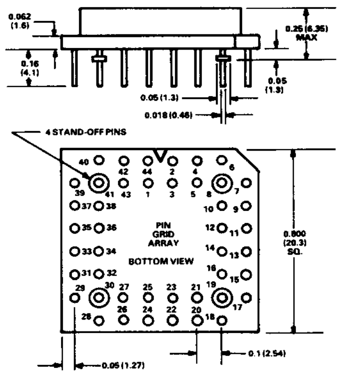
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

PLASTIC LEADLESS CHIP CARRIER*



44-PIN GRID ARRAY*



*PACKAGE NOTES:
A post assembly *water wash* cycle may trap water between the surface mount device and P.C. board. A drying period should be observed before operation (e.g., 65°C bake for 1 hour).
See Table VI for recommended sockets.

AD1145 PIN DESIGNATIONS

PIN	MNEMONIC	DESCRIPTION
1, 11, 12, 23, 34	NC	No Connection
2	DB11	Data Bit 11
3	DB10	Data Bit 10
4	DB9	Data Bit 9
5	DB8	Data Bit 8
6, 18, 28, 40	AGND	Analog Ground
7, 17, 29, 39	V_{REF}	Voltage Reference Input
8	10K	10kΩ Application Resistor
9, 10	20K	20kΩ Application Resistors
13	CODE	Selects Digital Input Code
14	$\overline{CLR}$	Clear, Active Low, Asynchronous
15	$\overline{LDAC}$	Load DAC Register, Active Low Asynchronous
16	CLK	Clock, Rising Edge Triggered
19	DB0/SI	Data Bit 0 (LSB), Serial Input
20	DB1	Data Bit 1
21	DB2	Data Bit 2
22	DB3	Data Bit 3
24	DB4	Data Bit 4
25	DB5	Data Bit 5
26	DB6	Data Bit 6
27	DB7	Data Bit 7
30	$\overline{WRHB}$	Write High Byte, Active Low
31	$\overline{WRLB}$	Write Low Byte, Active Low
32	$\overline{CS}$	Chip Select, Active Low
33	$\overline{RD}$	Readback, Active Low
35	V_{DD}	Digital Power Supply
36	DGND	Digital Ground
37	Σ	Application Resistor Common
38	V_O	DAC Voltage Output
41	DB15/SO	Data Bit 15 (MSB), Serial Output
42	DB14	Data Bit 14
43	DB13	Data Bit 13
44	DB12	Data Bit 12

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OUTPUT AMPLIFIER AND REFERENCE

The users choice of output amplifier and reference to complement the AD1145 will have a direct effect on the overall accuracy, speed and precision of the complete DAC circuit. The AD1145 can be optimized accordingly for a wide range of applications. Internal application resistors are provided to obtain output voltage ranges of 0 to 5V, 0 to 10V, 0 to −5V, 0 to −10V, ±5V, and ±10V. External resistors can be used for custom output voltage ranges as shown in Figure 2.

The AD1145's high impedance (5kΩ) voltage output must be buffered to drive a load since resistive loading at the output introduces a gain error (e.g., 50MΩ load resistance introduces a 0.01% gain error). Op amp bias current flows through the DAC output impedance to introduce an offset term (e.g., 100 nanoamps bias current introduces a 0.01% offset error).

In the noninverting mode the inputs of the operational amplifier swing between 0 and +5 volts. Therefore, to maintain 16-bit linearity the common-mode rejection ratio of the operational amplifier must be at least 96dB over a 5 volt range. Special consideration must be given to offset voltage, offset drift, bias current, bias drift, common-mode rejection, slew rate, and settling time when selecting an operational amplifier. High quality BiFET amplifiers, such as the AD711, are recommended.

The linearity and settling time for the AD1145 have a direct correlation to the output impedance and recovery time of the voltage reference. Therefore, a reference with a fast recovery time and low output impedance, such as the AD586, is recommended. When choosing a voltage reference, gain error and temperature drift must also be considered. A typical reference and output amplifier hookup is shown in Figure 1.

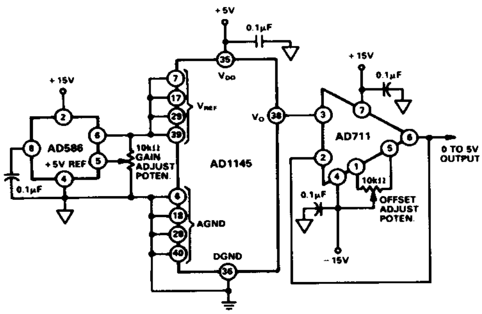


Figure 1. AD1145 Configured for a 0 to 5V Output with External Reference and Unity Gain Amplifier.

OFFSET AND GAIN CALIBRATION

The AD1145 has virtually no offset or gain errors of its own. When connected in a system, such as that shown in Figure 1, the system errors are nulled with external potentiometers. Offset error is nulled by adjusting the offset voltage of the output amplifier. Gain error is nulled by adjusting the output voltage of the external reference. The voltmeter used to measure the output must be capable of 1µV resolution. Offset adjustment should be done before gain adjustment.

UNIPOLAR MODE CALIBRATION

1. Apply a digital input of all "0"s.
2. Adjust the offset potentiometer until a 0.00000V output is obtained.
3. Apply a digital input of all "1"s.
4. Adjust the gain potentiometer until plus full-scale output is obtained. (see Table I for full-scale value).

BIPOLAR MODE CALIBRATION

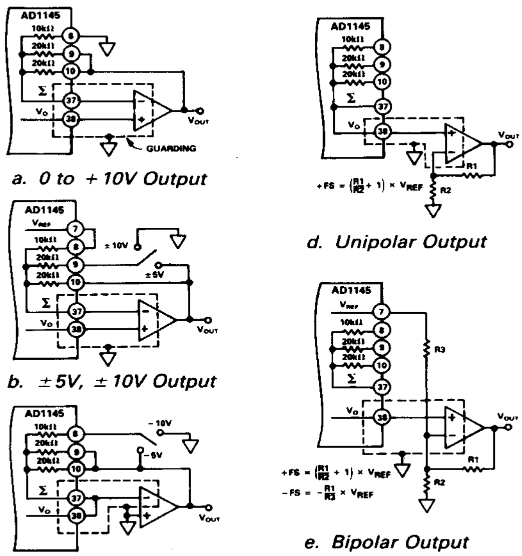
1. Apply a digital input of all "0"s (for offset binary coding) or 8000 Hex (for twos complement coding).
2. Adjust the offset potentiometer until minus full-scale output is obtained (see Table I for value).
3. Apply a digital input of all "1"s (for offset binary coding) or 7FFF Hex (for twos complement coding).
4. Adjust the gain potentiometer until plus full-scale output is obtained (see Table I for full-scale value).

Range	Input Code (Hex)		Output
Unipolar:			
0V to 5V	0000		0.00000V
	FFFF		4.999924V
0V to 10V	0000		0.00000V
	FFFF		9.999848V
	Offset	Twos Comp	
Bipolar:			
−5V to +5V	0000	8000	−5.00000V
	FFFF	7FFF	+4.999848V
−10V to +10V	0000	8000	−10.00000V
	FFFF	7FFF	+9.999695V

Table I. Offset and Gain Adjust

ANALOG OUTPUT RANGE

Figure 2 shows the required external amplifier connections for standard and custom output ranges. See Figure 1 for 0 to 5V.



a. 0 to +10V Output

b. ±5V, ±10V Output

c. 0 to −5V, −10V Output

d. Unipolar Output

e. Bipolar Output

Figure 2. Analog Output Range Configurations

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TIMING DIAGRAM

The timing requirements of the AD1145 are shown in Table II. The timing diagrams for both serial and parallel input modes of operation as well as serial output operation are shown in Figure 3. The serial output mode enables the user to read back data written to the AD1145.

Symbol	Parameter	Requirement
t_{DS}	Data Setup Time	25ns
t_{DH}	Data Hold Time	10ns
t_{WR}	Write Pulse Width	25ns
t_{CWS}	Chip Select to Write Setup	0ns
t_{CWH}	Chip Select to Write Hold	0ns

Table II. Timing Requirements

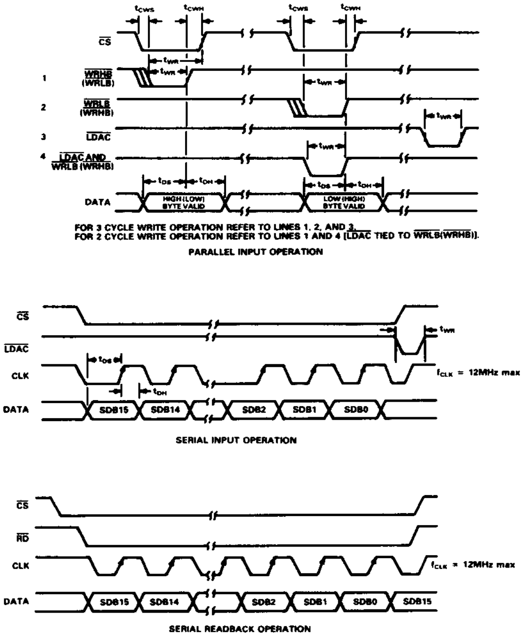

Figure 3. Timing Diagrams

The AD1145 has eight control lines. A brief description of each line follows:

$\overline{\text{CS}}$ is the Chip Select line and allows multiple AD1145s to share the same input bus. The desired DAC is selected with the $\overline{\text{CS}}$ line. A low on this line enables $\overline{\text{WRLB}}$, $\overline{\text{WRHB}}$, CLK, and $\overline{\text{RD}}$ of the selected DAC.

$\overline{\text{WRLB}}$ is the WRite line for the Low Byte input register. A low on this line makes the register transparent. A high level latches the input data into the register.

$\overline{\text{WRHB}}$ is the WRite line for the High Byte input register. Operation is the same as $\overline{\text{WRLB}}$.

$\overline{\text{LDAC}}$ is the Load line for the DAC register. A low on this line makes the DAC register transparent. A high level latches the data from the input registers into the DAC register. $\overline{\text{LDAC}}$ operates independently of $\overline{\text{CS}}$.

CLK is the line used to CLocK serial data into or out of the input registers. Data is moved on each positive transition of CLK. Note that CLK must be held high for parallel operation.

$\overline{\text{RD}}$ is the ReaD line. A low on this line enables the serial output function and also connects the serial output to the serial input.

$\overline{\text{CLR}}$ is the CLeaR line. A low on this line clears the DAC output to zero volts regardless of input coding. $\overline{\text{CLR}}$ operates independently of $\overline{\text{CS}}$.

CODE determines the input coding of the DAC. A low on this line inverts the MSB for twos complement coding. A high does not invert the MSB (for binary and OBN codes).

PARALLEL OPERATION

The AD1145 is fully compatible with either 8- or 16-bit microprocessor systems. In an 8-bit system, data may be loaded using either two or three instruction cycles, with either the high byte or the low byte being loaded first. Typical load sequences are (1) load high byte, load low byte, load DAC register, or (2) load high byte, load low byte and DAC register. With a 16-bit system, data may be loaded using either one, or two, instruction cycles, or the DAC may be operated with all of its registers transparent. Table III illustrates the AD1145's parallel operation as a function of its control lines. Note that CLK and $\overline{\text{RD}}$ must be held high for parallel operation.

$\overline{\text{CLR}}$	$\overline{\text{CS}}$	$\overline{\text{WRLB}}$	$\overline{\text{WRHB}}$	$\overline{\text{LDAC}}$	OPERATION
0	X	X	X	X	Reset DAC Output to Zero Volts.
1	0	0	0	0	Input and DAC Registers are Transparent.
1	0	0	0	1	Load High Byte and Low Byte Input Registers.
1	0	0	1	0	Load DAC Register from High Byte Register and Transparent Low Byte Inputs.
1	0	0	1	1	Load Low Byte Input Register.
1	0	1	0	0	Load DAC Register from Low Byte Register and Transparent High Byte Inputs.
1	0	1	0	1	Load High Byte Input Register.
1	0	1	1	0	Load DAC Register from Input Registers.
1	1	X	X	0	Load DAC Register from Input Registers.
1	1	X	X	1	No Operation.
1	X	1	1	1	No Operation.

Table III. Parallel Operation Truth Table

SERIAL OPERATION

In the serial mode, data is written from DB0/SI into the input register on each positive going transition of the clock. For error checking, data can also be readback from the input register to DB15/SO. The serial output is switched internally to the serial input in the readback mode so that the data is recirculated as it is read. In this way the data is restored after 16 clock cycles. The data in the DAC register and hence the DAC output voltage is unchanged during readback. Table IV shows the serial operation of the AD1145 as it relates to the status of the control lines.

INPUT CODING

The AD1145 accepts data in twos complement, offset binary, or straight binary formats. The code pin either *inverts* or *not inverts*

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$\overline{CLR}$	$\overline{CS}$	CLK	$\overline{RD}$	$\overline{LDAC}$	OPERATION
0	x	x	x	x	Reset DAC Output to Zero Volts.
1	0	↑	1	1	Clock Serial Data from DB0/SI into Input Register.
1	0	↑	0	1	Clock Serial Data from Input Register out to DB15/SO.
1	x	x	x	0	Load DAC Register.
1	x	↓	x	1	No Operation.

Table IV. Serial Operation Truth Table

the MSB. If code is low, the MSB is inverted for twos complement coding. If code is high, the MSB is true for straight binary and offset binary coding. See Table V for further detail.

CLEAR LINE OPERATION

The clear line, in conjunction with the code line, resets the DAC output to zero volts. For straight binary operation CODE should be tied to $+V_{DD}$, the MSB will not be inverted, the DAC register gets reset to 0000H, and the AD1145's output is reset to zero volts. For twos complement operation, CODE is tied to DGND, the MSB is inverted, the DAC register is reset to 1/2 full scale, and the AD1145's output is reset to zero volts. For offset binary operation CODE is tied to $\overline{CLR}$. In this way the MSB is not inverted in normal operation but on CLEAR the MSB gets inverted, the DAC register is reset to 1/2 full scale, and the AD1145's output is reset to zero volts. Table V shows the clear operation as a function of CODE input.

$\overline{CLR}$	CODE	OPERATION
0	0	BIPOLAR CLEAR (Twos Complement, Offset Binary)
0	1	UNIPOLAR CLEAR (Binary)
1	0	MSB INVERTED (Twos Complement)
1	1	MSB TRUE (Binary, Offset Binary)

Table V. Clear Operation Truth Table

POWER-UP RESET

In the event of a power failure, the DAC output is automatically reset to zero volts upon power-up. When CODE is high, the DAC is reset to zero for a unipolar clear. When CODE is low, the DAC is reset to 1/2 full scale for a bipolar clear (zero volt output).

GROUNDING AND GUARDING

The AD1145 is a precision D/A converter with 76µV LSB resolution at a FSR of 5V. Special care must be taken to insure proper layout, grounding, and guarding. Analog and digital grounds should be individually star pointed and then tied together at a single point near the measurement point. High-speed digital inputs should be kept separate from low level analog outputs. Power supplies should be locally bypassed around all high-speed components and at the power supply input to the printed circuit board. All high impedance nodes such as the DAC output and amplifier inputs are sensitive to interference from the digital input lines. They should be surrounded by low impedance guard tracks at all times. Figure 2 shows the proper guarding of the AD1145 depending on output configuration.

SINGLE SUPPLY OPERATION

The AD1145 can operate with V_{DD} connected to V_{REF}. If CMOS is used to drive the DAC inputs, the static current drawn from V_{DD} will be less than 10µA. If TTL is used to drive the DAC inputs, the static current draw will be increased to about 3mA depending on the digital input. Therefore, the reference must be well buffered to avoid code dependent errors when TTL inputs are used. Figure 4 shows the AD1145 operating from a single supply.

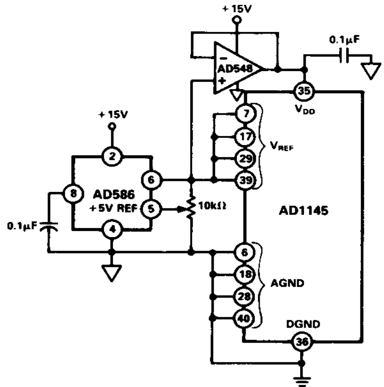

Figure 4. Single Supply Configuration

MULTIPLYING DAC OPERATION

The AD1145 operates as a two quadrant multiplying DAC over a limited voltage range. V_{REF} can vary between 3 and 6 volts. V_{DD} must track V_{REF} within $+0.6$ and -0.3 volts. Logic levels will vary with V_{DD}, with a logic low being less than $1/3V_{DD}$ and a logic high being greater than $2/3V_{DD}$. V_{DD} and V_{REF} may be tied together provided the reference voltage is well buffered.

A useful application of the multiplying feature is to set the reference voltage to 4.096 volts and configure the DAC as shown in Figure 2b for ±10V range. This provides a ±8.192 volt full-scale output for a bit weight of 0.25mV per LSB.

MULTIPLE DAC APPLICATION

The AD1145 is well suited for applications using multiple DACs sharing the same data bus, as in automated test equipment. Figure 5 shows a typical multiple DAC hookup. Note that the $\overline{WRLB}$, $\overline{WRHB}$, $\overline{LDAC}$, $\overline{RD}$, $\overline{CLR}$, and CLK lines from each DAC are tied together. A separate chip select ($\overline{CS}$) line is provided to individually select each DAC. Data can be written to one or all DACs by appropriate selection of the chip select lines. All DACs may be simultaneously updated by strobing the $\overline{LDAC}$ line. A separate CODE line is provided for each DAC so that they may be independently configured for unipolar and bipolar coding.

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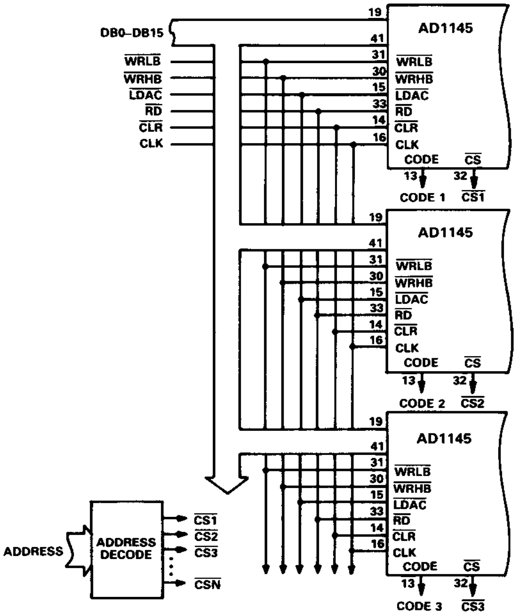

Figure 5. Multiple DAC Application

PARALLEL READBACK

Full parallel readback can be achieved by adding two 74ALS990 octal D-type read-back latch chips as shown in Figure 6. These latches also reduce digital feedthrough from the data bus; an important consideration in high accuracy systems.

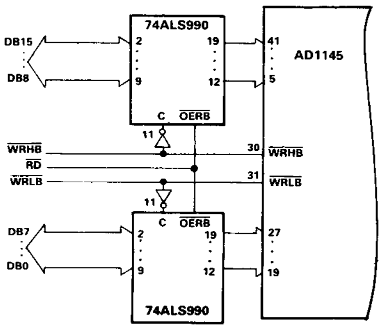

Figure 6. Parallel Readback

PACKAGE INFORMATION

The AD1145 is packaged in a 44-pad glass epoxy chip carrier. This package is ideal for automated surface mounting due to its excellent dimensional tolerances and planarity. As the package is made from the same material as printed circuit boards, it has the same temperature coefficient of expansion. This minimizes stress and maximizes product reliability. Standard JEDEC leadless chip carrier sockets such as those manufactured by Textool can be used for testing. For conventional through-hole mounting, the AD1145 is also available in a PGA package. See Table VI for recommended sockets.

Simple 8-Bit and 16-Bit Data Bus Connections

The AD1145 can be configured to directly connect to an 8-bit or 16-bit data bus. An 8-bit microprocessor requires at least two write cycles to supply 16 bits of input data. Utilizing the AD1145's high byte and low byte input registers, one byte at a time is loaded from the 8-bit bus. The 16-bit DAC register can be latched during or after the second byte write operation. Figure 7 shows a typical AD1145 connection to an 8-bit bus. Note that the three logic gates can be eliminated if two address lines are available.

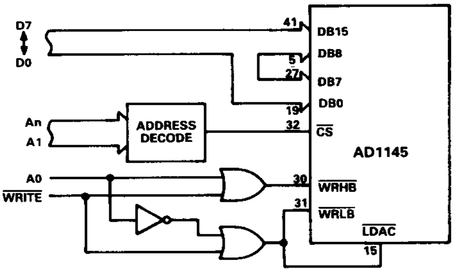

Figure 7. 8-Bit Microprocessor Interface

A 16-bit microprocessor supplies a complete 16-bit input in a single write cycle. This eliminates the requirement for the individual high byte and low byte input latches. Figure 8 shows a typical AD1145 connection to a 16-bit bus. The 16-bit DAC register is made transparent by grounding the $\overline{\text{LDAC}}$ line or can be strobed for full double buffering.

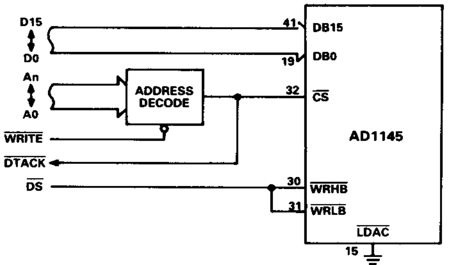

Figure 8. 16-Bit Microprocessor Interface

Package	Purpose	Manufacturer	Mfg. Part No.
PLLCC	Test	Textool	244-4961-000
PGA	Test	Amp	55280-4
PGA	Production	Advanced Interconnections Augat Samtec	CS044-01TG PPS044-3A0802-L MPAS–044-ZS-8

Table VI. Recommended Sockets

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