REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 05. Add case outline Z. Update boilerplate. Editorial changes throughout.	95-06-20	

REV																			
SHEET																			
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A				
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29				

REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
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CHECKED BY
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APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
93-08-31

REVISION LEVEL
A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 256K X 1 STATIC RANDOM ACCESS MEMORY (SRAM), SEPARATE I/O, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-93128
A	67268	

SHEET 1 OF 29

DESC FORM 193
JUL 94

5962-E160-95

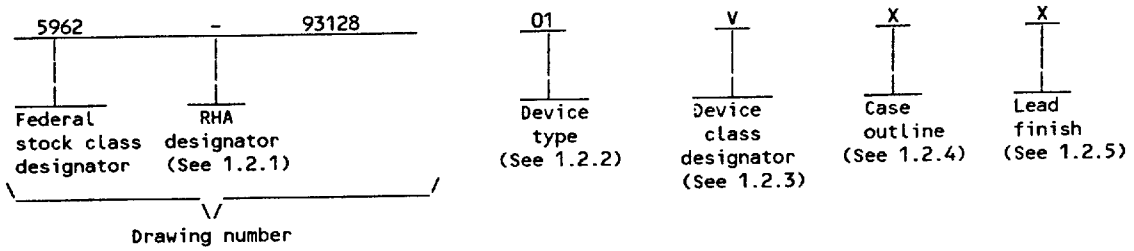
DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

9004708 0011697 359

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Access Time
01		256K x 1 CMOS SRAM (CMOS-I/O)	60
02		256K x 1 CMOS SRAM (TTL-I/O)	60
03		256K x 1 CMOS SRAM (CMOS-I/O)	40
04		256K x 1 CMOS SRAM (TTL-I/O)	40
05		256K x 1 CMOS SRAM (TTL-I/O)	50

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as disignated in MIL-STD-1835 and as follows:

Outline letter	Descriptive Designator	Terminals	Package Style
X	See figure 1	36	Flat pack
Y	See figure 1	40	Flat pack
Z	See figure 1	36	Flat pack

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1/ Generic numbers are listed on the Standard Military Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-BUL-103 and QML-38535.

1.3 Absolute maximum ratings. 2/ 3/

Supply voltage range (V_{CC})	-2.0 V dc to +7.0 V dc
DC input voltage range (V_{IN})	-0.5 V dc to V_{CC} + 0.5 V dc
DC output voltage range V_{OUT})	-0.5 V dc to V_{CC} + 0.5 V dc
Output voltage applied to high Z state	-0.5 V dc to V_{CC} + 0.5 V dc
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 5 sec)	+250°C
Thermal resistance, junction-to-case (Θ_{JC}):	
Cases X and Y	3.31°C/Watt
Maximum power dissipation (P_D)	2.0 Watts
Maximum junction temperature (T_J)	+175°C 4/

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc
Supply voltage (V_{SS})	0.0 V dc
High level (CMOS) input voltage range (V_{IH})	3.5 V dc to V_{CC} + 0.3 V dc
High level (TTL) input voltage range (V_{IH})	2.2 V dc to V_{CC} + 0.5 V dc
Low level (CMOS) input voltage range (V_{IL})	-0.3 V dc to 1.5 V dc
Low level (TTL) input voltage range (V_{IL})	-0.5 V dc to 0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	100 percent

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standard Microcircuit Drawings (SMD's).

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ All voltages referenced to V_{SS} (V_{SS} = ground), unless otherwise specified.
4/ Maximum junction temperature may be increased to +175°C during burn-in and steady-state life.

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-88 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of Latch-up in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2500 Wilson Boulevard, Arlington, VA 22201.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth Table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be as specified in figure 6.

3.2.5 Functional tests. Various functional tests used to test this device are contained in the appendix. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device class M, alternate test patterns shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request. For device classes Q and V alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the preparing or acquiring activity upon request.

3.2.6 Die overcoat. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection only. Each coated microcircuit inspection lot (see inspection lot as defined in MIL-I-38535) shall be subjected to and pass the internal moisture content test at 5000 ppm (see method 1018 of MIL-STD-883). The frequency of the internal water vapor testing shall not be decreased unless approved by the preparing activity for class M. The TRB will ascertain the requirements as provided by MIL-I-38535 for classes Q and V. Samples may be pulled any time after seal.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 41 (see MIL-I-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -200 µA, V_{IH} = 3.5 V, V_{IL} = 1.5 V		1,2,3	01,03	V_{CC}-.05		V
		V_{CC} = 4.5 V, I_{OH} = -4 mA, V_{IH} = 2.2 V, V_{IL} = 0.8 V			02,04, 05	2.4		
			M,D, L,R, F,G, H	1 2/		3/		V
Low level output voltage	V_{OL}	V_{CC} = 5.5 V, I_{OL} = 200 µA, V_{IL} = 1.5 V, V_{IH} = 3.5 V		1,2,3	01,03		0.05	V
		V_{CC} = 4.5 V, I_{OL} = 8 mA, V_{IH} = 2.2 V, V_{IL} = 0.8 V			02,04, 05		0.4	
			M,D, L,R, F,G, H	1 2/			3/	V
Input leakage current	I_{ILK}	V_{CC} = 5.5 V, V_{IN} = 0.0 V to 5.5 V, all other pins at 0.0 V		1,2,3	All	-5	5	µA
			M,D, L,R, F,G, H	1 2/		3/	3/	µA
Output leakage current	I_{OLK}	V_{CC} = 5.5 V, V_{OUT} = 0.0 V to 5.5 V, all other pins at 0.0 V		1,2,3	All	-10	10	µA
			M,D, L,R, F,G, H	1 2/		3/	3/	µA
Data retention voltage	V_{DR}	V_{CC} = 2.5 V		1,2,3	All	2.5		V
			M,D, L,R, F,G, H	1 2/		3/		V
Operating supply current	I_{CC1}	V_{CC} = 5.5 V, f = f_{MAX} 4/, E = GND, no output loading		1,2,3	All		70	mA
			M,D, L,R, F,G, H	1 2/			3/	mA

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Device type	Limits Min	Limits Max	Unit
Supply current (deselected)	I_{CC2}	V_{CC} = 5.5 V, f = f_{MAX} 4/, $\overline{E}$ = V_{CC}		1,2,3	All		2	mA
			M,D,L,R	1				
			F,G,H	2/			3/	mA
Supply current (standby)	I_{CC3}	V_{CC} = 5.5 V, f = 0.0 MHz, $\overline{E}$ = V_{CC}, all other inputs = V_{CC} or GND		1,2,3	All		2	mA
			M,D,L,R	1				
			F,G,H	2/			3/	mA
Data retention current	I_{CC4}	V_{CC} = 2.5 V		1,2,3	All		1	mA
			M,D,L,R	1				
			F,G,H	2/			3/	mA
Supply current (cycling, selected)	I_{CC5}	$\overline{E}$ = V_{IL} = GND, f = 4.0 MHz, no output loading		1,2,3	All		25	mA
			M,D,L,R	1				
			F,G,H	2/			3/	mA
Input capacitance 5/	C_{IN}	$0.0 \le V_{IN} \le V_{CC}$, T_A = +25°C, f = 1.0 MHz, see 4.4.1e		4	All		4	pF
Output capacitance 5/	C_{OUT}	$0.0 \le V_{OUT} \le V_{CC}$, T_A = +25°C, f = 1.0 MHz, see 4.4.1e		4	All		7	pF
Functional tests		See 4.4.1c		7,8A,8B	All			
			M,D,L,R	9				
			F,G,H	2/		3/		
Read cycle								
Read cycle time	t_{AVAV}			9,10,11	01,02	60		ns
					05	50		
					03,04	40		
			M,D,L,R	1				
			F,G,H	2/		3/		ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified		Group A subgroups	Device type	Limits Min	Limits Max	Unit
Address access time	t_{AVQV}			9,10,11	01,02		60	ns
					05		50	
					03,04		40	
			M,D, L,R, F,G, H	1 2/			3/	ns
Chip enable access time	t_{ELQV}			9,10,11	01,02		60	ns
					05		50	
					03,04		40	
			M,D, L,R, F,G, H	1 2/			3/	ns
Output enable access time	t_{GLQV}			9,10,11	All		15	ns
			M,D, L,R, F,G, H	1 2/			3/	ns
Chip enable to output active	t_{ELQX}			9,10,11	All	3		ns
			M,D, L,R, F,G, H	1 2/		3/		ns
Output enable to output active	t_{GLQX}			9,10,11	All	3		ns
			M,D, L,R, F,G, H	1 2/		3/		ns
Output hold after address change	t_{AXQX}			9,10,11	All	5		ns
			M,D, L,R, F,G, H	1 2/		3/		ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Chip disable to output disable	t_{EHQZ}		9,10,11	All		15	ns
		M,D, L,R, F,G, H	1				
			2/			3/	ns
Output enable to output disable	t_{GHQZ}		9,10,11	All		15	ns
		M,D, L,R, F,G, H	1				
			2/			3/	ns
Write cycle							
Write cycle time	t_{AVAV}		9,10,11	01,02	60		ns
				05	50		
				03,04	40		
		M,D, L,R, F,G, H	1				
			2/		3/		ns
Write pulse width	t_{WLWH}		9,10,11	01,02	55		ns
				05	45		
				03,04	35		
		M,D, L,R, F,G, H	1				
			2/		3/		ns
Chip enable to end of write	t_{ELWH}		9,10,11	01,02	55		ns
				05	45		
				03,04	35		
		M,D, L,R, F,G, H	1				
			2/		3/		ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Address setup to end of write	t_{AVWH}		9,10,11	01,02	55		ns
				05	50		
				03,04	35		
		M,D, L,R, F,G, H	1				
			2/		3/		ns
Data setup to end of write	t_{DVWH}		9,10,11	01,02, 05	40		ns
				03,04	30		
		M,D, L,R, F,G, H	1				
			2/		3/		ns
Data hold after end of write	t_{WHDX}		9,10,11	All	5		ns
		M,D, L,R, F,G, H	1				
			2/		3/		ns
Address setup to start of write	t_{AVWL}		9,10,11	All	0		ns
		M,D, L,R, F,G, H	1				
			2/		3/		ns
Address hold after end of write	t_{WHAX}		9,10,11	All	0		ns
		M,D, L,R, F,G, H	1				
			2/		3/		ns
Output active after end of write	t_{WHQX}		9,10,11	All	1		ns
		M,D, L,R, F,G, H	1				
			2/		3/		ns
Write enable to output disable	t_{WLQZ}		9,10,11	All		15	ns
		M,D, L,R, F,G, H	1				
			2/			3/	ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Write disable pulse width	t_{WHWL}		9,10,11	All	5		ns
		M,D, L,R,	1				
		F,G, H	2/		3/		ns

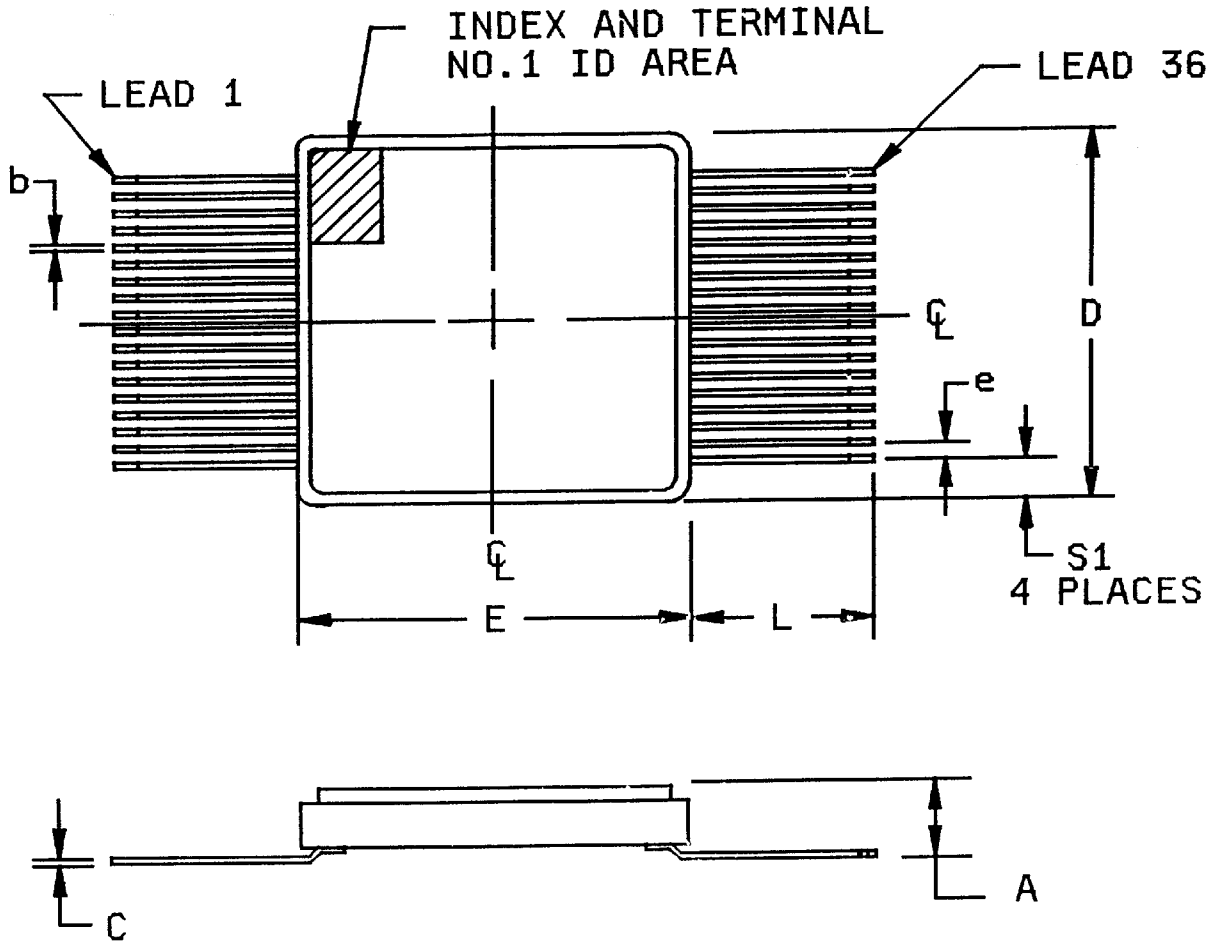
1/ AC measurements assume transition times ≤ 2 ns/volt. For output load circuit, see figure 4 and for timing waveforms, see figure 5.
2/ When performing postirradiation electrical measurements for any RHA level $T_A = +25°C$. Limits shown are guaranteed at $T_A = +25°C \pm 5°C$. The M, D, L, R, F, G, and H in the test condition column are the postirradiation limits for the device types specified in the device types column.
3/ Preirradiation values for RHA marked devices shall also be the postirradiation values, unless otherwise specified.
4/ $f_{MAX} = 1/t_{AVAV}$ (minimum).
5/ Tested initially and after any design or process changes which may affect that parameter, and therefore shall be guaranteed to the limits specified in table IA.

TABLE IB. SEP test limits. 1/ 2/

Device type	T_A = Temperature ±10°C 3/	Memory pattern	V_{CC} = 4.5 V		Bias for latch-up test V_{CC} = 5.5 V no latch-up LET = 3/
			Effective LET no upsets [MEV/(mg/cm²)]	Maximum device cross section (μm^2) (LET = 120)	
All	+125°C	4/	≥ 120	≤ 100	≥ 120

1/ For SEP test conditions, see 4.4.5 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Worst case temperature T_A = +125°C.
4/ Testing shall be performed using checkerboard and checkerboard bar test patterns.

Case X (see note)

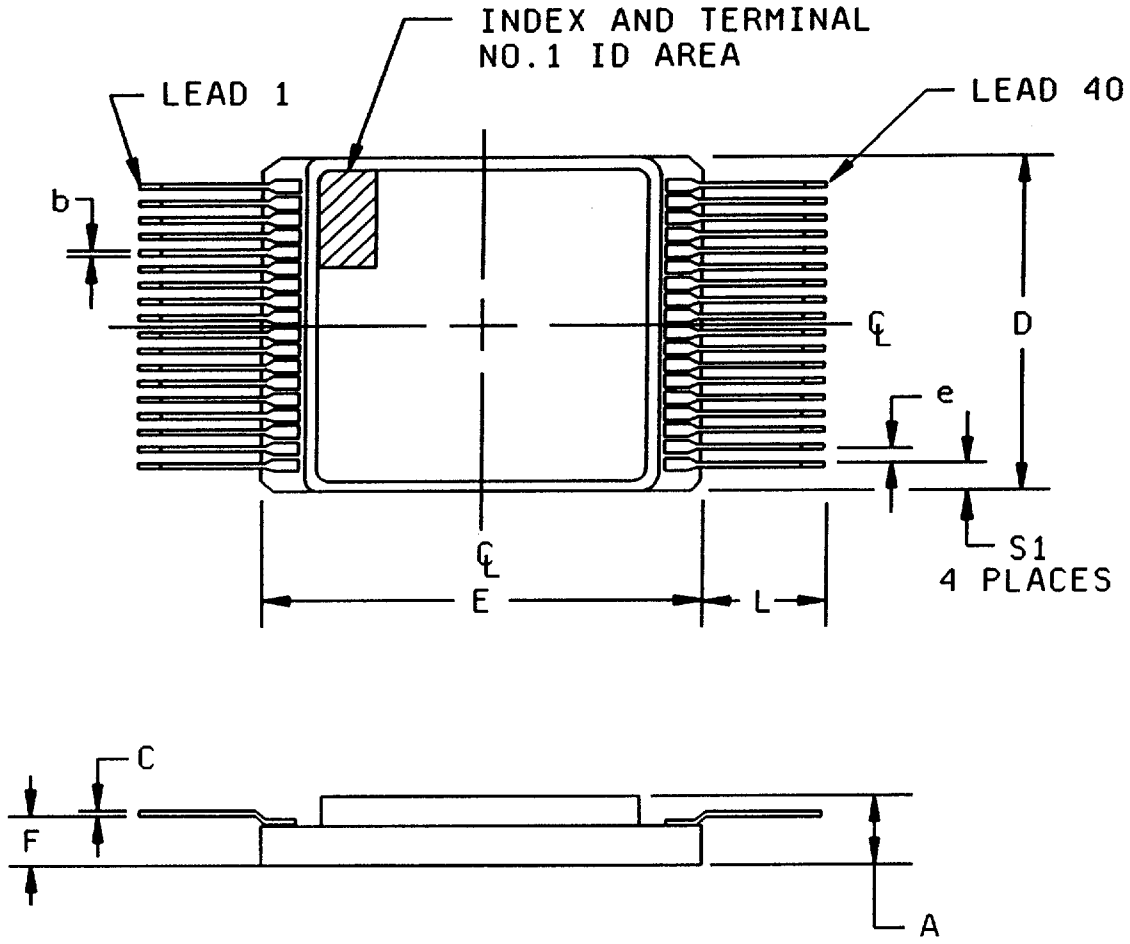


Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	1.91	2.41	.075	.095
b	.18	.25	.007	.010
s1	2.62	3.12	.103	.123
c	.11	.15	.004	.006
D	16.26	16.76	.640	.660
E	15.82	16.18	.623	.637
e	0.64 BSC		0.025 BSC	
L	5.96	7.24	.235	.285

Note: The US government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.

FIGURE 1. Case outlines.

Case Y (see note)



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	1.68	1.98	.066	.078
b	.18	.25	.007	.010
s1	1.98	2.48	.078	.098
c	.11	.15	004	.006
D	16.26	16.76	.640	.660
E	19.48	19.88	.768	.783
F	1.53	1.93	.060	.076
e	0.64 BSC		.025 BSC	
L	6.04	7.32	.238	0.288

Note: The US government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.

FIGURE 1. Case outlines - continued.

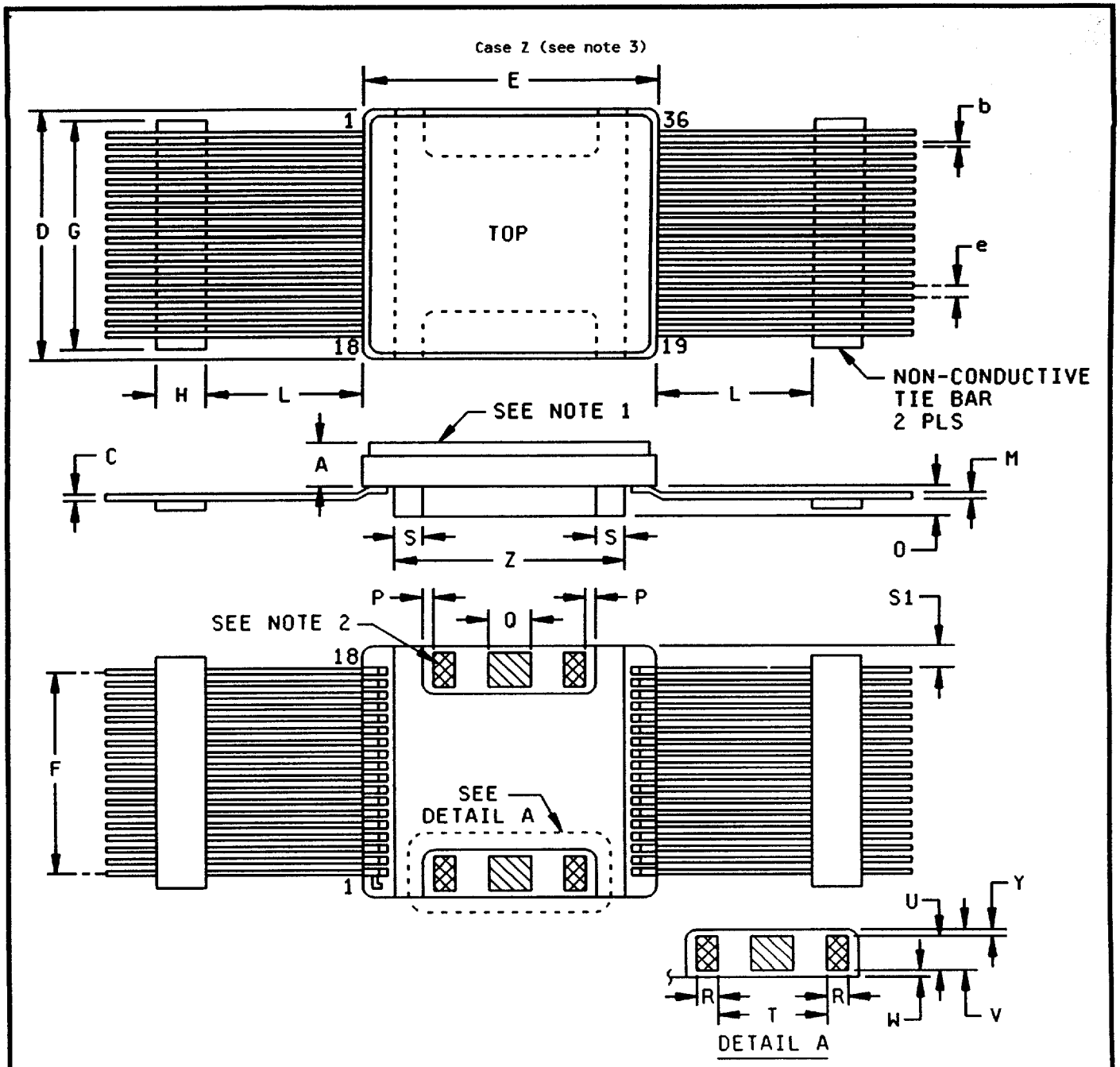


FIGURE 1. Case outlines - continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-93128
		REVISION LEVEL A	SHEET 15

DESC FORM 193A
JUL 94

9004708 0011711 559

Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	.075	.095	1.91	2.41
b	.007	.010	.178	.254
C	.0050	.0075	.127	.191
D	.640	.660	16.26	16.76
E	.623	.637	15.82	16.18
e	0.025 BSC		0.64 BSC	
F	.421	.429	10.69	10.90
G	0.525 REF		13.34 REF	
H	0.135 REF		3.43 REF	
L	.270	.300	6.86	7.62
M	.005	.011	.127	.279

Symbol	Inches		Millimeters	
	Min	Max	Min	Max
O	.045	.055	1.14	1.39
P	0.010 REF		0.254 REF	
Q	.075	.085	1.91	2.15
R	0.040 REF		1.02 REF	
S	.070	.080	1.77	2.03
S1	.103	.123	2.62	3.12
T	0.240 REF		6.10 REF	
U	0.100 REF		2.54 REF	
V	0.115 REF		2.92 REF	
W	0.005 REF		0.13 REF	
Y	0.010 REF		0.25 REF	
Z	0.490 REF		12.45 REF	

NOTES: 1. Lid tied to V_{SS}.
2. The indicated terminal pad is P1. Terminal pads are numbered clockwise (bottom view) through P6.
3. The US government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.

FIGURE 1. Case outlines - continued.

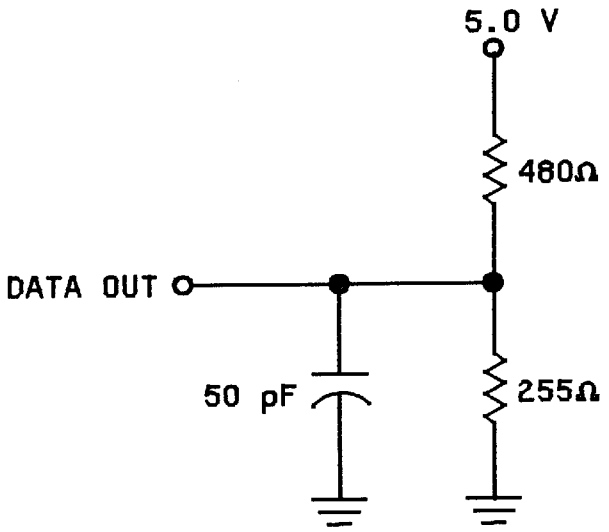
Device types	All		
Case Outline	X	Y	Z
Terminal No.	Terminal symbol		
1	GND	NC	GND
2	V_{CC}	GND	V_{CC}
3	NC	V_{CC}	NC
4	A_0	NC	A_0
5	A_{10}	A_0	A_{10}
6	A_9	A_{10}	A_9
7	A_7	A_9	A_7
8	A_8	A_7	A_8
9	A_{11}	A_8	A_{11}
10	A_{12}	A_{11}	A_{12}
11	A_{13}	A_{12}	A_{13}
12	A_{14}	A_{13}	A_{14}
13	$\overline{Q}$	A_{14}	$\overline{Q}$
14	$\overline{G}$	$\overline{Q}$	$\overline{G}$
15	$\overline{W}$	$\overline{G}$	$\overline{W}$
16	NC	$\overline{W}$	NC
17	V_{CC}	NC	V_{CC}
18	GND	V_{CC}	GND
19	GND	GND	GND
20	V_{CC}	NC	V_{CC}
21	NC	NC	NC
22	$\overline{E}$	GND	$\overline{E}$
23	D	V_{CC}	D
24	NC	NC	NC
25	A_1	$\overline{E}$	A_1
26	A_{15}	D	A_{15}
27	A_2	NC	A_2
28	A_{17}	A_1	A_{17}
29	A_6	A_{15}	A_6
30	A_5	A_2	A_5
31	A_4	A_{17}	A_4
32	A_3	A_6	A_3
33	A_{16}	A_5	A_{16}
34	NC	A_4	NC
35	V_{CC}	A_3	V_{CC}
36	GND	A_{16}	GND
37	---	NC	---
38	---	V_{CC}	---
39	---	GND	---
40	---	NC	---
P1	---	---	V_{CC}
P2	---	---	GND
P3	---	---	V_{CC}
P4	---	---	V_{CC}
P5	---	---	GND
P6	---	---	V_{CC}

FIGURE 2. Terminal connections.

DEVICE TYPES: All (See notes 1, 2, and 3)						
MODE	$\overline{E}$	$\overline{W}$	$\overline{G}$	D	Q	POWER
WRITE	Low	Low	X	Data-in	High-Z	Active
READ	Low	High	Low	X	Data-Out	Active
STANDBY	High	X	X	X	High-Z	Standby

NOTES:
1. Low = V_{IL}, High = V_{IH}, X = V_{IH} or V_{IL}.
3. When in standby mode, $\overline{E}$ must be $V_{IH} = V_{CC}$ to dissipate minimum standby power.
2. When $\overline{G}$ = high, Q is high-Z.

FIGURE 3. Truth Table.



Note: Capacitance includes scope and jig (minimum value).

AC test conditions

Input pulse levels	GND to V_{CC}
Input rise and fall times	≤ 2 ns/V
Input timing reference levels	2.5 V
Output reference levels	2.5 V

FIGURE 4. Output Load Circuit.

Read cycle

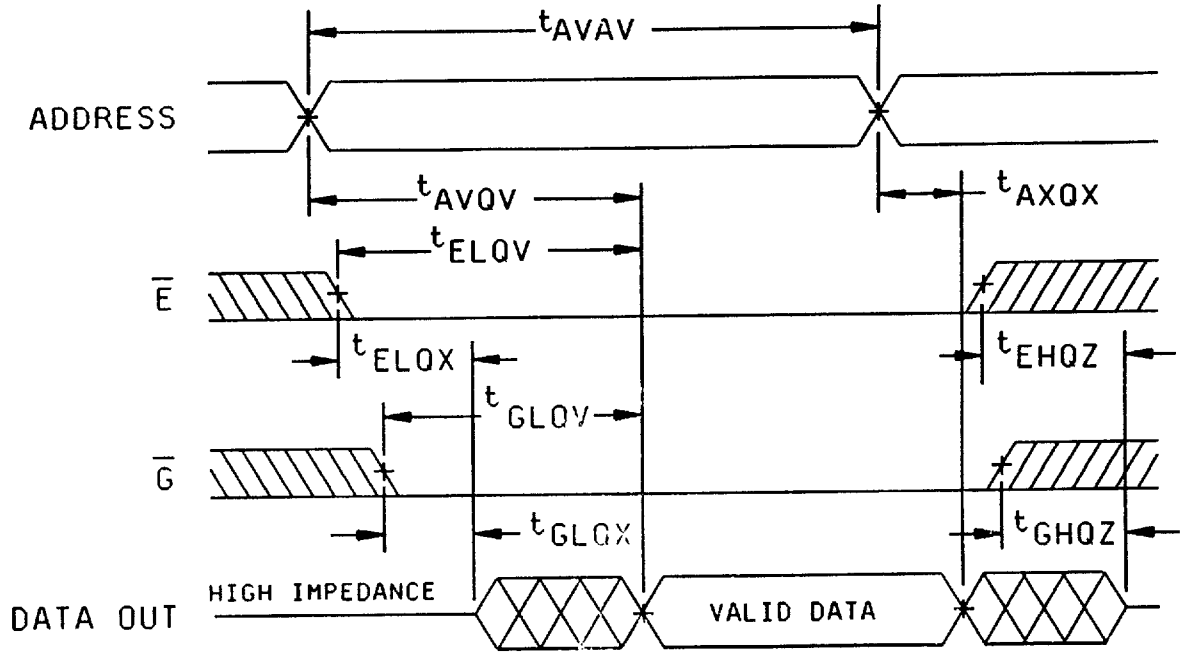
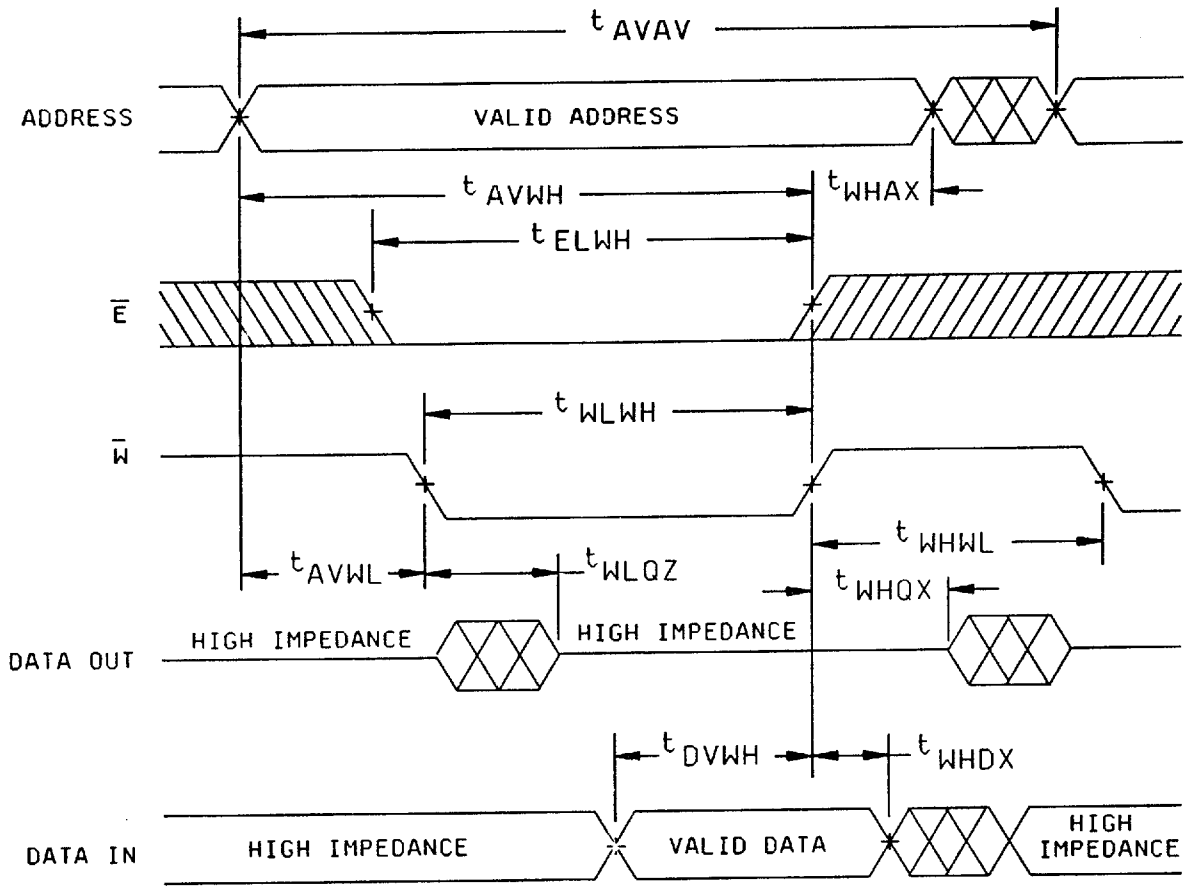


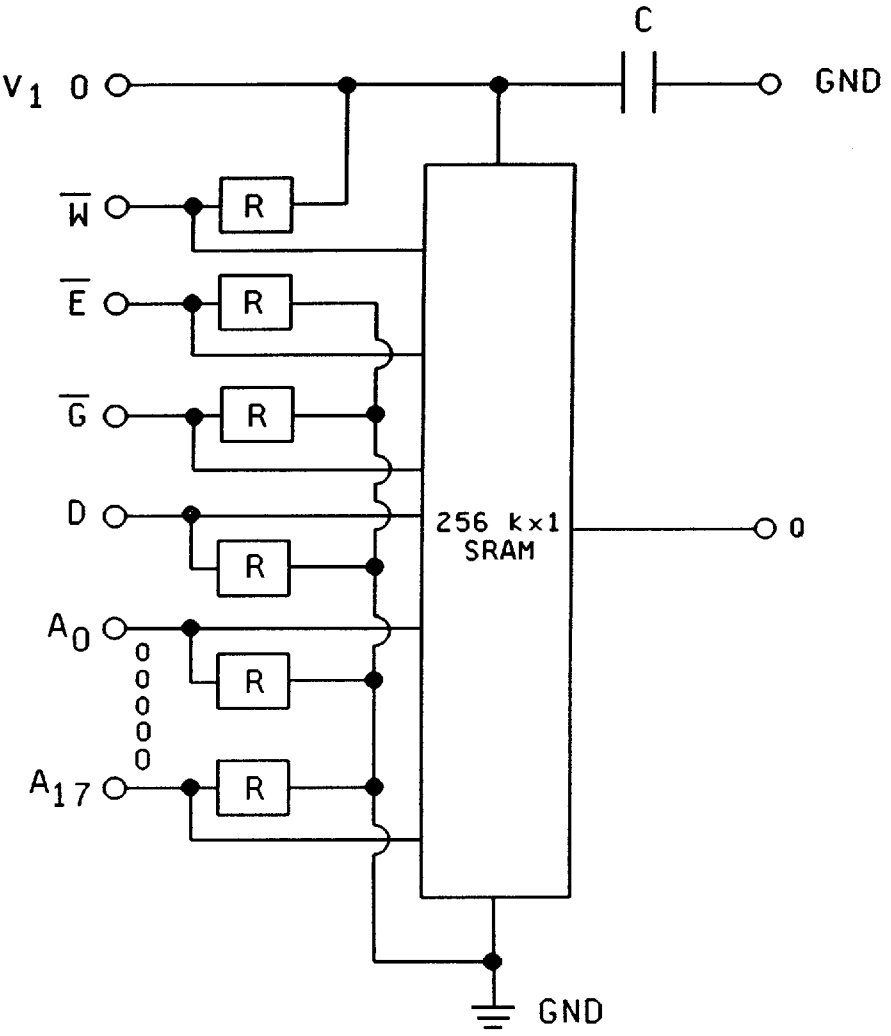
FIGURE 5. Timing waveforms.

Write cycle (see notes 1, 2, 3, and 4)



NOTES:
1. The writing of the RAM is initiated by the high to low transition on $\overline{W}$.
2. Write cycle data is latched by the first occurrence of $\overline{E}$ high or $\overline{W}$ high.
3. $\overline{E}$ high or $\overline{W}$ high must occur while address transitions.
4. Write cycle time is guaranteed for toggling $\overline{E}$ or holding $\overline{E}$ in an active state.

FIGURE 5. Timing waveforms - continued.



Notes:
1. Module power pins connected to V1.
2. The absolute voltage ratings of Section 1.3 shall not be exceeded.
3. ESD precautions shall be followed.
4. The pattern in the memory array will be checkerboard for irradiation and accelerated aging tests.
5. Pin conditions:

V_1 = 5.0 V	$\overline{W}$ = VIH	D,$\overline{E}$,$\overline{G}$ = VIL	
V_{IL} = GND	Q = Floating	C = 0.1 uF	(± 10%)
V_{IH} = VDD	A_0 - A_{17} = VIL	R = 10 KΩ	(± 10%)

FIGURE 6. Radiation exposure circuit.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)			1,7,9
2	Static burn-in I and II (method 1015)	Not required	Not required	Required
3	Same as line 1			1*,7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*,7* Δ
6	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9, 10,11
7	Group A test requirements	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11
8	Group C end-point electrical parameters	2,3,7, 8A,8B	1,2,3,7, 8A,8B	1,2,3,7, 8A,8B,9, 10,11 Δ
9	Group D end-point electrical parameters	2,3, 8A,8B	2,3, 8A,8B	2,3, 8A,8B
10	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1). For device classes Q and V performance of delta limits shall be as specified in the manufacturer's QM plan.
7/ See 4.4.1d.

TABLE IIB. Delta limits at +25°C.

Test 1/	All device types
I_{CC3} standby	±10 percent of specified value in table IA
I_{ILK}, I_{OLK}	±10 percent of specified value in table IA

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta Δ.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class M, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Dynamic burn-in for device class M (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

c. Interim and final electrical parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard number 17 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 1 of group C inspection and shall consist of tests specified in table IIB herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, L, R, F, G, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 and as specified herein.

4.4.4.1.1 Accelerated aging test. Accelerated aging tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latchup testing. Dose rate induced latchup testing shall be performed in accordance with test method 1020 of MIL-STD-883 and as specified herein. Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may effect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. Dose rate upset testing shall be performed in accordance with test method 1021 of MIL-STD-883 and herein.

a. Transient dose rate upset testing for class M devices shall be performed at initial qualification and after any design or process changes which may effect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-I-38535. Device parametric parameters that influence upset immunity shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-I-38535.

4.4.4.4 Single event phenomena (SEP). SEP testing shall be required on class V devices. SEP testing shall be performed on the SEC or alternate SEP test vehicle as approved by the qualifying activity at inital qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM standard F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The test temperature shall be +25 °C and the maximum rated operating temperature ±10 °C.

f. Bias conditions shall be V_{CC} = 4.5 V dc for the upset measurements and V_{CC} = 5.5 V dc for the latchup measurements.

g. For SEP test limits, see Table IB herein.

4.4.4.5 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied.

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of upsets (SEP).

d. Number of transients (SEP).

e. Occurence of latchup (SEP).

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

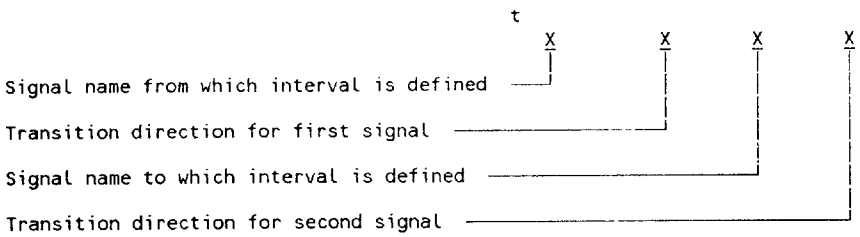
6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38535, MIL-STD-1331, and as follows:

C_{IN}, C_{OUT}	Input and Bidirectional output capacitance, terminal-to-GND.
GND	Ground zero voltage potential.
I_{CC}	Supply Current.
I_{IL}	Input Current Low.
I_{IH}	Input Current High.
T_C	Case Temperature.
T_J	Junction Temperature.
V_{CC}	Positive Supply Voltage.
O/V	Latch-up over-voltage.
O/I	Latch-up over-current.

6.5.1 Timing parameter abbreviations. All timing abbreviations use lower case characters with upper case character subscripts. The initial character is always "t" and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descripters for each signal specify the signal name and the signal transition. The format is as follows:



a. Signal definitions:

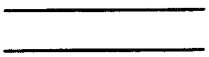
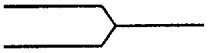
$\overline{E}$ = Chip Enable	$\overline{W}$ = Write Enable	$\overline{G}$ = Output Enable
A = Address Input Bus	D = Data In	Q = Data Out

b. Transition definitions:

H = Transition to High	L = Transition to Low
V = Transition to Valid	X = Transition to invalid or "Don't Care"
	Z = Transition to off (High Impedance)

6.5.2 Timing Limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minumum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.3 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standard Microcircuit Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standard Microcircuit Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

APPENDIX

FUNCTIONAL ALGORITHMS

10. SCOPE

10.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

30. ALGORITHMS

30.1 Algorithm A (pattern 1).

30.1.1 Checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

30.2 Algorithm B (pattern 2).

30.2.1 March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing X-fast sequentially for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing X-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing X-fast from maximum to minimum address locations.

30.3 Algorithm C (pattern 3).

30.3.1 XY March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing Y-fast sequentially for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing Y-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing Y-fast from maximum to minimum address locations.

30.4 Algorithm D (pattern 4).

30.4.1 CEDES - CE deselect checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Deselect device, attempt to load memory with checkerboard-bar data pattern by incrementing from location 0 to maximum.
Step 3. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 4. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 5. Deselect device, attempt to load memory with checkerboard data pattern by incrementing from location 0 to maximum.
Step 6. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.