MOTOROLA

T-51-10-90

Dual A/D Converter

Military 1651

ELECTRICALLY TESTED PER:
MPG 1651 (– 30°C to + 85°C)

The 1651 is a very high speed comparator utilizing differential inputs to sense analog signals above or below a reference level. An output latch provides a unique sample-hold feature. The 1651 is a lower impedance option to the 1650, with higher input slew rate and higher speed capability.

The clock inputs ($\overline{C}_a$ and $\overline{C}_b$) operate from MECL III or MECL 10,000 digital levels. When $\overline{C}_a$ is at a logic high level, Q_0 will be at a logic high level provided that $V_1 > V_2$ (V_1 is more positive than V_2). $\overline{Q}_0$ is the logic complement of Q_0. When the clock input goes to a low level, the outputs are latched in their present state.

- P_D = 330 mW typ/pkg (No Load)
- t_{pd} = 3.5 ns typ
- Input Slew Rate = 500 V/µs
- Differential Input Voltage Range: 5.0 V (– 30°C to 85°C)
- Common Mode Range: – 3.0 V to + 2.5 V (– 30°C to 85°C)
- Resolution: ≤ 20 mV (– 30°C to 85°C)
- Drives 51Ω lines

AVAILABLE AS

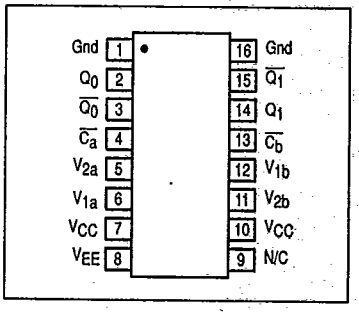
1) JAN: N/A
2) SMD: N/A
3) 883: N/A
4) 1651/BXA *
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F

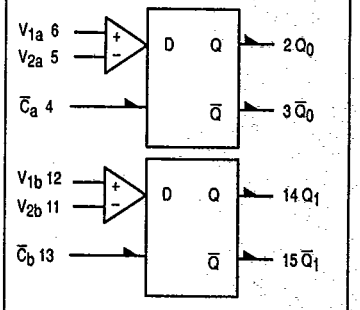
*** 883 Processing (Non-Compliant)**

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	BURN-IN (CONDITION C)
GND	1	5	GND
Q_0	2	6	51 Ω to V_{TT}
$\overline{Q_0}$	3	7	51 Ω to V_{TT}
$\overline{C_a}$	4	8	GND
V_{2a}	5	9	V_{TT}
V_{1a}	6	10	GND
V_{CC}	7	11	V_{CC}
V_{EE}	8	12	V_{EE}
N.C.	9	13	OPEN
V_{CC}	10	14	V_{CC}
V_{2b}	11	15	V_{TT}
V_{1b}	12	16	GND
$\overline{C_b}$	13	1	GND
Q_1	14	2	51 Ω to V_{TT}
$\overline{Q_1}$	15	3	51 Ω to V_{TT}
GND	16	4	GND

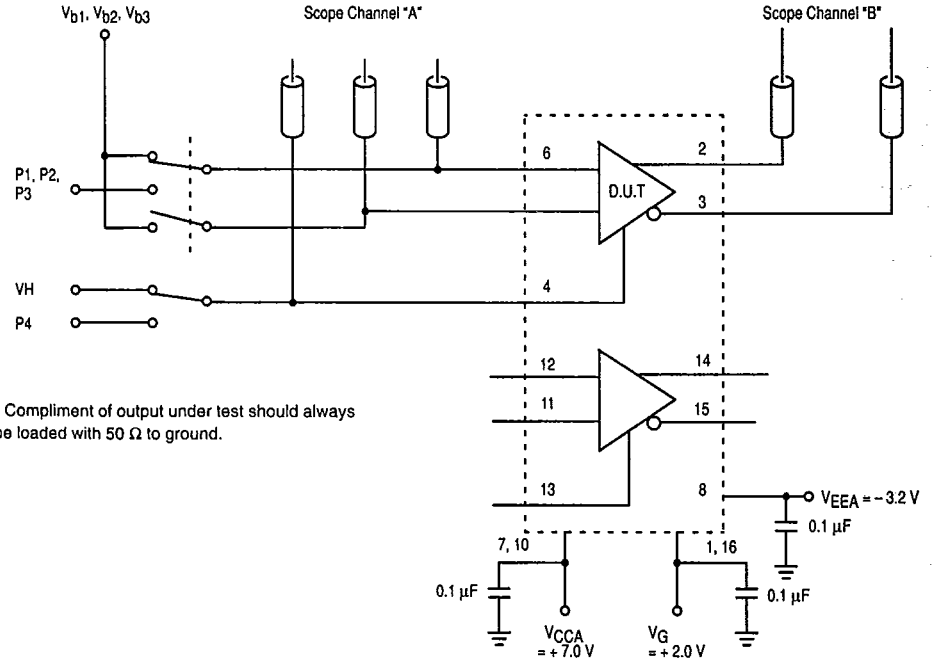


LOGIC DIAGRAM



BURN - IN CONDITIONS:
V_{TT} = – 1.8 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 4.7 V MIN
V_{CC} = + 5.0 V MAX/ + 4.5 V MIN

ABSOLUTE MAXIMUM RATINGS:	Symbol	Min	Max	Unit
Power Supply Voltage	V_{CC} V_{EE}		+ 6.0 − 8.0	Vdc Vdc
Analog Input Voltage	V_{IN}		− 3.0 to + 3.0	Vdc
Gate Input Voltage	V_{IN}		0 to V_{EE}	Vdc
Storage Temperature Range	T_{stg}	− 55	+ 125	°C
Operating Temperature Range	T_A	− 30	+ 85	°C



* Compliment of output under test should always be loaded with 50 Ω to ground.

Figure 1. Circuit Schematic

TRUTH TABLE			
$\overline{C}$	V_1, V_2	$Q0_{n+1}$	$\overline{Q0}_{n+1}$
H	$V_1 > V_2$	H	L
H	$V_1 < V_2$	L	H
L	ϕ ϕ	$Q0_n$	$\overline{Q0}_n$

ϕ = Don't Care

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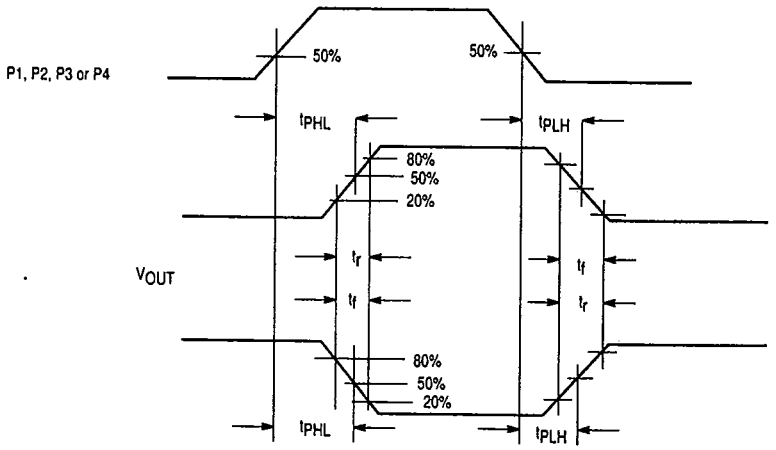
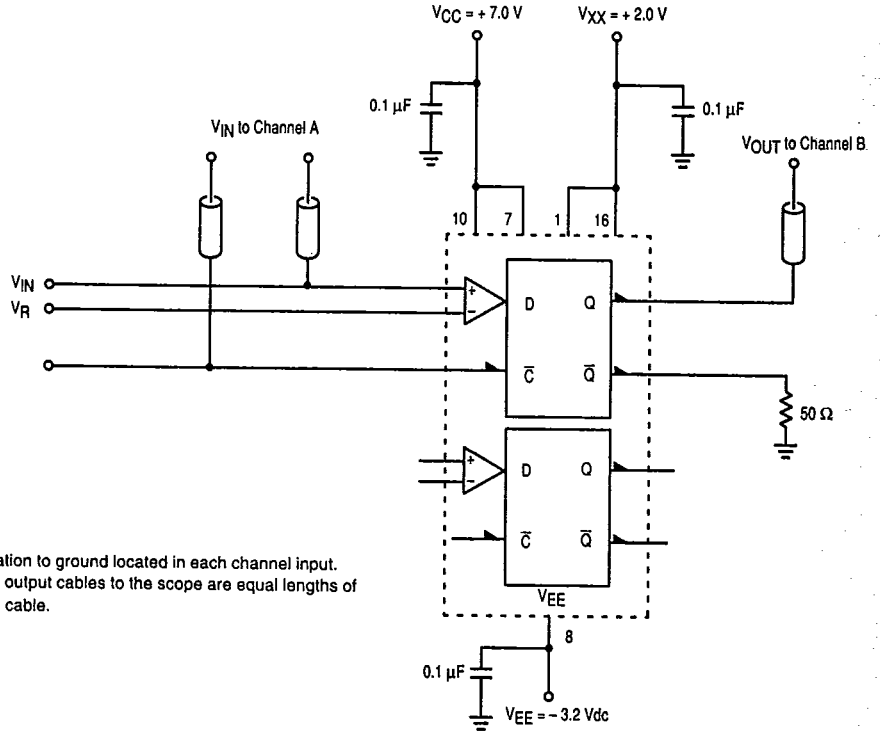


Figure 2. Test Circuit Waveforms



50 Ω termination to ground located in each channel input.
All input and output cables to the scope are equal lengths of 50 Ω coaxial cable.

Figure 3. Clock Enable Time Test Circuit

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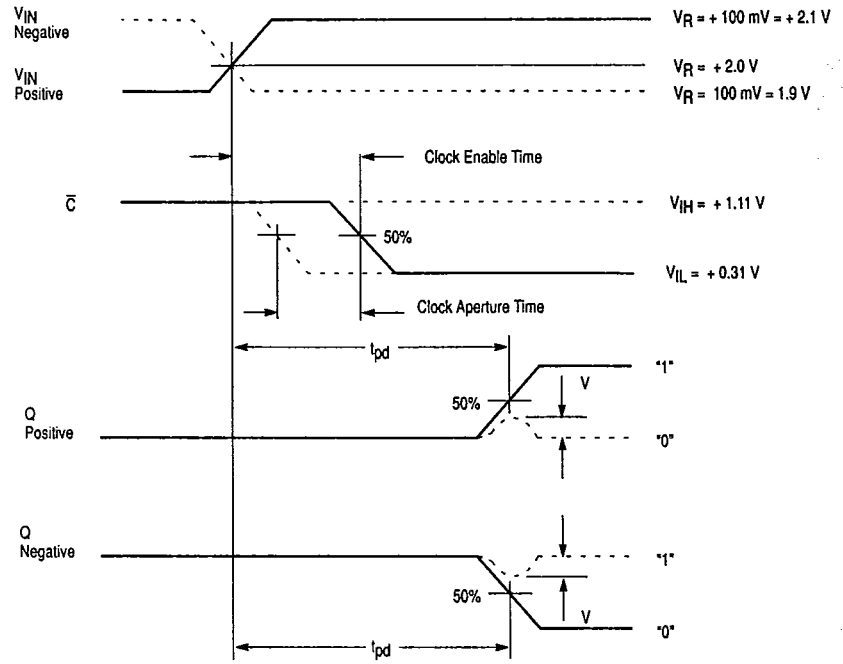

Figure 4. Analog Signal Positive and Negative Skew Case

———— Clock enable time = minimum time between analog and clock signal such that output switches, and t_{pd} (analog Q) is not degraded by more than 500 ps.

- - - - - - Clock aperture time = time difference between clock enable time and time that output does not switch and V is less than 150 mV.

NOTE: All power supply and logic levels are shown shifted 2.0 volts positive.

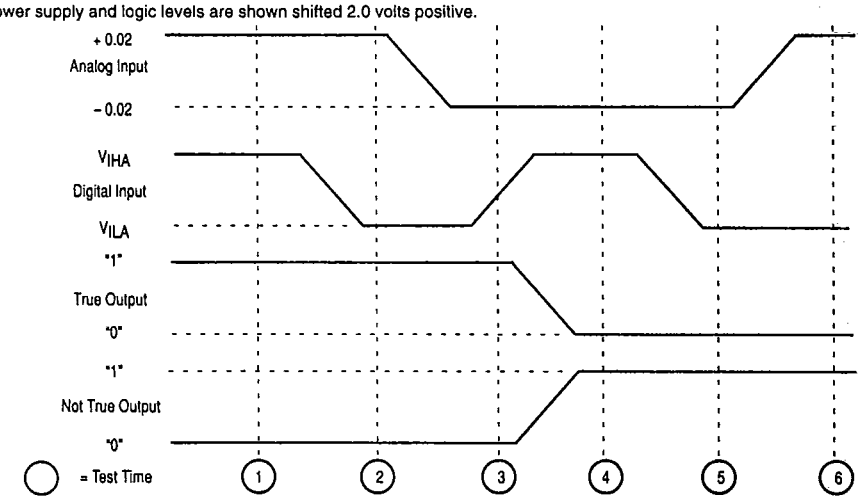

Figure 5. Threshold Pulse Diagram

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QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)											
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{EE}	V_{CC}	V_{A1}	V_{A2}	V_{A3}	V_{A4}	V_{A5}	V_{A6}
T_A = 25 °C	-0.81	-1.85	-1.095	-1.485	-5.2	+5.0	+0.02	-0.02	+2.5	+2.48	-3.0	-2.98
T_A = 85 °C	-0.70	-1.83	-1.025	-1.440	-5.2	+5.0	+0.02	-0.02	+2.5	+2.48	-3.0	-2.98
T_A = -30 °C	-0.875	-1.89	-1.180	-1.515	-5.2	+5.0	+0.02	-0.02	+2.5	+2.48	-3.0	-2.98

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW								
	Functional Parameters:	+ 25 °C		+ 85 °C		- 30 °C			Pinouts referenced are for DIL package, check Pin Assignments Output Load = 50 Ω to - 2.0 V								
		Subgroup 1		Subgroup 2		Subgroup 3											
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{CC}	V_{EE}	V_{A1-6}	GND	P.U.T.
V_{OH}	High Output Voltage	- 0.96	- 0.81	- 0.89	- 0.7	- 1.045	- 0.875	V	4, 13				7, 10	8	5, 6, 11, 12	1, 5, 6, 16	2, 3, 14, 15
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.83	- 1.575	- 1.89	- 1.65	V	4, 13				7, 10	8	5, 6, 11, 12	1, 5, 6, 16	2, 3, 14, 15
V_{OHA}	High Output Voltage	- 0.98	- 0.825	- 0.91	- 0.715	- 1.065	- 0.89	V		4, 6, 12, 13	4, 13	4, 13	7, 10	8	6, 12	1, 5, 6, 16	2, 3, 14, 15
V_{OLA}	Low Output Voltage	- 1.83	- 1.60	- 1.80	- 1.555	- 1.83	- 1.60	V		4, 6, 12, 13	4, 13	4, 13	7, 10	8	6, 12	1, 5, 6, 16	2, 3, 14, 15
I_{INH}	Input Current High		350					µA	4, 13	4, 13			7, 10	8	5, 11	1, 6, 12, 16	4, 13
I_L	Leakage Current	- 10						µA	4, 13	4, 13			7, 10	8	5, 6, 11, 12	1, 6, 12, 16	5, 6, 11, 12

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Test Temperature	Test Voltage Values (Volts)											
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{EE}	V_{CC}	V_{A1}	V_{A2}	V_{A3}	V_{A4}	V_{A5}	V_{A6}
T_A = 25 °C	-0.81	-1.85	-1.095	-1.485	-5.2	+5.0	+0.02	-0.02	+2.5	+2.48	-3.0	-2.98
T_A = 85 °C	-0.70	-1.83	-1.025	-1.440	-5.2	+5.0	+0.02	-0.02	+2.5	+2.48	-3.0	-2.98
T_A = -30 °C	-0.875	-1.89	-1.180	-1.515	-5.2	+5.0	+0.02	-0.02	+2.5	+2.48	-3.0	-2.98

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 85 °C		- 30 °C			Pinouts referenced are for DIL package, check Pin Assignments Output Load= 50 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{CC}	V_{EE}	V_{A1-6}	GND	P.U.T.
I_{INL}	Leakage Current Low	0.5						µA	4, 13	4, 13	7, 10	8	5, 6, 11, 12	1, 5, 6, 12, 16	5, 6, 11, 12
I_{EE}	Power Supply Drain Current	- 55						mA	4, 13		7, 10	8	5, 6, 11, 12	1, 5, 6, 12, 16	8
* I_{CC}	Power Supply Drain Off		+25					mA		4, 13	7, 10	8	5, 6, 11, 12	1, 5, 6, 12, 16	7, 10

* I_{CC} = Total current to pin 7 and 10 tied together.

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QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)							Test Parameter	Test Voltage Values (Volts)		
	V_H	V_G	V_{B1}	V_{B2}	V_{B3}	V_{CCA}	V_{EEA}		P_1	P_2	P_3
T_A = 25 °C	+1.11	+2.0	-0.9	+2.0	+4.4	+7.0	-3.2	V_{IH}	+2.10	+4.5	-0.80
T_A = 85 °C	+1.19	+2.0	-0.9	+2.0	+4.4	+7.0	-3.2	V_R	+2.0	+4.4	-0.90
T_A = -30 °C	+1.04	+2.0	-0.9	+2.0	+4.4	+7.0	-3.2	V_{IL}	+1.9	+4.3	-1.0

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW								
	Functional Parameters:	+ 25 °C		+ 85 °C		- 30 °C			Pinouts referenced are for DIL package, check Pin Assignments Output Load = 50 Ω to GND								
		Subgroup 9		Subgroup 10		Subgroup 11											
		Min	Max	Min	Max	Min	Max		V_H	V_G	V_{B1}	V_{B2}	V_{B3}	V_{CCA}	V_{EEA}	P_{1-3}	P.U.T./V_{OUT}
t_{TLH}	Rise Time	1.0	3.5	1.0	3.8	1.0	3.5	ns	4, 13	1, 16	5, 12	5, 12	5, 12	7, 10	8	4, 6, 11, 13	2, 3, 14, 15
t_{THL}	Fall Time	1.0	3.0	1.0	3.3	1.0	3.0	ns	4, 13	1, 16	5, 12	5, 12	5, 12	7, 10	8	4, 6, 11, 13	2, 3, 14, 15
$t_{pd(1)}$	Propagation Delay	2.0	5.0	2.0	5.7	2.0	5.0	ns	4, 13	1, 16	5, 12	5, 12	5, 12	7, 10	8	4, 6, 11, 13	2, 3, 14, 15
$t_{pd(1)}$	Propagation Delay	2.0	5.0	2.0	5.7	2.0	5.0	ns	4, 13	1, 16	5, 12	5, 12	5, 12	7, 10	8	4, 6, 11, 13	2, 3, 14, 15
$t_{pd(2)}$	Propagation Delay	2.0	5.0	2.0	5.2	2.0	5.0	ns	4, 13	1, 16	5, 12	5, 12	5, 12	7, 10	8	4, 6, 11, 13	2, 3, 14, 15
$t_{pd(2)}$	Propagation Delay	2.0	5.0	2.0	5.2	2.0	5.0	ns	4, 13	1, 16	5, 12	5, 12	5, 12	7, 10	8	4, 6, 11, 13	2, 3, 14, 15
t_{setup}	Setup Time	2.5		2.5		2.5		ns	4, 13	1, 16	5, 12	5, 12	5, 12	7, 10	8	4, 6, 11, 13	2, 3, 14, 15

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